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Defect Level vs. Yield and Fault Coverage in the Presence of an Imperfect BIST

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Abstract Williams and Brown's formula, relating the product defect level as a function of the manufacturing yield and fault coverage, is re-examined in this paper. In particular, special attention is given to the influence of an imperfect built-in self-test (BIST) on this relationship. We show that when the BIST hardware is used to screen the functional product, an imperfect BIST circuitry tends to reduce the effective fault coverage and increase the corresponding product defect level.

1. Introduction

Williams and Brown [1] had shown the relationship between manufacturing yield and the fault coverage of the test process used to screen the product into either a *good* lot or a *bad* lot. This well-known relationship is derived assuming that the test equipment is *perfect*, i.e. fault-free.

Many chips today have BIST circuitry in them. These BIST circuits are used to test the chips and perform the screening described above. Since the BIST hardware is manufactured using the same technology and process as the functional circuits, it is unrealistic to assume that it is fault-free. It is, therfore, imperative to allow the BIST hardware be subjected (during the analysis) to the same defect level (impurity) as the functional circuits themselves. It is the subject of this paper to investigate the effect of an imperfect (i.e. possibly faulty) BIST environment on the William's and Brown's equation. In theory, the side effect of an imperfect BIST is to either cause a good product (i.e. no functional defects present) be declared faulty, resulting in a yield loss, or cause a bad product be passed as good. In practice, however, the first side effect is the predominant one, while the second side effect has very low probability of actually occuring, and, therefore, can be ignored.

In [2,3] the effects of an imperfect tester on the resulting yield during a delay (AC) test is discussed. In [4,5] a more generalized fault probability model is introduced to enhance the defect vs. yield equation. In [6] an experiment using CrossCheck technology is conducted in order to evaluate the relationship between defect level and fault coverage.

This paper is organized as follows. Section 2 is a brief review of Williams and Brown's formula. Section 3 derives the yield equation in BISTed products with imperfect BIST circuitry. We show that the Williams and Brown's equation is a special case of our more generelized formula, i.e. our new formula reduces to Williams and Brown's under perfect BIST circuitry. Section 4 discusses the properties of the newly derived formula by displaying the graphs of some typical case studies. Section 5 draws some conclusions from this analysis.

2. Recapitulation of Williams and Brown's Equation

Let the circuit under test (CUT) have n possible faults, each having the same probability of occurrence, p. The yield, Y, is the probability that the circuit is fault-free, i.e.

$$Y = (1-p)^n \qquad (1)$$

The raw defect level of the product coming out of the manufacturing line (without any test) is

$$D_0 = 1 - Y = 1 - (1-p)^n \qquad (2)$$

Assuming that the test process can detect m out of the n possible fault, the fault coverage is given by

$$F = \frac{m}{n} \qquad (3)$$

A circuit that passes the test is guaranteed to be free of any detectable fault (m in total), but can still possess an undetectable fault that escaped the test. Since there are n-m undetectable faults, the defect level after test is given by

$$D = 1 - (1-p)^{n-m}, \qquad (4)$$

which can be further reduced to

$$D = 1 - [(1-p)^n]^{(1-\frac{m}{n})} = 1 - Y^{1-F} \qquad (5)$$

Thus, this equation assumes that the test process is *fault-free,* i.e. a circuit being declared by the test process to be faulty is *truly faulty*. This is the underlying assumption in the derivation of this formula.

3. Enhanced Equation in the Presence of an Imperfect BIST

The product is assumed to have BIST circuitry besides its own functional circuits. The BIST hardware tests the functional circuits in order to determine whether they are faulty or fault-free. A product that fails the self-test is being discarded (or placed in the bad lot). A product may fail the test even when its functional piece is fault-free due to faulty BIST hardware. This is a clear case of a yield loss. In the sequel we will refer to the product functional circuits as the CUT. We use the following parameters in our analysis:

- D – Product defect level after test under perfect BIST hardware
- D' - Product defect level after test under imperfect BIST hardware
- F - Fault coverage of the CUT under perfect (fault-free) BIST hardware
- F' – Effective fault coverage of the CUT in the presence of an imperfect BIST hardware
- Y - Product yield
- p - Fault probability
- n_c - Total number of possible faults in the CUT
- n_b - Total number of possible faults in the BIST hardware
- m - Number of CUT faults covered by perfect (fault-free) BIST hardware
- m' - Expected number of CUT faults covered by an imperfect BIST hardware
- k - Number of CUT faults covered by a faulty BIST hardware
- m_b - Number of BIST faults covered by the BIST hardware
- α - Ratio between BIST area to the CUT area
- ρ - Fault coverage reduction factor
- μ - BIST circuitry fault coverage by its own test procedure
- λ - Yield coefficient

The meaning of α, ρ, μ and λ will become evident from the following analysis.

Notice that we are allowing the test procedure conducted by the BIST hardware to cover $k<m$ possible CUT faults when faulty. Also, the BIST hardware is assumed to cover $m_b < n_b$ of its own faults.

We proceed to calculate m', the expected number of CUT faults covered by BIST:

$$m' = m \times \Pr\{Good\ \ BIST\} + k \times \Pr\{Bad\ \ BIST\}$$
$$= m(1-p)^{n_b - m_b} + k[1-(1-p)^{n_b - m_b}] \qquad (6)$$

The expected CUT fault coverage, as conducted by the BIST circuitry, is:

$$F' = \frac{m'}{n_c} = \frac{m}{n_c}(1-p)^{n_b-m_b}$$
$$+\frac{k}{n_c}[1-(1-p)^{n_b-m_b}] = \frac{m}{n_c}\{(1-p)^{n_b-m_b}$$
$$+\frac{k}{m}[1-(1-p)^{n_b-m_b}]\}$$

Define:

$$\rho = \frac{k}{m} \tag{7}$$

to be the *fault coverage reduction factor* when the BIST circuitry is faulty. Then,

$$F' = F\{(1-p)^{n_b-m_b} + \rho[1-(1-p)^{n_b-m_b}]\} \tag{8}$$

Eq. (8) can also be written as:

$$F' = F[Y^{\frac{n_b-m_b}{n_c}} + \rho(1-Y^{\frac{n_b-m_b}{n_c}})] \tag{9}$$

The exponent in Eq. (9) can be written as

$$\frac{n_b-m_b}{n_c} = \frac{n_b}{n_c}(1-\frac{m_b}{n_b}) = \alpha(1-\mu) = \lambda, \tag{10}$$

where $\alpha = \frac{n_b}{n_c}$ is roughly the ratio between the BIST circuitry area and the area of the CUT, and $\mu = \frac{m_b}{n_b}$ is the BIST circuitry fault coverage as conducted by BIST itself. We call $\lambda = \alpha(1-\mu)$ the *yield coefficient*.

The effective fault coverage, *F*', can now be written as

$$F' = F[Y^{\lambda} + \rho(1-Y^{\lambda})] \tag{11}$$

The new formula relating the product defect level to the yield and the effective fault coverage becomes:

$$D' = 1 - Y^{1-F'} \tag{12}$$

Example 1: Consider a chip manufacturing line with 90% yield. The chips are screened using their BIST circuitry. The BIST circuitry constitutes 5% of the entire chip area. The BIST procedure has 95% coverage of the functional faults when assumed to be fault-free, and only 40% coverage when assumed faulty. The BIST procedure covers 30% of of its own faults. Compute the chip defect level after its BIST screening.

Solution: We have the following parameters:

$$\alpha = \frac{5}{95} = \frac{1}{19}, \qquad \mu = 0.3,$$

$$\lambda = \frac{0.7}{19} \approx 3.68\times10^{-3}, \ \rho = \frac{40}{95} \approx 0.421$$

$$F' = 0.95[0.9^{3.68\times10^{-3}} + 0.421\times(1-0.9^{3.68\times10^{-3}})] \approx 0.9498$$

$$D' \approx 1-0.9^{1-0.9498} \approx 1-0.9^{0.0502} \approx 5.275\times10^{-3} \approx 5275\,ppm$$

Notice that if we ignore the effects of the BIST, the defect level is:

$$D = 1-0.9^{1-0.95} = 1-0.9^{0.05} \approx 5.254\times10^{-3} \approx 5254\,ppm$$ ■

It is interesting to take note of the following special cases:

(a) If there is no BIST circuitry ($\alpha = 0$), we have $F' = F$, and $D' = D$. This is the Williams and Brown's case. Similarly, in the case where there is a BIST hardware with $\mu = 1$, the formulas also reduce to the Williams and Brown's case.

(b) If the BIST procedure has zero coverage against functional faults while being itself faulty, then $\rho = 0$. The effective fault coverage then reduces to:

$$F' = F\,Y^{\lambda} \qquad (13)$$

The impact of the BIST impurity on the product defect level can be best measured by the differential $\Delta D = D' - D$. In most real–life cases $F' \approx F$, $\lambda \approx 0$. By using calculus approximation techniques, and under the restrictions just described, ΔD can be approximated to be:

$$\Delta D \approx F\lambda(1-\rho)\ln^2 Y \qquad (14)$$

and the ratio $\frac{\Delta D}{D}$ to be:

$$\frac{\Delta D}{D} \approx \frac{F\lambda(1-\rho)\ln^2 Y}{(1-F)(1-Y)} \qquad (15)$$

Example 2: Consider again the case described in Ex. 1. By using Eq. 14 we get:

$$\Delta D = 0.95\times 3.68\times 10^{-3}\times(1-0.421)\times\ln^2 0.9$$
$$\approx 22\,ppm$$

Compare this to the exact result of $21\,ppm$ derived in Ex. 1. ■

4. Some Typical Behavior

In order to see the trend of these newly derived formula, we plot F'/F and $\Delta D/D$ for the parameter ranges $0.9 \le Y \le 0.95$, $0.9 \le F \le 0.99$, $0.4 \le \rho \le 0.6$, $10^{-3} \le \lambda \le 5\times 10^{-3}$. These are typical ranges for IC manufacturing.

In Fig. 1 we show the behavior of F'/F and $\Delta D/D$ as a function of Y, while keeping the other parameters fixed at $F = 0.9$, $\rho = 0.4$, and $\lambda = 0.005$. In Fig. 2 we show the behavior of F'/F and $\Delta D/D$ as a function of ρ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.9$, and $\lambda = 0.005$. In Fig. 3 we show the behavior of F'/F and $\Delta D/D$ as a function of λ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.9$, and $\rho = 0.4$. In Fig. 4 we show the behavior of F'/F and $\Delta D/D$ as a function of F, while keeping the other parameters fixed at $Y = 0.9$, $\rho = 0.4$, and $\lambda = 0.005$.

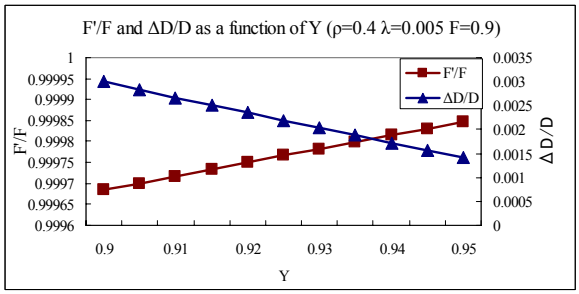

Fig. 1. F'/F and $\Delta D/D$ as a function of Y

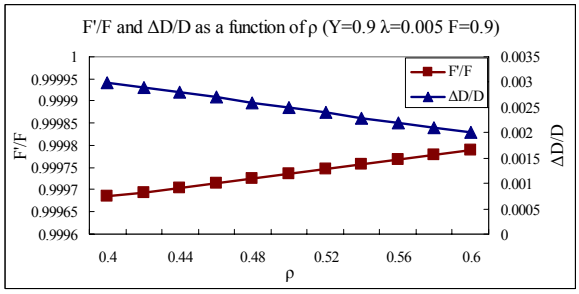

Fig. 2. F'/F and $\Delta D/D$ as a function of ρ

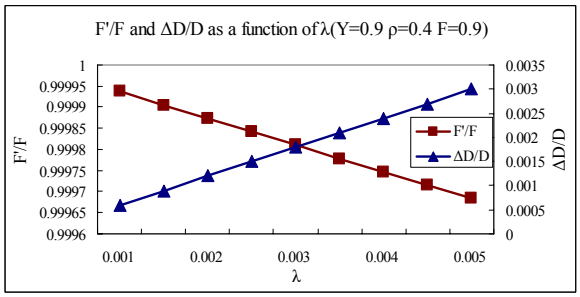

Fig. 3. F'/F and $\Delta D/D$ as a function of λ

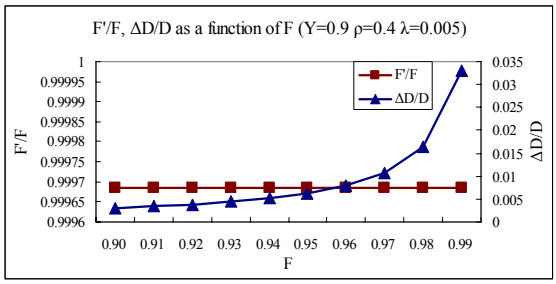

Fig. 4. F'/F and $\Delta D/D$ as a function of F

As seen in these figures, the impact of the BIST circuitry imperfection is minor. The drop in fault coverage, and the defect level increment, rising from the presence of an imperfect BIST circuitry, is quite small.

In Fig. 4, when F is very close to 1 (say F=0.999), the ΔD differential starts to grow substantially faster. The reason for this phenomenon is that in this case D is already very small, and the impact of the imperfect BIST makes D' so much worse compared to D . Since $\Delta D = D' - D$, this differential is noticeably larger than in cases where F is in the neighborhood of 0.99.

5. Conclusions

This paper extends Williams and Brown's formula for products with BIST hardware, where the screening into pass/fail lots is done by the BIST hardware itself. The BIST hardware is assumed to suffer from the same defect density as the functional circuits themselves. The impact of this imperfect BIST is studied in detail. We have shown that the general form of Williams and Brown's formula still holds in this case, provided the CUT's fault coverage is replaced by the CUT's *effective fault coverage*. The impact of this imperfect BIST is to increase the defect level of the products passing the BIST procedure. Formulas to assess this impact have been derived. We have shown that in the range of typical IC manufacturing behavior this impact is quite low.

References

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