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Max-Testable Class of Sequential Circuits having Combinational Test Generation Complexity

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Abstract: The paper uses the concept of time expansion model [9] to find the test generation for acyclic sequential circuits. It identifies a class of sequential circuits called as max-testable sequential circuits, where test generation can be obtained using a combinational test generator with the capability of detecting multiple faults on a kernel of combinational circuit. Any acyclic sequential circuit without hold registers belongs to this class. For the sequential circuits having hold registers, a subset of such circuits are found to be belonged to max-testable class. The paper also suggests an algorithm to find such class of circuits.

1. Introduction

Test generation for a sequential circuit is, in general a hard problem and may be unsolvable in reasonable amount of time for a large circuit [1],[2]. If a test generation problem of a sequential circuit *S* can be reduced to the problem of test generation for a combinational circuit, then *S* is called a sequential circuit with combinational test generation complexity [3]. Generally, it is believed that the cyclic structures of sequential circuits are mainly responsible for making the test generation of such circuits more complex. But even acyclic sequential circuits do not allow test generation with combinational test generation complexity. Several attempts were reported earlier to find the classes of acyclic sequential circuits that can provide combinational test generation complexity. For example, strongly balanced [4], balanced [5], internally balanced [6] are classes of circuit structure with this feature.

If the acyclic sequential circuit contains hold registers, the situation becomes worse for the test generation. In [7], a concept of time expansion graph (TEG) was introduced for testing of acyclic sequential circuits, where test generation is done using a combinational test generator on a combinational kernel circuit called as time expansion model (TEM). In this method all the hold registers are scanned. The concept of this model was later enriched in [8],[9] and attempts were made to find the test generation by not scanning the hold registers.

In this paper we use the concept of TEG and TEM and explore the properties of TEG, which lead us to identify a class of acyclic sequential circuits called as max-testable class for which test generation can be obtained by running a combinational test generator with capability of detecting multiple faults on a combinational kernel. This class includes (i) all acyclic sequential circuits without hold registers and (ii) a subset of sequential circuits containing hold registers. We also present an algorithm to search for such class of circuits.

2. Preliminaries

2.1 Time Expansion Graph (TEG)

Definition 1: (Topology graph) A topology graph is a directed graph $G = (V,A,r)$, where a vertex $v \in V$ denotes a logic block and an arc $(u, v) \in A$ denotes a connection from u to *v* and each arc has a label $r: A \rightarrow Z^+$ (non-negative integers) $\cup \{h\}$.When two logic blocks *u,v* are connected through one or more L-registers, the label *r(u,v)* denotes the number of L-registers (i.e., $r(u,v) \rightarrow Z^+$). When two logic blocks u,v are connected through one hold register, the label r(u,v) =h.

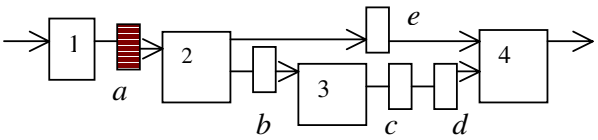

Fig. 1a: The sequential circuit S

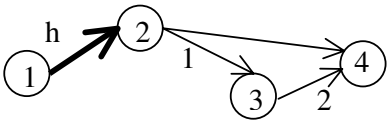

Fig. 1b: The topology graph G of S

Example 1: Consider a sequential circuit S shown in Fig. 1a, in which 1,2,3 and 4 are logic blocks, *b,c,d,* and *e,* are L-registers, and *a* which is highlighted, is a H-register. The topology graph G of S is shown in Fig. 1b.

Definition 2: The set of direct predecessors of any vertex *u* in a directed graph is denoted as *pre(u).* The set of direct successors of any vertex *u* in a directed graph is denoted as *suc(u).*

Definition 3: (Time-expansion graph (TEG)): Let S be an acyclic sequential circuit and let $G=(V,A,r)$ be the topology graph of S. Let $E=(V_E, A_E, t, l)$ be a directed graph, where V_E is a set of vertices, A_E is a set of arcs, t is a mapping from V_E to a set of integers, and l is a mapping from V_E to the set of vertices in G. If graph E satisfies the following five conditions, graph E is said to be a time-expansion graph (TEG) of G.

C1(Logic Preservation) The mapping l is a surjective, i.e., $\forall v \in V, \exists u \in V_E$ *s.t.* $v = l(u)$

C2(Input preservation) Let u be a vertex in E. For any direct predecessor v ($\in$pre(l(u)) of $l(u)$ in G, there exists a vertex u' in E such that $l(u') = v$ and $u' \in pre(u)$.

C3(Time consistency) For any arc (u,v) ($\in A_E$), there exists a corresponding arc $(l(u),l(v))$, and if $r(l(u),l(v)) \in Z^+$, then $r(l(u),l(v))=t(v)-t(u)$, or else $(r(l(u),l(v))=h, t(u) < t(v)$.

C4(time uniqueness) For any pair of vertices u,v ($\in V_E$), if $t(u) = t(v)$ and if $l(u) = l(v)$, then the vertices u and v are identical, i.e., $u=v$.

C5(Hold consistency) For any pair of arcs (u_1,v_1), (u_2,v_2) ($\in A_E$) such that $(l(u_1), l(v_1)) = (l(u_2), l(v_2))$ and $r(l(u_1), l(v_1)) = r(l(u_2), l(v_2)) = h$, if $t(v_1) > t(v_2)$, then either $t(u_1) = t(u_2)$ or $t(u_1) \geq t(v_2)$.

Example 2: Figs. 2a, 2b and 2c show the three TEGs E_1, E_2 and E_3 respectively of the TG G shown in Fig. 1b.

Remark: Note that TEGs E_1 and E_2 are different only in time-frames – they are isomorph to each other. From now on, we consider them as same.

Lemma 1: Given two TEGs E_1 (V_1, A_1,t_1,l_1) and E_2 (V_2, A_2,t_2,l_2) of a TG G (V,A,r), let $u_1 \in V_1$ and $u_2 \in V_2$ are two vertices in E_1 and E_2 respectively such that $l_1(u_1) = l_2(u_2)$. Then for any vertex $v_1 \in pre(u_1)$, there exists a vertex $v_2 \in pre(u_2)$, such that $l_1(v_1) = l_2(v_2)$.

Proof: See [10].

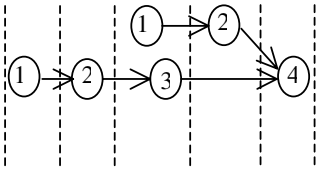

Fig. 2a: TEG of G: E_1

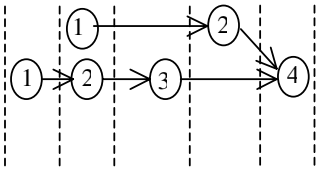

Fig. 2b: TEG of G: E_2

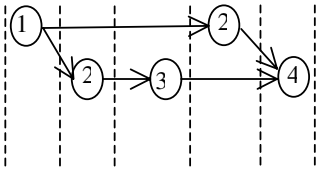

Fig. 2c: TEG of G: E_3

Lemma 2: Let $G=(V,A,r)$ be the TG of an acyclic sequential circuit S, and let $E = (V_E, A_E, t, l)$ be a TEG of G. Consider two vertices v_1 and $v_2 \in V_E$, such that $l(v_1) = l(v_2) = w \in V$. If there exists a vertex $u \in V_E$ such that $(l(u),w)$ and $u \in pre(v_2)$, then $(l(u),w)$ is a hold arc in the TG G.

Proof: see [10].

Lemma 3: Given two vertices u and v in a TEG, all paths between them are having same length.

2.2 Time Expansion Model (TEM)

Definition 4: [9] Let S be an acyclic sequential circuit, let $G=(V,A,r)$ be the topology graph of S, and let $E=(V_E, A_E,t,l)$ be a TEG of G. The combinational circuit $C_E(S)$ obtained by the following procedure is said to be the *time-expansion model (TEM)* of S based on E.

(1) For each vertex $u \in V_E$, let logic block $l(u)$ ($\in V$) be the logic block corresponding to u.

(2) For each arc $(u,v) \in A_E$, connect the output of u to the input of v with a bus in the same way as $(l(u),l(v))$ ($\in A$). Note that the connection corresponding to (u,v) has noregister even if the connection corresponding to $(l(u),l(v))$ has a register (i.e., $r(l(u),l(v)) \neq 0$).

(3) In each logic block, lines and logics that are reachable to neither other ogic blocks nor primary outputs are removed.

Example 3: Fig. 3 is a TEM of the sequential circuit S (Fig. 1a) based on TEG E_1 (Fig. 2a).

Theorem 1: [9] Let S be an acylic sequential circuit, and let F be the set of faults in S. Let $G=(V,A,r)$ be the topology graph of S.

(1) A fault $f \in F$ is testable (or irredundant) in S if and only if there exists a TEG E of G such that the fault $f_e \in F_e$, corresponding to f is testable in the TEM $C_E(S)$ based on E.

(2) A test pattern for a fault f_e ($\in F_e$) obtained using a TEM $C_E(S)$ can be transformed into a test sequence for the fault f ($\in F$) corresponding to fault f_e.

From this theorem, we can see that test generation for an acyclic sequential circuit can be performed by using several different TEMs. Furthermore, since TEMs are fully combinational, a combinational test generator can be used for the test generation provided the test generator can deal with the multiple faults.

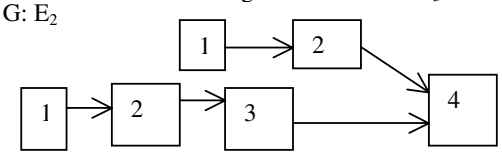

Fig.3: TEM of S based on E_1

2.3 Cover relation

Given a TG, there can be several TEGs for it.

Definition 5: A vertex in a directed graph is called as a *sink vertex*, if there is no outgoing edge from the vertex.

Example 4: The vertex in each of the directed graphs of Figs. 1b, 2a, 2b and 2c is a sink vertex..

Definition 6: Let u is a vertex in TG *G* and let $E(V_E, A_E, t, l)$ be any TEG of *G*. The cone sub-graph $E'(E, u)$ of *E* with respect to *u* is defined as the maximal sub-graph of *E* in which u_E $[l(u_E) = u]$ is the only sink vertex, i.e. there is no other vertex v_E in *E'*, for which $l(v_E)=u$.

Definition 8: Given a TG, if there exist two TEGs E_1 and E_2 for it such that E_1 covers E_2 and E_2 covers E_1, then E_1 and E_2 are said to be equivalent.

Example 7: E_1 (Fig. 2a) and E_2 (Fig.2b) are equivalent.

Remark: If the two TEGs are equivalent, they are not necessarily isomorph to each other.

The question is, given two TEGs E_1 and E_2 for a TG G, how to determine that whether E_1 covers E_2. The answer is, we have to find the mapping *m*, if exists as defined in Definition 7. The following algorithm determines the cover relation by finding the required mapping.

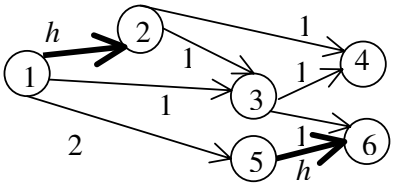

Fig. 4a: TG G_2

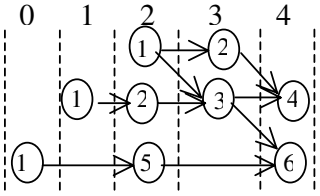

Fig. 4b: TEG E_4 of G_2

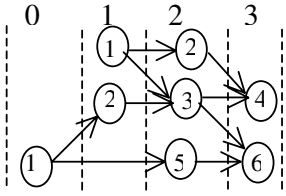

Fig. 4c: TEG E_5 of G_2

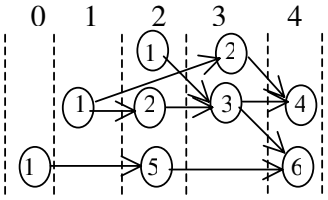

Fig. 4d: TEG E_6 of G_2

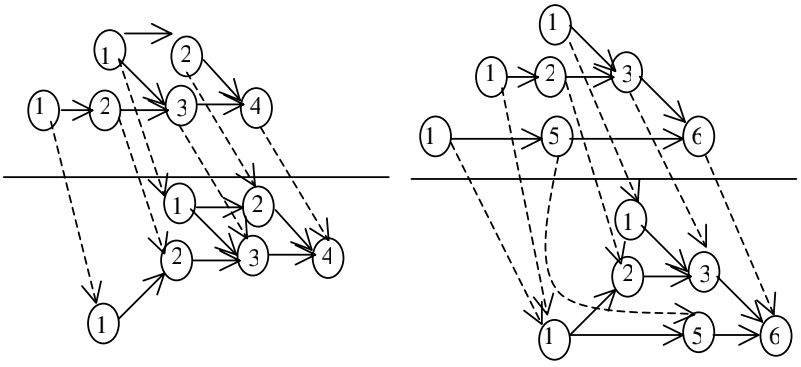

Fig. 4e: The mapping *m* that showing the covering of E_5 by E_4

Definition 7: Let $G = (V, A, r)$ be the TG of an acyclic sequential circuit *S*, and let $E_1 = (V_1, A_1, t_1, l_1)$ and $E_2 = (V_2, A_2, t_2, l_2)$ be arbitrary TEGs of *G*. Let *s* be any sink vertex in *G*. Let $E'_1(E_1,s) = (V'_1, A'_1)$ $[E'_2(E_2,s) = (V'_2, A'_2)]$ is the cone sub-graph of E_1 $[E_2]$ with respect to *s*. TEG E_1 is said to cover TEG E_2 if there exists a mapping m from V'_1 to V'_2, such that for every *s*,

(i) $m(s_1) = s_2$, where $l_1(s_1)= l_2(s_2) =s$

(ii) For $v_1 \in V'_1$ and $v_2 \in V'_2$, if $v_2 = m(v_1)$, then the following condition holds, for any pair of vertices $u_1 \in pre(v_1)$ and $u_2 \in pre(v_2)$, if $l_1(u_1) = l_2(u_2)$, then $u_2=m(u_1)$.

Example 5: Consider the TG G_2 of Fig. 4a. The three TEGs of G_2, E_4, E_5 and E_6 are shown in Figs. 4b, 4c and 4d respectively. E_4 covers E_5 with the mapping shown. Notice that E_4 does not cover E_6.

Example 6: The TEG E_1 (Fig. 2a) and E_2 (Fig. 2b) covers TEG E_3 (Fig. 2c). Obviously, E_1 (Fig. 2a) covers E_2 and E_2 covers E_1

Algorithm Cover-relation *(G,E1,E2)*

Input: TG $G(V, A, r)$, TEG $E_1(V_1, A_1, t_1, l_1)$, TEG $E_2(V_2, A_2, t_2, l_2)$

Output: to find mapping m if E_1 covers E_2, else report "NO COVER"

for every sink vertex $s \in V$

(1) select vertex $s_1 \in V_1$ and $s_2 \in V_2$, such that $l_1(s_1) = l_2(s_2) = s$,
Let $E'_1(E_1,s) = (V'_1, A'_1)$ and $E'_2(E_2,s) = (V'_2, A'_2)$ be cone sub-graphs with respect to *s*.
Make $m(s_1) = s_2$, mark s_1 as mapped

(2) for each vertex u_2 $[u_2 \in V'_2]$ that has a mapping relation $m(u_1)=u_2$, where u_1 $(\in V'_1)$ is already mapped.
for each vertex $v_2 \in pre(u_2)$
(a) find a vertex $v_1 \in pre(u_1)$ with $l_1(v_1) = l_2(v_2)$.
(b) if such v_1 is already mapped,
then (i) report "NO COVER"
(ii) return
else (i) make $m(v_1)= v_2$,
(ii) mark v_1 as mapped

Lemma 4: The algorithm cover-relation establishes the cover relation between two TEGs, if it exists.
Proof: see [10].

Lemma 5: Let $G= (V, A, r)$ be the TG of an acyclic sequential circuit S, and let $E_1 = (V_1, A_1, t_1, l_1)$ and $E_2 = (V_2, A_2, t_2, l_2)$ be arbitrary TEGs of G, where E_1 covers E_2 with a mapping m. Let s_1 and s_2 be any two sink vertices in E_1 and E_2 respectively, such that $l_1(s_1) = l_2(s_2)$. Let $E'_1 = (V'_1, A'_1, t'_1, l'_1)$ $[E'_2 = (V'_2, A'_2, t'_2, l'_2)]$ is the cone sub-graph of E_1 $[E_2]$ with s_1 $[s_2]$ as sink vertex. If v_1 and v_2 are two non-sink vertices in V'_1 and V'_2 respectively, such that, $v_2 = m(v_1)$, then $U_2(v_2) \supseteq U_1(v_1)$, where $U_i(v_i)$ is a set of vertices in TG G given by $U_i(v_i) = \{v \in V \mid v = l_i(u), u \in suc(v_i)\}$.
Proof: see [10].

Definition 9: A path from a vertex u_1 to u_k in a TG $G(V, A, r)$ [TEG $E(V_E, A_E, t, l)$] is obtained by concatenation of several arcs (u_1,u_2), (u_2,u_3), (u_3,u_4), (u_4,u_5),……..,(u_{k-1},u_k) $\forall$ i, $1 \leq i \leq (k-1)$, where $(u_i, u_{i+1}) \in A$ $[A_E]$.

Definition 10: Given a TG $G(V,A,r)$ let $E(V_E, A_E, t, l)$ be any TEG of it, let p be a path from a vertex u_1 to u_k in E obtained by concatenation of the arcs (u_1,u_2), (u_2,u_3), (u_3,u_4), (u_4,u_5), ……., (u_{k-1},u_k) $\forall$ i, $1 \leq i \leq (k-1)$, where $(u_i, u_{i+1}) \in A$ $[A_E]$. The path p' in TG from the vertex v_1 to v_k in TG G passing through vertices $(v_1,v_2, v_3, ……..,v_k)$, where each $v_i = l(u_i)$ is called as the corresponding path of p.

Lemma 6: Let $G = (V, A, r)$ be the TG of an acyclic sequential circuit S, and let $E_1 = (V_1, A_1, t_1, l_1)$ and $E_2 = (V_2, A_2, t_2, l_2)$ be arbitrary TEGs of G.

TEG E_1 covers TEG E_2 if and only if, for any vertex $u_k \in V_1$, there exists a vertex $v_k \in V_2$ which satisfies the following two conditions

(i) $l_1(u_k) = l_2(v_k)$

(ii) for any pair of vertices $u_1 \in P(u_k)$ and $v_1 \in P(v_k)$, if $l_1(u_1) = l_2(v_1)$, and $L_1(u_1,u_k) \cap L_2(v_1,v_k) \neq \phi$, then $L_1(u_1,u_k) \subseteq L_2(v_1,v_k)$.

$P(v)$ denotes the set of all predecessors of v. $L_i(u,v)$ denotes the set of paths $(l(u),……,l(v))$ (in G) corresponding to paths $(u,……,v)$ whose tail and head are u and v in E_i respectively.
Proof: see [10].

The above Lemma basically reaches the definition of cover relation, as described in [9].

2.4 Maximum TEG

Definition 11: Given a TG G, a TEG E which cannot be covered by any other TEG of the TG except by its equivalent TEG, is called a maximal TEG of G. If number of maximal TEGs is one, then that maximal TEG is called as the maximum.

If a TG has a maximum TEG, how can we find out that? One method may be to attempt to draw all TEGs, and then find the maximum TEG among them that covers any other TEGs and cannot be covered by anyone else. Obviously, this process is time consuming and quite impractical. The best way to achieve this maximum TEG is to draw it in such a manner such that it follows the properties of the maximum TEGs. The question definitely arises- while we achieved a TEG, is it easy to confirm whether this TEG is maximum or not? In some cases, the features in a TEG clearly indicates its not being maximum, which can be easily verified, as evident from the following Lemma.

Lemma 7: Given a TEG, if it has no re-convergent fanout, then it is maximum TEG.
Proof: see [10].

Lemma 8: Consider a hold arc h (h_1, h_2) in a TG $G(V,A,r)$. Let $E = (V_E, A_E, t, l)$ is a TEG of G. Consider two vertices v_1 and $v_2 \in V_E$, such that $r(l(v_1),l(v_2)) = h$. If there exist a vertex $u \in V_E$ such that $l(u) = h_1$ and $u \in pre(v_1)$ and $u \in pre(v_2)$, then E cannot be a maximum TEG.
Proof: see [10].

The verification of the condition in the above Lemma is very easy. Because, if we observe in the TEG that if any hold-start vertex originates two hold-end vertices of the same hold arc in the TEG, we confirm that TEG is not maximum. If a TEG is not maximum, it does not imply that it is not also maximal. But obviously, if a TEG is maximal, then there does not exist any maximum TEG of the TG. The condition in the Lemma 8 describes a necessary condition for a TEG to be not maximum, but it is not sufficient.

Lemma 9: Let a TEG E has re-convergent fan-outs. If for every such re-convergent fan-out, no path in the re-convergent loop contains an arc that corresponds to a hold arc in TG, then E is maximum.
Proof: see [10].

Definition 12: Two paths p_1 and p_2 in a TG $G(V,A,r)$ [TEG (V_E, A_E, t, l)] are called parallel to each other with respect to an arc $(v_1,v_2) \in A$ $[A_E]$ if both head and tail vertices of the two paths are same and the arc (v_1, v_2) is not common to both p_1 and p_2.

Theorem 2: Consider a TEG $E(V_E, A_E, t, l)$ of a TG $G(V, A, r)$. The necessary and sufficient condition for E not to be maximum TEG, is that if there exist a pair of vertices $u,v \in V_E$, such that there are at least two parallel paths p_1 and p_2 between u and v, with respect to an arc (v_1, v_2), such that $r(l(v_1),l(v_2)) = h$.
Proof: Let E is such a TEG that there does not exist any pair of parallel paths p_1 and p_2 with respect to an arc (v_1, v_2), such that $r(l(v_1),l(v_2)) = h$. It means, even if there is reconvergent fanout in E, no path in the reconvergent loop contains an arc

that corresponds to hold arc in TG. Obviously in that case E is always maximum (Lemma 9).

Now, let E contains two parallel paths p_1 and p_2 between u and v, with respect to an arc (v_1, v_2), such that $r(l(v_1),l(v_2)) = h$. It implies there exists a re-convergent fan-out between u and v, with the reconvergent loop containing an arc that corresponds to hold arc in TG. We now prove that E can never be maximum.

Let path p_1 (and not p_2) contains the arc (v_1, v_2), such that $r(l(v_1),l(v_2)) = h$. Let us draw another TEG $E'(V'_E, A'_E, t', l')$ in following manner- (i) the paths in E that don't contain the arc (v_1, v_2), are redrawn in E' in identical manner with same time frames. Let p'_2 is the path in E', such that p_2 and p'_2 correspond to the same path in TG and p'_2 passes through the vertices u' and v' in E', such that $l(u)=l'(u')$ and $l(v)=l'(v')$. (ii) For all the arcs from v_2 to v in E, they are drawn in identical manner in E'. Let $l'(v'_2)=l(v_2)$, (iii) for the path p_1 in E, a path p'_1 in E' is drawn with p_1 and p'_1 corresponding to the same path in TG and $r(l'(v'_1),l(v'_2)) = h$, but the length of the arc (v'_1, v'_2), is chosen as a such large value that p'_1 does not pass through u' [let it pass through u'' with $l'(u') = l'(u'')$ and $t'(u'') < t'(u')$. The rest of the paths containing the arc (v'_1, v'_2) are drawn following the rules of drawing TEG.

If we consider the reduced subgraphs $E_{reduced}$ and $E'_{reduced}$ of E and E' by removing the paths containing arc (v_1, v_2) from E and (v'_1, v'_2) from E', as $E_{reduced}$ and $E'_{reduced}$ are identical. If we now consider the complete E and E', for a path p' between u' and v' in E', there always exists a path p between u and v in E, such that p and p' corresponds to same path in TG. In totality, it implies that for any vertex $u_k \in V'$, there exists a vertex $v_k \in V$ which satisfies the following two conditions

(i) $l_1(u_k) = l_2(v_k)$

(ii) for any pair of vertices $u_1 \in P(u_k)$ and $v_1 \in P(v_k)$, if $l_1(u_1) = l_2(v_1)$, and $L_1(u_1,u_k) \cap L_2(v_1,v_k) \neq \phi$, then $L_1(u_1,u_k) \subseteq L_2(v_1,v_k)$.

It implies E' covers E (Lemma 6). Thus E cannot be maximum. Hence the Proof.

Lemma 10: If a TEG E is maximum, then for any path p in it that contains an arc (v_1,v_2) with $r(l(v_1),l(v_2))=h$, there cannot exist any other parallel path to p with respect to (v_1, v_2).

Proof: see [10].

Given a sequential circuit or its TG, if we obtain a TEG by following the method described in the definition, we can easily confirm whether that obtained TEG is maximum or not. We need not draw the other TEGs to compare them with it to check which one covers the other. But suppose, we are failed, given a TG, we have got a TEG E and found that it is not maximum. Obviously, we will try to obtain another TEG that satisfies the properties of the Lemma 10. For a simple structured TG, it may not be a hard task to try for other alternatives. But, if the structure is a complex one and there are several hold registers and paths, this process may not be so easy. Moreover, a TG may not have any maximum TEG. Thus, our efforts may be futile after searching of the different possibilities and then to report that the concerned TG has no maximum. The question is, by observing the TG can we confirm that whether this TG has a maximum TEG or not and if it is having this maximum TEG, how to obtain that in one chance. This is discussed in the next section.

3. The properties of a sequential circuit having maximum TEG

If any arc $(v_1, v_2) \in A_E$ in a TEG $E (V_E, A_E, t, l)$, is a non-hold arc, $len(v_1, v_2)$ is always fixed and that is given by $r(u_1, u_2)$, where $u_1 = l(v_1)$ and $u_2=l(v_2)$. But if (v_1, v_2) corresponds to a hold arc what can be the value for $len(v_1,v_2)$? As a hold register can hold a value for arbitrary amount of time, this $len(v_1,v_2)$ can be any value between 1 and ∞. But there are some restrictions on this length, it depends on the length of other hold arcs in the TEG.

Consider two pairs of vertices (v_1, v_2) and (v'_1, v'_2) in the TEG , such that $l(v_1) = l(v'_1) = h_1$ and $l(v_2)=l(v'_2) = h_2$, where (h_1,h_2) is a hold arc in the TG. In this case, between two arcs (v_1, v_2) and (v'_1,v'_2) in the TEG, depending on one of the lengths, the other length is highly dependent to fulfill the constraint described in condition C5 of the definition of TEG.

Let us introduce a concept of bounded distance between two vertices u and v in a TG, which is defined through the following definitions in the different cases.

Definition 13: Consider a TG $G(V,A,r)$ where $(h_1, h_2) \in A$ is a hold arc and $u \in V$ is a vertex reachable from h_2. Let in each TEG $E(V_E,A_E, t,l)$ of G, v_1, v_2 and $w \in V_E$, are three vertices such that (i) $l(v_1)= l(v_2) = h_2$ (ii) $l(w)= u$ and (iii) $t(v_1) < t(v_2)$. Let p_1^* $[p_2^*]$ is the path from v_1 $[v_2]$ to w and p_1 $[p_2]$ in G is the corresponding path of p_1^* $[p_2^*]$ in E. The path p_3 in TG obtained by concatenation of hold arc (h_1,h_2) with p_1 is called unbounded with respect to p_2. The path p_4 in TG obtained by concatenation of hold arc (h_1,h_2) with p_2 is called bounded with respect to p_3, bounded by a range $\{n_1$ to $n_2\}$ where n_1 and n_2 are two positive integers and $n_1 < n_2$. The values of n_1 and n_2 are obtained in such a manner such that in any TEG $E(V_E,A_E, t,l)$ of TG G, for the pair of paths p_3^* and p_4^* in E with p_3 and p_4 respectively be the corresponding paths in G, if the length of the path p_4^* in E is any value between

n_1 and n_2 (both inclusive), then p_3* and p_4* has no common vertex v for which $l(v)= h_1$.

Definition 14: Let u and v are two vertices in a TG, and there is a path p between them which does not contain any hold arc, then there exists a fixed distance between u and v along the path p, which is given by the summation of the lengths of the different arcs along the path.

Definition 15: If between two vertices u and v in a TG, there exists a bounded path, bounded by a range {d to d'}, then there exists a bounded distance d_{bound} between u and v, which is obtained by assigning any integer value in the range {d to d'} to d_{bound} i.e. $d \leq d_{bound} \leq d'$. If there are several such bounded paths between u and v, there exist several bounded distances between u and v and all these distances depend on how we do assign them in appropriate ranges.

A path p which is unbounded with respect to a path p', may be bounded, when we compare it with another path.

Theorem 3: Between two vertices u and v in a TG G, if there exists one or more bounded paths, and whatever be the assignment, if any bounded distance of a path p becomes equal to bounded or fixed distance of any other path p' between u and v, where p and p' are parallel to each other with respect to an arc (v_1, v_2) where $r(v_1, v_2)=h$, then G has no maximum TEG.

Proof: see [10].

Lemma 12: If a TG has no maximum TEG, then there exist two vertices u and v in TG, such that there are two paths between u and v, where one of them is bounded and the other is either bounded or fixed.

Proof: see [10].

Corollary: If a TG has no maximum TEG, then there exist two vertices u and v in TG, such that there are at least three paths between u and v.

Algorithm to find maxtestabilty

for each sink vertex s in a TG $G(V,A,r)$

(i)Find the set H of head-hold vertices, s.t. for all $u \in H$, there exists at least 3 paths to s and only two of which contain a common hold arc,

(ii) for each $u \in H$

(a) find all the bounded ranges and fixed distances from u to s

(b) assign the bounded distances

(c) if bounded distance of a path p becomes equal to bounded or fixed distance of another path p', where p and p' has at least one uncommon hold arc, then try for another assignment in (b), if no other assignment exists, then report 'not maximum' and return

(d) Draw the TEG with the assignment, this TEG is maximum. Return.

4. Conclusion

We used a model called time expansion model (TEM) to have the test sequences for acyclic sequential circuits. To obtain the TEMs of a sequential circuit, we used time expansion graphs (TEG), constructed from the original sequential circuit by following some conditions, described in the paper. We identify a class of acyclic sequential circuits, called as max-testable class for which the test sequences can be easily achieved by running a combinational test generation tool on a TEM of the circuit, obtained by finding a particular TEG called as maximum TEG. The combinational test generator should have the capability of detecting multiple faults. We presented an algorithm to find max-testable class of circuits. Any acyclic sequential circuit with no hold register belongs to the max-testable class (thus it includes balanced and internally balanced structure). For acyclic sequential circuits with hold registers, we presented an algorithm to determine whether it belongs to max-testable class or not and if it belongs to max-testable class we also find the TEM on which the test generator tool is to be run.

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