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Perfect error identification in at-speed BIST environment

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Abstract

In this paper, we provide a practical formulation of the problem of identifying all error occurrences and all failed scan cells in at-speed scan based BIST environment. We propose a method that can be used to identify every error when the circuit test frequency is higher than the tester frequency. Our approach requires very little extra hardware for diagnosis and identifies errors in practical test application time decided by the frequency ratio between the CUT and the tester. We also propose a diagnosable BIST architecture with error detectors, which reduces the test application time in the proposed error identification method.

Key words: BIST, fault diagnosis, error identification, at-speed test

1 Introduction

Built-in self-test (BIST) has become the major test technique for today's large scale and high speed system-on-chip (SoC) designs. Pseudo-random BIST designs are the most widely used due to their relative simplicity and low cost [1]. Since BIST compacts test responses, BIST requires only small tester memory and it can perform at-speed test even if the test frequency is much higher than the tester frequency.

On the other hand, BIST causes problems in diagnosis due to its compacted responses. Indeed, pass/fail information obtained form BIST response analyzer is insufficient for diagnosis. Two kinds of information are required to identify a fault in the CUT. These are 1) the time information (i.e., the input pattern(s) which causes errors), and 2) the space information (i.e., scan cells where errors occur for scan based BIST architecture [1]). Using time information, fault diagnosis can be performed for a given fault model by methods such as dictionary or fault simulation [2]. Using space information, diagnosis can be performed by cone of logic methods [3]. High resolution diagnostic for a given fault model can be achieved by diagnosis techniques combining space information with time information [4, 5].

For scan-based BIST architecture, finding the time when errors occur as the scan chains are unloaded gives both time (failing input pattern) and space (position of erroneous scan cells within the scan chain) information. A number of methods to identify space information have been proposed, especially for scan-based BIST architecture [6-10], however, only a few practical techniques have been developed to identify time information.

Some of the existing techniques are based on signature analysis using cycling register [11] and error correcting codes [12]. These methods compact the complete test response into one signature and can identify certain errors from the signature. Since they observe signature only once, they are suitable even if circuit frequency is much higher than the tester frequency. However, for large number of error bits, say r errors, they need as many as r-LFSRs or signature registers and may still have diagnostic aliasing over 40% if actual number of errors is higher than r [12]. Thus, they either have poor diagnostic resolution or require impractically high hardware overhead to achieve maximum diagnosis resolution. An alternative approach trades off overhead for time by repeating the test sequence and compacting it at each iteration into a different signature [13]. Thus, instead of using r-LFSRs, the test sequence is repeated r times using programmable LFSR to identify r errors. Since it is mathematically equivalent to [12], diagnostic aliasing is same as using r-LFSRs. Thus, achieving maximum diagnostic resolution requires repeating the test sequence an impractically large number of times.

Techniques that use two phases for diagnostics have also been proposed [14-17]. During the first phase, intermediate signature is checked a few times during test in order to narrow down the failing candidates within some windows. The

failing patterns are then identified inside the windows by applying the corresponding patterns one at a time [14] or by using cycling register [15]. These methods use small hardware overhead or test application time. Furthermore, they can be used even if the circuit frequency is higher than the tester frequency. However, occurrence of aliasing may invalidate the result of this diagnosis. Enhancements of these methods have also been studied using variable window size [16], or multiple signature analyzers [17], but they also do not achieve maximum diagnosis resolution.

The most commonly used diagnosis techniques require both failing space and time information, without compacting responses, during the diagnosis phase [18]. However, this method requires the circuit to operate at the tester frequency during test. Therefore, the faults that affect only at-speed operation may not be diagnosable.

In this paper, we propose a method that identifies every error occurrence in at-speed scan based BIST environment. Every error can be identified even if the circuit test frequency is faster than the tester frequency. In section 2, we formulate the problem of identifying every error occurrence. In Section 3 we introduce an enhanced procedure to identify every error in at-speed scan BIST environment. In Section 4, we give an enhanced version of our method and in Section 5 we show some experimental results. Section 6 summarizes the conclusions of our analysis.

2 Problem formulation

In this section, we formulate the problem of identifying failing response time.

We first identify the differences between diagnosis process and production testing process. Diagnosis can be performed for devices that didn't pass the production test or devices that passed the production test and were found to be faulty in field. In each case, testing during diagnosis should be performed at the same speed which resulted in the failure of the device.

Another difference is that the test application time is not critical for diagnosis. Indeed, typical test application time is at most several seconds, whereas the diagnosis processing on a workstation (effect-cause analysis or fault simulation etc.,) can take several hours. Hence, the quality of diagnosis is far more important than the test application time.

Our first formulation concerns the complete diagnosis of a scan based BIST circuit. In this formulation, we assume that BIST operates at-speed during diagnosis. In the at-speed BIST environment, we assume that the CUT operates at frequency f_c, whereas the tester has a frequency limitation and cannot operate at a frequency higher than f_t, such that $f_t < f_c$. The problem is to locate the errors that occur when applying the test set to the circuit. There are two priorities of objectives. The first priority is to maximize the resolution in error location (i.e., identify every error occurrence at frequency f_c) and the second priority is to minimize the test application time. There are two constraints: (1) The CUT should be tested exactly at frequency f_c, and (2) the tester frequency for observation can be no more than f_t.

In our second formulation, we assume that the actual faults may not depend so much on the frequency at which the fault was originally detected. Thus it may be possible to test the circuit at a frequency lower than f_c and it could be as low as f_l. However, we assume that the tester frequency limitation (f_t) is given. As before, the two priorities of objectives are to maximize the resolution in error location as the first priority while minimize the test application time as the second priority. Again, there are two constraints: (1) the CUT test frequency (f_{CUT}) should be between f_l and f_c ($f_l \le f_{CUT} \le f_c$), and (2) the tester frequency for observation must not exceed f_t. Note that when $f_l = f_c$, this problem reduces to the first problem formulation.

Finally, the goal of the above methods is to achieve the maximum resolution under the given constraints without increasing tester memory and with little or no hardware overhead. Previous works identified in Section 1 do not solve these problems. Some of the techniques do not satisfy the conditions imposed on the tester speed, $f_t < f_c$ [18], while others do not achieve the maximum resolution [11,14-17]. Also, most of the known techniques require substantial hardware overhead [12] or test application time [13].

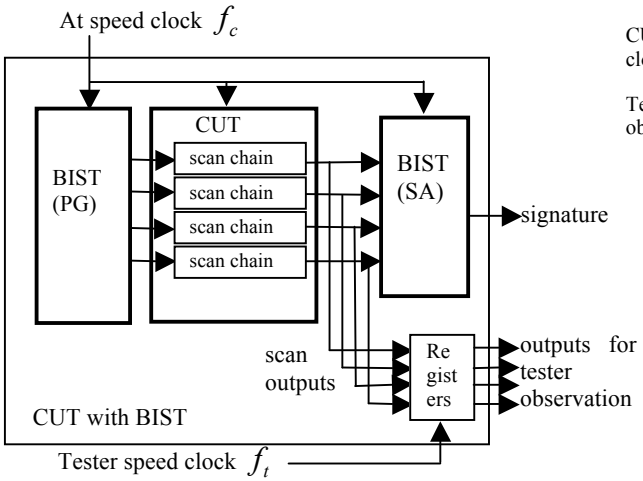

Fig. 1 Diagnosable BIST

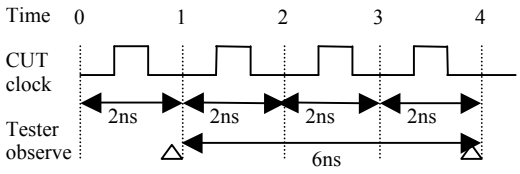

Fig. 2 CUT and observe intervals

Time	0	1	2	3	4	5	6	7	8	•••	•••	124	125	126	127
Scan out	OK	OK	ERR	OK	OK	OK	OK	ERR	OK	•••	•••	OK	OK	OK	OK
observe No.	0	-	-	1	-	-	2	-	-	•••	•••	-	-	42	-

Fig. 3 scan out and observed results

Absolute time (relative time)	0	1	2	3	4	5	6	7	8	•••	•••	124	125	126	127
Scan out	OK	OK	ERR	OK	OK	OK	OK	ERR	OK	•••	•••	OK	OK	OK	OK
Observe No.	0	-	-	1	-	-	2	-	-	•••	•••	-	-	42	-

128 (0)	129 (1)	130 (2)	131 (3)	132 (4)	133 (5)	134 (6)	135 (7)	136 (8)	•••	•••	252 (124)	253 (125)	254 (126)	255 (127)
OK	OK	ERR	OK	OK	OK	OK	ERR	OK	•••	•••	OK	OK	OK	OK
-	43	-	-	44	-	-	45	-	•••	•••	84	-	-	85

256 (0)	257 (1)	258 (2)	259 (3)	260 (4)	261 (5)	262 (6)	263 (7)	264 (8)	•••	•••	380 (124)	381 (125)	382 (126)	383 (127)
OK	OK	ERR	OK	OK	OK	OK	ERR	OK	•••	•••	OK	OK	OK	OK
-	-	86	-	-	87	-	-	88	•••	•••	-	127	-	-

Fig.4 Successful observation

3 Test application method for maximum diagnostic resolution

3.1 BIST architecture and diagnosis problem

Fig.1 shows a BIST architecture and its outputs required for diagnosis. The BIST pattern generator (PG) provides scan inputs, and the signature analyzer (SA) compact its responses. A MISR is used as signature analyzer. The BIST architecture of Fig.1 is the scan-based BIST which is one of the most commonly used architectures. As shown in Fig.1, each scan out is connected to an output port during diagnosis like the non-compaction based approach [17]. Registers are inserted at scan outs to synchronize tester since CUT test frequency may be higher than the tester frequency. If the number of scan chains exceeds the number of output ports available for scan observations, the diagnostic procedure described in this paper can be applied in several steps by applying only a subsets of the scan chains at each step.

As shown in [17], we can identify all failing responses by observing scan outputs if CUT test frequency is slower than the tester frequency limitation. However, if CUT test frequency is higher than tester frequency limitation, a tester will not be able to observe every response. Figs.2 and 3 show demonstrate this through an example. When the CUT clock period is 2ns and the tester observing period is 6ns, a tester can observe only 1/3 of the responses. Thus, it will fail to identify failing responses.

PG, e.g. as an LFSR, returns to initial state after generating the last pattern. If the BIST sequence is 128 cycles long, as shown in Fig.4, every cycle can be observed by repeating the BIST sequence three times (i.e., applying 384 clocks). During the first sequence, the tester observes response bit 0,3,..,126. Then bits 1,4,…,127 are observed during second sequence and bits 2,5,…,128 during the third sequence. However, such method may not be possible to observe all bits in all cases by simple repletion of the sequence. For example if the length of the BIST sequence is 129, or if the tester observes with a period of 8ns, the tester can not observe every response by simply repeating the sequence. In the next section, we derive conditions for observing every response bit and describe a method to identify every error occurrence for the above BIST architecture.

3.2 Problem of observing every response

In this paper, we use the following terms.

Absolute time - The number of scan clock cycles starting from the beginning of the first BIST iteration.

Relative time - The number of scan clock cycles starting from the beginning of the current BIST iteration.

We use the following notation.

N - Length of the BIST test sequence.

P - Period of the tester relative to the CUT test clock period. The available range of P is $1 < P < N$.

$R_{\min}$ - Minimum number of BIST iterations to observe every response.

$M(i)$ - Relative time observed during the i^{th} iteration.
The range of $M(i)$ is $0 \le M(i) < N$

Using the above notation, the method for observing every response can be described as follows.

Observation method: Apply the BIST test sequence of length N $R_{\min}$ times, while observing its response at every time period P.

Our goal is to use the above method to observe all the responses to identify every error occurrence. This maximum resolution observation is defined as follows.

Definition 1. The response at relative time t_i ($0 \le i \le N-1$) can be observed provided that the equation

$$t_i = M(x) \qquad (1)$$

has a solution x. The *resolution* is defined as the number of responses that can be observed. The maximum resolution is N. ■

3.3 Conditions to achieve maximum resolution

In this section, we derive the relationship between P and N to achieve the maximum resolution of observation.

Lemma 1. The response at the relative time 1 is observable if and only if P and N are co-prime (i.e., $\gcd(N, P) = 1$).

Proof. $M(i)$ can be expressed as:

$$M(i) = iP \mod N \quad (2)$$

or,

$$M(i) = iP - kN \quad (3)$$

if the relative time $M(i)$ is observed during k^{th} BIST iterations.

When the response at relative time 1 is observable, the following equation has a solution.

$$M(i) = 1 \quad (4)$$

or,

$$iP - kN = 1 \quad (5)$$

Eq.5 has a solution (i,k) if and only if P and N are co-prime. ■

Lemma 1 shows that $\gcd(N,P) = 1$ is necessary to achieve maximum resolution. Next, we show that it is also sufficient.

Lemma 2. If the number of BIST iterations is no more than P and $\gcd(N,P) = 1$, then the equation

$$M(i) = t \quad (6)$$

has a unique solution.

Proof. If Eq.6 has two solutions i_1, i_2, then $M(i)$ can be expressed in two ways by Eq.3:

$$M(i) = i_1P - k_1N = i_2P - k_2N$$

$$(i_1 - i_2)P = (k_1 - k_2)N \quad (7)$$

Since the number of iterations is smaller than P, we have $0 \le |k_1 - k_2| < P$. Furthermore P divides $k_1 - k_2$ since P divides $(k_1 - k_2)N$ (from Eq.7) and $\gcd(P,N) = 1$. Therefore, $k_1 = k_2$ and $i_1 = i_2$ is deduced. Thus, Eq.6 cannot have more than one solution. ■

Theorem 1. The maximum resolution is achieved if and only if $\gcd(N,P) = 1$ and the number of BIST iterations is P.

Proof. The number of observations in P BIST iterations is PN/P, i.e., N. And since $M(i)$ for every $0 \le i < N$ are different by lemma 2, the set $\{M(i) : 0 \le i < N\}$ has to be {0,1,2,…,N-1}, i.e., the observing resolution is N. Therefore, $\gcd(N,P) = 1$ is a necessary and sufficient condition to achieve the maximum resolution in P iterations. ■

Example 1. Let the length of a BIST sequence be 2^{32} clocks, the CUT test frequency be 500MHz and the tester frequency be 100Mhz. In this case the tester observing period is P = 100/500 = 5, which is co-prime with 2^{32}, therefore the maximum observing resolution is achieved. ■

Example2. Let the length of a BIST sequence be 2^{10} clocks, the CUT test frequency be 600MHz and the tester frequency be 100Mhz. In this case the tester observing period is P = 100/600 = 6, which is not co-prime with 2^{10}, therefore the maximum observing resolution is not achieved. ■

3.4 Adjusting N or P to achieve maximum observing resolution

In Section 3.3, we showed that the maximum resolution of observation is always achieved if N and P are co-prime. However, in general, N and P may not be co-prime. In such cases, the maximum resolution of observation can be achieved by adjusting N and/or P. For the first problem formulation described in Section 2, the following two possibilities exist:

- Increasing the length of BIST sequence N by inserting additional tests or dummy clock cycles.
- Slowing down the tester by increasing tester observation period P.

The adjustment of N and/or P is chosen to minimize the test application time.

Let $N' = N + i$ be the adjusted length of the BIST sequence and $P' = P + j$ be the adjusted tester observing period. The test application time is:

$$TAT = \frac{N'P'}{f_c} = \frac{1}{f_c}(NP + iP + jN + ij) \quad (8)$$

The problem is to find a pair (i,j) that minimizes $iP + jN + ij$, with $N + i$ and $P + j$ co-prime.

Theorem 2. If $N \geq P(P-1)$, The solution (*i,j*) that minimizes Eq.8 with $N+i$ and $P+j$ co-prime is such that $j=0$.

Proof. Since $\gcd(\alpha P+1, P)=1$ for any integer $\alpha \geq 0$, there exists a co-prime of P in any consecutive P integers. Therefore, the range of i in Eq.8 is $0 \leq i < P$. Similarly, the range of j is $0 \leq j < N$. First we consider the case where $j=0$. The worst case of minimum $iP+jN+ij$ is the case of $i=P-1$, therefore:

$$iP+jN+ij=(P-1)P \qquad (9)$$

Next, we consider the case when $j \neq 0$. The best case of minimum $iP+jN+ij$ is the case of $i=0$, therefore:

$$iP+jN+ij=jN \geq N \qquad (10)$$

If $N > P(P-1)$, Eq.10 is always larger than Eq.9. Therefore, $j=0$ is the solution that minimizes Eq.8. ■

A typical tester can operate at about 50MHz and the CUT test frequency in modern DSM circuits in increasing to as high as 5GHz. Thus, we can assume $P<100$. On the other hand, typical N can be of the order of several million, making $N > P(P-1)$. Therefore, in most practical cases it is sufficient to adjust only N by inserting dummy clocks since in such cases $j=0$ provides the optimal solution.

3.5 Procedure for identifying every error occurrence

Summarizing Section 3.1-3.4, the procedure for identifying every error occurrence using diagnosis outputs is as follows.

Given condition

(a) Test frequency of CUT : f_c
(b) Tester frequency limitation: f_t
(c) Initial BIST test length: N
(d) scan cells in a chain: L

Step 1. Set observing time period P as $P = f_c / f_t$.

Step 2. Adjust BIST test length by adding minimum i dummy clocks (i.e., $N' = N + i$) such that N' is co-prime with P.

Step 3. Apply $P \cdot N'$ clocks to BIST pattern generator, observing one scan output every P test cycle.

Step 4. If an error is detected at the i^{th} observation, then:

(a) Relative time of error occurrence e is: $e = iP \bmod N$
(b) Failing scan pattern = $\lfloor e/(L+1) \rfloor$
(c) Erroneous scan cell = e mod (L+1)

Note that the scan chain length is incremented by one to identify the failing scan pattern and erroneous scan cell in order to account for the capture cycle between successive scans.

3.6 Adjusting N or P to achieve maximum observing resolution and minimum TAT

In Section 2, we defined a second problem formulation. It relaxes the constraints of CUT clock frequency f such that $f_l \leq f \leq f_c$, whereas the first formulation only allows $f = f_c$. Note that the test application time is constant; regardless of the CUT clock frequency f because it is dictated by the tester frequency as shown below,

$$TAT = \frac{NP}{f} = \frac{Nf}{f \cdot f_t} = \frac{N}{f_t} \qquad (11)$$

To minimize test application time, CUT clock frequency f is selected from the range $f_l \leq f \leq f_c$ with $P = f / f_t$ and N co-prime. If there is no such P co-prime with N, we select f such that $P = f / f_t$ is co-prime with N+1, and so on. The procedure for identifying every error occurrence for the second problem formulation is as follows.

Given condition

(a) Maximum Test frequency of CUT : f_c
(b) Minimum Test frequency of CUT: f_l
(c) Tester frequency limitation: f_t
(d) Initial BIST test length: N
(e) scan cells in a chain: L

Step 1. Set the maximum observing time period $P_{\max}$ and the minimum observing time $P_{\min}$ as

$$P_{\max} = f_c / f_t, \; P_{\min} = f_l / f_t$$

Step 2. Select P from the range $P_{\min} < P < P_{\max}$, and $N' = N + i$ where i is minimum with P and N' co-prime .

Step 3. Apply $P \cdot N'$ clocks to BIST pattern generator, observing one scan output every P test cycles.

Step 4. If an error is detected at the i^{th} observation, then:

(a) Relative time of error occurrence e is:
$$e = iP \bmod N$$
(b) Failing scan pattern = $\lfloor e/(L+1) \rfloor$
(c) Erroneous scan cell = e mod (L+1)

4 Enhanced approach to reduce the BIST iterations

The approach we introduced in Section 3 solves the problems defined in Section 2. We showed that we have to repeat the BIST sequence at least P times to identify every error occurrence where P is the ratio between the CUT test frequency and the tester frequency.

The approach introduced in Section 3 does not use any signature analyzers. There is a way to reduce the number of BIST iterations if we use signature analyzers as error detectors albeit at the espense of possibility of aliasing during diagnosis.

Fig 5 shows a diagnosable BIST structure with the error detectors. While the tester observes the response of the first iteration of the BIST sequence, signature analyzers compact the responses which are to be observed by the tester in the second and the third BIST iterations. A counter is used to select responses for signature analyzers. If a signature is not erroneous, we can skip the corresponding iteration. For example, if the first signature analyzer detects no error and the second signature analyzer detects an error, tester skips the second iteration and observes the third iteration. Also, during the third iteration the signature analyzers compact the

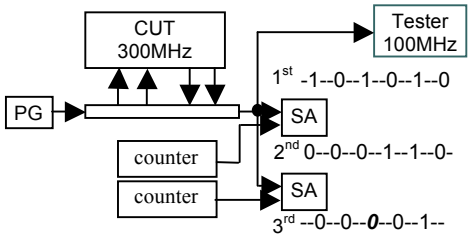

Fig. 3 Diagnosis with error detector SAs

responses which are to be observed by the tester in the 4th and 5th iterations.

It is obvious that if we use more signature analyzers as error detectors, fewer iterations may be required, albeit at the expense of increasing the hardware overhead. The optimal number of signature analyzers will also depend on the probability of error occurrence.

Note that each signature analyzer compacts a sequence of length $\lfloor N'/P \rfloor$. Now, making conventional assumptions about the occurrence of errors [19], the probability that a signature analyzer detects no errors is:

$$\Pr\{no\ error\} = (1 - \Pr\{1\,bit\ error\})^{\left\lfloor \frac{N'}{P} \right\rfloor} \quad (12)$$

If we use n signature analyzers as error detectors, we can skip a BIST iteration only when it has already been checked by a signature analyzer and resulted into no error. Note also that the BIST iteration j cannot be checked by a signature analyzer if all n iterations preceding it have been skipped. Simple combinatorial arguments suggest that the probability of skipping one BIST iteration, $\Pr\{1\,skip\} = x$, is obtained by finding a root of the following equation:

$$\Pr\{no\ error\}x^n + x - \Pr\{no\ error\} = 0 \quad (13)$$

Also, the probability of skipping m ($m \le n$) BIST iterations is:

$$\Pr\{m\,skip\} = \binom{P}{m} (\Pr\{1\,skip\})^m (1 - \Pr\{1\,skip\})^{P-m} \quad (14)$$

Therefore, the expected number of BIST iterations to be skipped is:

$$E(skip) = \sum_{m=1}^{P} m \cdot \Pr\{m\,skip\}$$
$$= P \cdot \Pr\{1\ skip\} \quad (15)$$

Since $\Pr\{1\,bit\ error\} \approx 0$, for $n \ge 2$ Eq.15 can be approximated as:

$$E(skip) \approx P \cdot \Pr\{no\ error\}$$
$$\approx P - N' \cdot \Pr\{1\,bit\ error\}$$
$$\approx P \cdot (1 - \Pr\{1\,bit\ error\})^{\left\lfloor \frac{N'}{P} \right\rfloor} \quad (16)$$

5 Experiments

In order to see the effect of the error detectors that we proposed in Section 4, we plot the reduction ratio $E(skip)/P$ for the following different parameters, $1 \le n \le 10$, $10^{-4} \le \Pr\{1bit\ error\} \le 10^{-3}$, $10^3 \le N \le 5 \times 10^6$ and $1 \le P \le 100$. In Fig. 6 we show the iteration reduction rate as a function of *P*, while keeping the other parameters fixed at $\Pr\{1bit\ error\} = 10^{-4}$, $n = 5$ and $N = 2^{20} - 1$. In Fig. 7 we show the iteration reduction rate as a function of *n*, while keeping the other parameters fixed at $\Pr\{1bit\ error\} = 10^{-4}$, $P = 64$ and $N = 2^{20} - 1$. In Fig. 8 we show the iteration reduction rate as a function of *N*, while keeping the other parameters fixed at $\Pr\{1bit\ error\} = 10^{-4}$, $n = 5$ and $P = 64$. In Fig. 9 we show the iteration reduction rate as a function of $\Pr\{1bit\ error\}$, while keeping the other parameters fixed at $n = 5$, $N = 2^{20} - 1$ and $P = 64$.

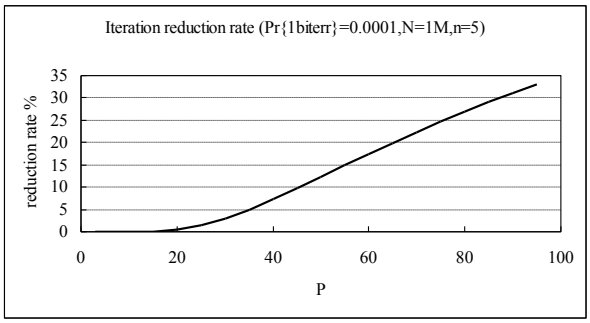

Fig. 4 Iteration reduction rate as a function of *P*

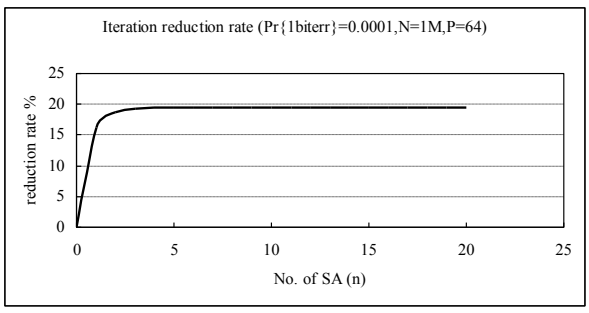

Fig.5 Iteration reduction rate as a function of number of SAs

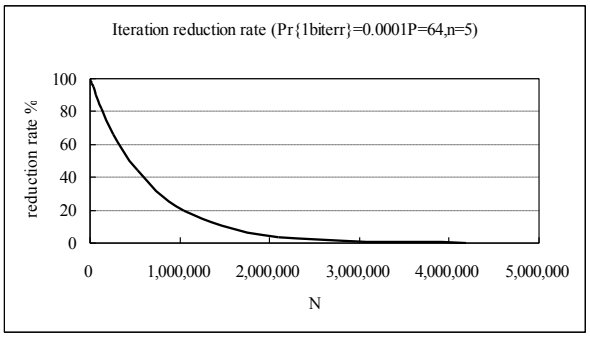

Fig. 6 Iteration reduction rate as a function of *N*

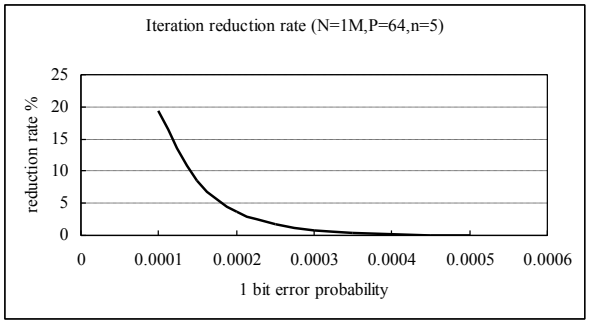

Fig. 7 Iteration reduction rate as a function of 1 bit error probability

Clearly more iterations are required as the CUT clock frequency becomes higher relative to the tester frequency. Fig.6 shows that the use of error detectors reduce the number of iterations and the rate of reduction is linearly proportional to *P*. For an example value of P = 50 the reduction is over 10%. Fig.7 shows that two to three signature analyzers are sufficient as error detectors. The reduction rate is almost constant for more than 3 signature analyzers. Fig.8 and Fig.9 show that the error detectors are no more effective when the length of the BIST sequence is very long or the error probability of 1 bit error is high. However, these conditions rarely occur in practice under scan based BIST architecture. In general, length of the BIST sequence is not very long since typical scan based BIST architectures use shorter length multiple scan chains [1]. Also, the probability of 1 bit error is known to be very low for the scan based BIST designs since scan registers split CUT into smaller independent combinational components and an error is propagated to a very limited number of scan registers.

6 Conclusions

In this paper, we showed a method for identifying every failing pattern and all erroneous

scan cells for the BIST architecture. Our approach is efficient even if the CUT test clock frequency is much higher than the tester frequency. Tester can observe every response in the limited number of BIST iterations determined by the ratio of CUT clock frequency and the tester frequency.

We also proposed a use of signature analyzers as error detectors to reduce the number of BIST iterations. Experimental results show that the error detectors can reduce the number of BIST iterations by more than 10% for the large number of iterations. Experimental results show that two or three signature analyzers are sufficient as error detectors. Therefore, our proposed approach achieves the maximum resolution with very low hardware overhead in practical test application time within the available tester memory.

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