

## A Low Power Deterministic Test Using Scan Chain Disable Technique

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### Abstract

This paper proposes a low power scan test scheme and formulates a problem based on this scheme. In this scheme the flip-flops are grouped into  $N$  scan chains. At a time, only one scan chain is active during scan test. Therefore, both average power and peak power are reduced compared with conventional full scan test methodology. This paper also proposes a tabu search-based approach to minimize test application time. In this approach we handle the information during deterministic test efficiently. Experimental results demonstrate that this approach reduces power dissipation as well as the test application time on various benchmark circuits.

**Key words** low power testing, full scan testing, deterministic test, scan chain disable, tabu search algorithm.

### 1. Introduction

Due to the chip density increasing drastically through the last decade, power dissipation becomes one of the most important factors of very large scale integration (VLSI) design. Furthermore, power and energy consumption of digital systems are considerably higher in test mode than in normal mode [1]. In particular, in the case of scan test, the power dissipation due to clocking all the scan flip-flops is so excessive that it may burn the chip. Hence, many techniques have investigated into power minimization or power constraints test.

Test power dissipation depends directly on the global clock frequency and switching transitions of the circuit under test (CUT) [2]. Therefore, decreasing both the clock frequency and the switching activity can reduce test power. The method [3] reduces average power in sequential circuits by decreasing the test clock frequency. The main disadvantages of this method are that the test

application time increases as the clock frequency decreases and the peak power cannot be reduced.

The main direction to reduce power is to reduce the switching activity in the circuit. Various techniques have been proposed to reduce switching activity during test. The methodologies in [4-7] employ test vector or scan cell reordering technique where test vectors in a test set are reordered for minimal power consumption. The basic idea of these techniques is to find a new order of the test set such that the correlation between consecutive test patterns is increased. The methodologies in [8,9] also explore the correlation between consecutive test patterns by filling each don't care bit in the test cubes with appropriate value 0 or 1.

There are some methods [10-14] that reduce power consumption by using scan chain disabling techniques. Whetsel [10] and Saxena et al. [11] proposed two schemes that divide scan chain into multiple sub-scan chains, and at a time only one sub-scan chain is activated during scan shifting to reduce the power consumption. The power during scan shifting is reduced to  $1/N$ , where  $N$  is the number of sub-scan chains. However, these methods did not consider peak power dissipation. During capture cycle, all the sub-scan chains are active. Therefore, the peak power dissipation may be so high. The scheme in [12] employs two different clocks that work at half of the initial frequency such that these two scan chains is operated at different clock cycle during scan shift. This methodology suffers the same disadvantage with those in [10,11]. In [13], scan chains are grouped into two sets while the given test set  $T$  is divided into two sub-sets. For one test sub-set except for the test group boundaries, only one-group scan chains are active. Hence, this method reduced average power. However, for the other test sub-set, it activates all the scan chains. Therefore, the peak power reduction may not be guaranteed. To reduce the peak power dissipation, Basturkmen et al. [14] proposed a low power pseudorandom

BIST methodology for scan circuits. In this method, the scan chains are partitioned into  $N$  groups. At a time, only the scan chains in a group are active throughout scan cycles and capture cycle. Therefore, both average and peak power dissipation is reduced. However, this method, which suffers from a very long test application time, is not efficient for deterministic test.

In this paper, we present a low power deterministic test methodology for sequential circuits using scan chain disable technique. The flip-flops are grouped into  $N$  scan chains. At a time, only one scan chain is active during scan test. Therefore, this technique reduces average power as well as peak power dissipation. In this paper, we also propose a new approach for minimizing test application time.

This paper is organized as follows. Section 2 presents a low scan test scheme. The test flow is given in section 3. Section 4 shows a problem based on this scheme. Section 5 describes a tabu search-based algorithm to minimize the test application time. Section 6 concludes with a brief summary.

## 2. Proposed Scheme

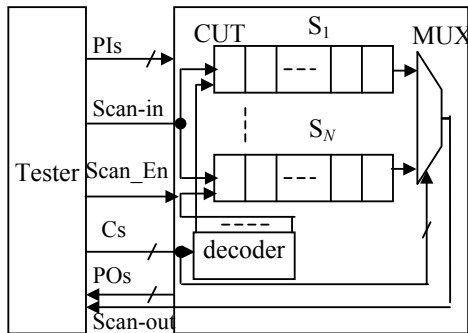


Fig. 1. Proposed scheme

In this section, we present a low power scan test scheme shown in Fig. 1. The proposed scheme divides the flip-flops into  $N$  groups. In this paper, we do not care of the order of flip-flops. The flip-flops in a group are lined into a scan chain according to the order of appearance in the circuit description. Similarly to the scheme in [11], we use a decoder to control which scan chain is active, and a multiplexer to select which scan chain's response can be shifted out, according to the value of control signals ( $Cs$ ) that is given by tester. When  $Scan\_En=1$ , tester applies test vectors and  $Cs$  to

CUT. The main difference between our proposed scheme and the scheme in [11] is that one scan chain is active at both shift and capture cycles rather than only at shift operation.

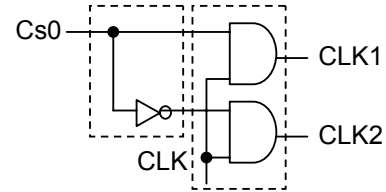


Fig. 2. Decoder and gating logic

Fig. 2 shows a decoder and gating logic to describe the realization of the scheme in the case of  $N=2$ .  $Cs0$  is the signal of a 1-2 decoder. When  $Cs0=1$ , the clock of scan chain 2  $CLK2$  is gated by the gating logic while  $CLK1$  that is the clock of scan chain 1. However, when  $Cs0=0$ , scan chain 1 is disabled while scan chain 2 is activated. A test application procedure is summarized as follows. First, some vector  $t$  is shifted into the scan chains according to the following way. By setting the value of  $Cs0$  that is 1 or 0, the scan chains 1 and 2 are active in turn. The bits corresponding to the activated scan chain are shifted into the scan chain. Secondly, by setting appropriate value  $Cs0$ , only one scan chain captures the test response. If the next vector has the same specified values for the disabled scan chain,  $Cs0$  keeps the same value. We shift in the bits of vector and shift out test response corresponding to the activated scan chain until the other scan chain need to be activated or the bits in disabled scan chain of the vector to be applied are different from that of vector  $t$ . The test response is shifted out. Finally, we continue to apply next vector as shown in above steps until all the test vectors are applied.

Therefore, this scheme can reduce both average and peak power dissipation. The additional hardware elements that are a decoder and a multiplexer are a little higher compared with conventional full scan design.

Though the proposed method has these advantages, if the test response of a fault cannot propagate to the input of activated scan chain, the fault response cannot be captured. In this case, to achieve the same fault coverage with conventional full scan testing, we should repeat this test vector while one of the scan chains that can capture its test response turns active.

If we apply each test vector  $N$  times, and the  $N$  scan chains are active in turn among the  $N$  same vectors, the test achieves the same fault coverage

with conventional full scan design. Although it reduces average power and peak power dissipation, test application time is so long. Fortunately, there are mainly two pieces of information.

- i. Usually, several flip-flops capture the test response of a fault when a test vector is applied. It is enough to test the fault if only one of the flip-flops is active.
- ii. Usually, a fault can be tested by several test vectors in a test set. We can use any one of those test vectors.

If we handle the information efficiently, the test application time can be reduced drastically. Section 5 will describe the approach in detail.

### 3. Test Flow

This section shows a procedure of test. It consists of the following five steps.

The first step is to perform automatic test pattern generation (ATPG) to generate test cubes, and do static compaction to merge the compatible test cubes together.

In the second step, we obtain the test information about which primary outputs (POs) and/or pseudo-primary outputs (PPOs) capture the test response of a fault when applied one test cube. Fig. 3 shows a simple example of a test set with test cubes. Its test information is given in Table 1. The first row shows the test cubes. The second row describes which faults can be detected by the corresponding test cube. The flip-flops that can capture the corresponding fault are given in row 3.

In the third step, the flip-flops are grouped into  $N$  scan chains. At a time, one scan chain is active. The test cubes are divided into  $M$  *D-compatible* sub-sets where the bits have non-conflicting values for the disabled scan flip-flops. The detail information to group flip-flops and test cubes will be shown in section 5. According to the test information, if a fault cannot be tested, we repeatedly apply that test cube while a scan chain that can capture its test response turns active. For example, Fig. 4 except for the last test cube gives the division of flip-flops and test cubes when  $N=2$ . In this example, flip-flops 1 and 2 are grouped into Group 1 and flip-flops 3 and 4 are grouped into Group 2. According to the activity of the grouped flip-flops and D-compatibility, the test cubes 1 and 2 are grouped into a D-compatible sub-set, and the test cubes 3 and 4 are grouped into another D-compatible sub-set. For each D-compatible sub-set, the flip-flops corresponding to the bits in the

rectangle field are active. For the first cube, flip-flops 3 and 4 are active. Therefore, as shown in Table 1, faults 1, 4 and 6 can be detected. However, it lost fault coverage by only applying these four test cubes, since fault 5 is tested by only cube 3 and its test response should be captured by flip-flop 3 but only flip-flops 1 and 2 are active. We duplicate the test cube, and activate the flip-flops in Group 2 shown as the last test cube in Fig. 4.

After that, all X's in test cube are filled with specified value 0's or 1's. For the X's in the disabled scan chains, we fill them in the way of non-conflicting compatibility. For example, the X's in Cube 2 are filled by 0's because the corresponding bits of the Cube 1 that is in the same D-compatible sub-set with Cube 2 are 0's. For the remaining X's, we randomly fill them with 0's or 1's. Therefore, we can randomly fill the X in the fifth cube by 0 or 1.

Finally, fault simulation is done to drop any test vector that does not test any new faults.

Flip-flops	1	2	3	4
	0	0	1	1
	X	X	0	0
	1	0	X	1
	0	1	0	1

Fig. 3. Example of a test set with test cubes

Table 1. Test information for the test cubes in Fig.3.

	Cube 1			Cube 2			Cube 3			Cube 4			
Fault	1	4	6	2	4	7	3	5	6	7	1	3	8
Flip-flop	1,3,4	2,3	4	2,3	3	4	2,3	3	4	4	1,3,4	3	1

Flip-flops	1	2	3	4
	Group 1		Group 2	
	0	0	1	1
	X	X	0	0
	1	0	X	1
	0	1	0	1
	1	0	X	1

Fig. 4. Example for division flip-flops and test cubes for Fig. 3.

In the third step, we mentioned the problem where we group flip-flops, divide and duplicate test cubes. This problem is very complex. To clarify this problem, we introduce the following proposition.

**Proposition 1** The peak power of this scheme is near  $1/N$  of the full scan design method, and hardware overhead is a little higher than that of multiple scan design while keeping the same fault coverage. ■

Therefore, the only factor that needs to be optimized is test application time, which is direct to the total test power.

**Theorem 1** The test application time (clock cycles) of a scan circuit based on the proposed scheme is

$$TAT = n + n \times F / N + M \times F + r \times (F / N + 1), \quad (1)$$

where,  $n$  is the number of original test cubes,  $F$  is the number of flip-flops,  $N$  is the number of scan chains,  $M$  is the number of D-compatible sub-sets, and  $r$  is the number of increased test cubes. ■

If the number of scan chains  $N$  is given, the test application time is in direct proportion to  $M \times F + r \times (F / N + 1)$ . Thus, we formulate the following problem.

#### 4. Problem Formulation

**Problem** Minimize the test application time of a scan circuit under the proposed scheme. Stating it more formally,

Given:

•**Input:** a sequential circuit, its test information, and the number of scan chains  $N$

Task:

•**Output:** Multiple( $N$ )-scan chains design with  $M$  compatible test sets, that achieves:

•**Objective:** minimizing test application time, i.e.

$$M \times F + r \times (F / N + 1). \quad \blacksquare$$

Notice that to minimize test application time, the number of D-compatible sub-sets  $M$  is a more important factor than the number of increased test cubes  $r$ .

### 5. Flip-Flops and Test Cubes Grouping

In this section, we introduce the approach to group flip-flops into  $N$  scan chains and test cubes into  $M$  D-compatible sub-sets. In this approach, to solve the formulated problem, we use tabu search algorithm to explore the solution space.

#### 5.1. Tabu Search-Based Algorithm

Fig. 5 summarizes the tabu search-based algorithm [15]. Line 1 starts with an initial solution, which is obtained by the algorithm from section 5.2. Lines 3-15 are the heart of the optimization process. For every flip-flop in a scan chain, we try every

possible move, which is not in the tabu list (lines 4-5). Here, a move is a term for swapping two flip-flops in different scan chains. After a move, we obtain  $M$  D-compatible sub-sets using the algorithm from section 5.2.3, and compute the test

#### Tabu search-based Algorithm:

1. Generate an initial solution (section 5.2);
2.  $S_{current} \leftarrow S_{init}$ ;
3. repeat{
  4. for every flip-flop in a scan chain{
    5. for every flip-flop in other scan chain
      - do swap, if it is not in tabu list{
      6. Obtain  $M$  D-compatible sub-sets, get  $S_i$  (in section 5.2.3);
      7. Compute  $TAT_i$ ;
      8. }
      9. }
  10. Find  $S_k$  for which  $M \times F + r \times (F / N + 1)$  is minimum;
  11.  $S_{current} \leftarrow S_k$ ;
  12. Record the move into tabu list;
  13. If this solution is the best so far, then
    - set  $S_{best} \leftarrow S_k$ ;
  14. }
15. until #iterations >  $\text{Min}\{N_{itr1}, N_{itr2}\}$

Fig. 5. Tabu search-based algorithm

application time ( $TAT_i$ ) (lines 6-7). We, then, search for a solution<sup>1</sup>  $S_k$  that minimizes the value of the cost function  $M \times F + r \times (F / N + 1)$ , and set  $S_{current} = S_k$ . This move is then recorded in the tabu list (line 12). If this solution turns out to be the best one so far, we set  $S_{best} = S_k$ . The algorithm ends when either the maximum number of iterations is reached ( $N_{itr1}$ ), or the maximum number of iterations since the last obtained best solution exceeds some predetermined value ( $N_{itr2}$ ).

#### 5.2. Generate an Initial Solution

A good initial solution is very important for search algorithms to find a near optimal solution with short computation time. The main idea of this algorithm is that we use the test information to reduce the solution space and group the flip-flops, which should be active to detect some fault when a test cube is applied, as much as possible together to get a good initial solution. This algorithm consists of the following three phases.

<sup>1</sup> A solution is a complete test D-compatible sub-sets with established values for test application time.

**Phase 1.** Reduce the solution space using test information.

**Phase 2.** Group the flip-flops into  $N$  scan chains.

**Phase 3.** Obtain  $MD$ -compatible sub-sets.

### 5.2.1. Solution Space Reduction (Phase 1)

In a test, some faults' test response can be captured by a PO, and some flip-flops should be active to detect some fault when a test cube is applied. This information can reduce the solution space efficiently.

1. For each fault  $f$  in the fault list, if its test response can be propagated to a PO, then the fault  $f$  is removed from the fault list. This is because even if all scan chains are disabled fault  $f$  can be tested by capturing the response at the PO.
2. For each fault  $f$  in the fault list, if there exists only one cube that tests the fault, and only one flip-flop that captures its test response, then record the cube and flip-flop as a test pair  $p(\text{cube}, \text{FF})$ , and remove the fault from the fault list.

Here, the test pair shows the information that the flip-flop should be active once when we apply the test cube.

For example, as shown in Table 1, fault 5 only appears in the columns of Cube 3, and its test response can be captured only by flip-flop 3. Hence, there is a test pair that is  $p(3,3)$ .

3. For each fault  $f$  in the fault list, if it can be tested by a test pair of  $p(\text{cube}, \text{FF})$ , then we remove the fault from the fault list.

The tabu search algorithm will explore the solution space that is reduced by this phase.

### 5.2.2. Group Flip-Flops into $N$ Scan Chains (Phase 2)

Usually, the results of the first phase are not enough to group the flip-flops. In this phase, we use some greedy algorithms to still get some information that if the flip-flop is active when applying a test cube it may test more faults. After that we employ a greedy algorithm to group the flip-flops into  $N$  scan chains.

1. For the faults whose test response can be captured only by one and the same flip-

flop, we obtain the minimum number of cubes that test all the faults when the flip-flop is active, record the test pairs of  $p'(\text{cube}, \text{FF})$ , and remove the faults. We named the set of all the faults as fault set  $F_1$ .

```

1. For ( $i=1$  to  $N$ ) {
2.   from the unselected nodes in  $FTRG$ , select
   the pair with the highest edges weight;
3.   add the pair to group  $i$ ;
4.    $group\_i=2$ ;
5.   while( $group\_i < F/N$ ) {
6.     select a node such that the sum of the
     weights of the edges between the node
     and the already selected nodes in group  $i$ 
     is maximum;
7.     Add the node to group  $i$ ;
8.      $group\_i++$ ;
9.   }
10.}
```

Fig. 6. Flip-flop division algorithm

As shown in Table 1, both test responses of faults 6 and 7 are captured only by flip-flop 4. And Cube 3 can test these faults. Therefore, we record a test pair  $p'(3,4)$ .

2. For the faults that have only one and the same test cube, we obtain the minimum number of flip-flops that capture the test response of all the faults. After that, we record the test pairs of  $p'(\text{cube}, \text{FF})$ , and remove the faults. We notated the set of all the faults as fault set  $F_2$ .

The problems in steps 5 and 6 are equivalent to the minimum prime-implicant covering problem, which is known to be NP-hard. We, therefore, use a greedy algorithm, where we select a cube (flip-flop) that can test (capture) the maximum number of faults from  $F_1$  ( $F_2$ ). We repeat this greedy algorithm until all the faults are tested.

3. For each remaining fault  $f$ , if it can be tested by a pair of  $p'(\text{cube}, \text{FF})$  given by last two steps, then remove the fault.

Notice that we use different notations for the test pair of test cube and flip-flop. This is because the tabu search algorithm will still employ  $p(\text{cube}, \text{FF})$  rather than  $p'(\text{cube}, \text{FF})$ .

4. Partition the flip-flops, such that the number of test pairs, where the flip-flop FF is active during applying the corresponding test cube, is maximized.

Here, we employ a greedy algorithm, where we group the flip-flops into  $N$  scan chains, such that for the test cubes it has the maximum number of test pairs where the flip-flop FF is in the activated scan chain. First, we give some concepts.

**Definition 1** We denote the number of test cubes where both flip-flops  $j$  and  $k$  have the test pair as a *flip-flop relative degree (FRD)*  $w_{j,k}$ . ■

For instance, there are two test pairs about Cube 3,  $p(3,3)$  and  $p'(3,4)$ . Both flip-flops 3 and 4 have the test pair for the same cube 3. And, there does not exist any other test pair of flip-flops 3 and 4. As a result, the  $FRD w_{3,4}=1$ .

**Definition 2** *Flip-flop test relative graph (FTRG)*. Let  $G=(V, E)$  be an weighted undirected graph, where each node  $v_i \in V$  corresponds to a flip-flop and the weight of the edge between two nodes  $j$  and  $k$  is an  $FRD w_{j,k}$ . ■

The greedy algorithm, which is similar to that of [14], groups the flip-flops into  $N$  scan chains shown as Fig. 6.

### 5.2.3. Obtain $M$ D-compatible Sub-sets (Phase 3)

After getting the  $N$  scan chains, the final phase is to obtain  $M$  D-compatible sub-sets. In this phase, we use the greedy algorithm shown as Fig. 7.

## 6. Experimental Results

We have conducted experiments on full scan version of ISCAS89 benchmark circuits. In the experiments, we use the ATPG tool “TestGen” of Synopsys to generate the test cubes and do fault simulation. Table 2 shows the results of our proposed method compared with previous methods. We do not report the fault coverage in the results because it is the same as that of full scan test.

Columns Ckt. and #ff give the circuit name and the number of scan elements respectively. After them, the test application time TAT for  $N$  scan chains is reported, where the  $N$  scan chains are grouped using the procedure of the last section. When  $N=1$ , all the scan flip-flops are kept active

1. For( $i=1$  to  $n$ ) {
2.  $m$ =the number of scan chains that the inside flip-flops have the test pair  $p(\text{cube } i, \text{FF})$ ;
3. If  $m \geq 1$ , then the test cube  $i$  is duplicated into  $m$  test cubes where the scan chains that the inside flip-flops have  $p(\text{cube } i, \text{FF})$  are active in turn;  
Else the scan chain that the inside flip-flops have the maximum number of  $p'(\text{cube } i, \text{FF})$  is activated (in the tabu search algorithm, in this case we randomly select one scan chain to be activated);
4. }
5. For the faults in fault list, remove all the faults that can be detected by the test cubes use the scheme;
6. If there are remaining faults, find the test cube with the activated scan chain such that it can test the maximum number of untested faults; remove the faults from fault list; do this step until the fault list is empty.
7. We regard a test cube as a D-compatible” sub-set; From D-compatible” sub-set 1 to  $n+r$ , if two D-compatible” sub-sets are “D-compatible”, merge them in a “D-compatible” sub-set;
8. Return the “D-compatible” sub-sets;

Fig. 7. Test set grouping algorithm

during test, that is, the conventional full scan test is applied. The following columns show the reduction in average power and peak power for  $N=2$ ,  $N=3$  and  $N=4$  compared to conventional full scan test with one scan chain, and the approach in [10,11] separately. In this experiment, we use the technique of weight transition count described in [8] to estimate power.

In this table, comparing with the conventional full scan test, when  $N=2$ ,  $N=3$  and  $N=4$ , the average power is reduced up to 61.8%, 72.7% and 76.5% respectively. The peak power dissipation is also reduced drastically up to 50.0% when  $N=2$ , up to 65.6% when  $N=3$ , and up to 75.0% when  $N=4$ . In comparison with the method in [10,11], both average power and peak power are reduced, especially the peak power. The maximum reduction ratios in peak power dissipation are the same with that of the conventional full scan test though they are sometimes a little smaller. For test application time, except S1423, our method can achieve better results than that of the other two methods. For

Table 2. Results of Power Saving Using Scan Disable technique

Ckt.	#ff	TAT(clock cycles)				Power Red. (%) (N=2)				Power Red. (%) (N=3)				Power Red. (%) (N=4)			
		N=1	N=2	N=3	N=4	vs. conv.scan		vs. [10, 11]		vs. conv.scan		vs. [10, 11]		vs. conv.scan		vs. [10, 11]	
						Av.	Pk.	Av.	Pk.	Av.	Pk.	Av.	Pk.	Av.	Pk.	Av.	Pk.
S838	32	6500	6219	4718	4151	49.9	50.0	0.1	50.0	65.3	65.6	1.8	65.6	74.0	75.0	1.1	75.0
S953	29	3149	2477	2030	1965	51.8	31.8	6.1	16.7	64.8	54.5	2.1	44.4	72.9	63.6	7.4	55.6
S1196	18	3419	2084	1546	1336	61.8	46.7	38.0	46.7	72.7	60.0	28.6	60.0	76.5	66.7	19.6	66.7
S1238	18	3514	2257	1603	1382	53.0	42.9	11.0	42.9	70.2	57.1	23.9	57.1	75.6	64.3	16.4	64.3
S1423	74	3974	4679	4699	5015	53.4	34.9	7.9	28.2	67.8	53.5	6.4	48.7	74.4	65.1	3.0	61.5

example, applying test to S1196 the test application time is reduced by 60.9% when  $N=4$ .

From the table, we can conclude that the proposed method is efficient in reducing both average power and peak power dissipation during test without loss the fault coverage. Notice that, some other power reduction techniques, such as test vector reordering, scan cell reordering and minimum transition fill (MT-fill), adapt to this method. If we apply one or more these techniques to this method, both average power and peak power dissipation can be reduced significantly. This method is also efficient to reduce test application time that is one of the most important factors in the test.

## 7. Conclusions

This paper proposes a low power scan test scheme. In this scheme, both average power and peak power reduction is achieved by activating only one scan chain during scan test. To minimize test application time as well as the total test power, this paper also formulates a problem based on this scheme. A tabu search-based algorithm is presented to solve the problem. Experimental results show that the our proposed approach is more efficient in reducing average power, peak power and test application time compared with full scan test methodology.

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