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Using Weighted Scan Enable Signals to Improve the Effectiveness of Scan-Based BIST *

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Abstract

Unlike deterministic testing, it is unnecessary for scan-based BIST to apply a complete test vector into the circuit via the scan chains. A new scan-based BIST scheme is proposed by properly controlling the test signals of the scan chains. Different weighted random signals are assigned to the test signals of different scan chains. In the proposed test scheme, capture cycles can be inserted at any clock cycle. Testability calculation procedure according to the proposed testing scheme is presented. Techniques for selecting different weights on the test signals of the scan chains are also proposed. Experimental results show that the proposed method can improve the test effectiveness of scan-based BIST greatly, and most circuits can reach complete fault coverage or very close to complete fault coverage.
Keywords: Test signal, scan-based BIST, random testability, weighted random testing.

1 Introduction

Conventional scan-based BIST can be simply classified into two types: *Test-per-scan* and *test-per-clock* [11]. In the *test-per-clock* test scheme, the scan flip-flops capture test responses at every clock cycle. An example *test-per-clock* test scheme is the BILBO [11] structure. However, a test vector is first shifted into the scan chains in *test-per-scan* BIST scheme, and a functional cycle is adopted to capture test responses after that. The test responses captured in the scan flip-flops are shifted out when the next test vector is scanned in. Unlike the *test-per-clock* scheme, data inputs of all scan flip-flops are unable to be observed during the shift cycles using the *test-per-scan* BIST scheme. PSBIST [12] combines partial scan design with pseudo-random testing, which should be a trade-off between both BIST schemes. Most of the current *test-per-scan* BIST schemes are based on the *stumps* parallel scan architecture [2].

Test length of scan-based BIST is usually determined by the random resistant faults. Test length reduction of the random resistant faults should be an important issue. Various techniques are adopted to handle the problem. The most popular techniques include (1) weighted random testing [3,10,13,14,16,18,19] and (2) test point insertion [12,17,20,21]. Other methods include designing a more effective test generator [5,6,7] or reseeding techniques [8].

We are interested in weighted random testing. Weighted random testing has been studied for about three decades. Weighted random testing refers to apply test patterns that have different signal probabilities (the probability to assign value 1 to a specific line by a random vector) instead of 0.5 to primary inputs in order to reduce test length or test application time to reach a given fault coverage. The signal probability of a primary input is the weight of the primary input. Muradali, Agrawal, and Nadeau-Dostie [13] computed weight set based on fault propagation characteristics of gates in the circuit. Bardell, McAnney, and Savir [3] proposed a procedure to propagate the weight at each gate backward to the primary inputs to maximize fault coverage, calculation of which is very simple. The procedure to generate weight set for primary inputs in [3] was further modified for LSSD designed circuits in [16]. Wunderlich [19] formulated the weighted random testing problem as the one to maximize the probability to detect all faults in the circuit. The weighted test generation method in Pomeranz and Reddy [14] tried to cover the deterministic test set for complete fault coverage. Kapur, Patil, Snethen, and Williams [10] proposed a method to select weights based on proven ineffectiveness of the test vectors via fault simulation.

Recently, Tsai, Cheng, and Bhawmik [17] proposed a novel BIST scheme, which selected a small number

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of non-scan flip-flops in the circuit. The method also inserts multiple capture cycles after the scan shift cycles during a test cycle. Both techniques can improve observability of the circuit, and thus the test effectiveness of the scan-based BIST. An improved method of the above paper was presented recently in [9]. The method in [9] can increase the proportion of at-speed test and enhance test quality of scan-based BIST.

In this paper, a new scan-based BIST scheme is introduced. It is not believed that a test vector must be shifted completely like deterministic testing. Unlike the conventional *test-per-scan* scheme, our method can insert capture cycles at any time if necessary. The proposed method is an alternative weighted random testing method, which does not need to add a more complicated test generator or modify the scan flip-flops. Our method only needs to assign different weights on the test signals of the scan chains. Experimental results show that the proposed method can improve the test effectiveness greatly.

In the rest of this paper, notation and definitions are presented in Section 2, respectively. The new scan-based BIST architecture is presented then in Section 3. The implementation of the scan-based BIST scheme is introduced in Section 4, which selects weights for the test signals of the scan chains. Experimental results of the proposed method and comparison with previous approaches are given in Section 5. Section 6 concludes the paper finally.

2 Notation and Definitions

Several necessary definitions should be presented first. In the conventional *test-per-scan* test scheme, a *scan cycle* is the period in which a test pattern is shifted into (or test responses are shifted out of) the scan chains. The length of a scan cycle (the number of clock cycles) is equal to the number of scan flip-flops in the longest scan chain. A *capture cycle* is the period between two adjacent scan cycles. The circuit is set to the normal mode during the period when the test pattern is applied to the circuit and the test responses are captured in the scan flip-flops. A *test cycle* consists of a scan cycle followed by a capture cycle.

The $i-$controllability $C_i(l)$ ($i \in \{0,1\}$) measure of a node l is defined as the probability for a randomly selected input vector to control l as value i. The observability $O(l)$ is defined as the probability for a randomly selected input vector to propagate the value of l to a primary output or scan-out signals of the scan chains. The *signal probability* of a node is the same as its $1-$controllability measure.

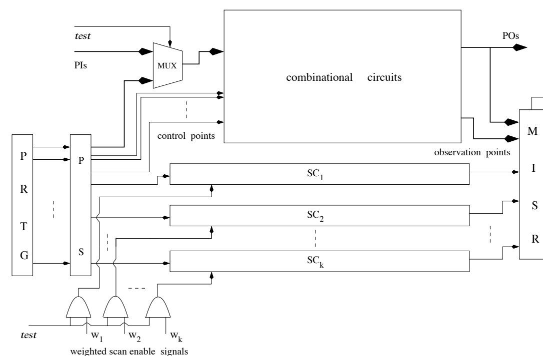

Figure 1: Assign different weights to the test signals of the scan chains.

3 The New Scan-Based BIST Architecture

A new architecture is presented to improve the effectiveness of scan-based BIST in Fig. 1. As shown in Fig. 1, only scan flip-flops in the same scan chain are assigned the same weighted test signal, but not all scan flip-flops in the circuit. All weighted signals are assigned to the scan chains when *test* is set as 1. In the scan-based architecture as shown in Fig. 1, different weights w_1, w_2, ..., and w_k are assigned to the test signals of the scan chains SC_1, SC_2, ..., and SC_k, respectively, where $w_1, w_2, \ldots, w_k \in \{0.5, 0.625, 0.75, 0.875\}$. The reason why we do not assign any weight less than 0.5 to the test signals should be that our method does not hope to insert more capture cycles than scan shift cycles.

Our method presents an effective method to select weights for the test signals of scan chains. Selection of the weights on the test signals of the scan chains is determined by the following testability cost function,

$$G = \sum_{l/i \in F} \frac{|C_1(l) - C_0(l)|}{O(l)}, \qquad (1)$$

where l/i represents the stuck-at i ($i \in \{0,1\}$) fault at line l. In Equation (1), F is the random resistant fault set that contains the faults, whose detection probability is no more than 10 times of that of the hardest fault. It should be noted that our method does not consider redundant faults according to the COP measure [4]. Our method tries to minimize the above cost function.

Assume all scan chains use separate test signals. We consider assigning one of the following weights $\{0.5, 0.625, 0.75, 0.875\}$ to each test signal of the scan chains. The procedure to determine weights can be

Procedure select–weight–for–test–signals()
{
Assign the same values to the test signals as the ordinary test–per–scan BIST scheme to all scan chains. That is, all test signals are assigned as 1 in a sequence of scan shift cycles, and 0 for the following capture cycle.
while the scan chain set S is not empty, do
{
select a scan chain SC from the scan chain set S, and delete SC from S select the best weight w from the weight set {0.5, 0.625, 0.75,0.875} that makes the cost function as stated in Equation (1) minimum. If no weight can be selected for a scan chain, set that test signal like the conventional test–per–scan scheme. The selected weights and the testability estimation procedure is adopted to evaluate the cost function.
}
}

Figure 2: Procedure to select different weights for the test signals of the scan chains.

illustrated as follows: First, all scan chains uses the common *test-per-scan* test signals. That is, the test signal is set as 1 in a sequence of scan shift cycles and set as 0 in a following capture cycle for each test cycle. Our method selects a weight for the first scan chain test signal that makes the cost function minimum. After the best weight has been selected for the first scan chain, our method selects the best weight for the test signal of the second scan chain that minimizes the cost function as presented in Equation (1). For each scan chain, if no weight can be selected, just leave its test signal as the one in conventional *test-per-scan* test scheme. Continue the above process until proper weights have been chosen for all test signals of the scan chains.

The detailed procedure to determine weights for the test signals is presented in Fig. 2. The details to calculate testability of the circuit will be introduced in the following section.

Our method does not need to insert complex hardware into the original circuit in order to generate different weights for the test signals of the scan chains. The weighted signals assigned to the test signals of the scan chains can be generated easily. As shown in Fig. 3, the biased signals 0.625, 0.75, and 0.875 can be generated. The signal of weight 0.625 can be produced by connecting two random signals with a 2-input AND gate, whose output is connected with a 2-input OR gate. Another input of the OR gate is a pseudo-random signal. The signal of weight 0.75 can be obtained from the output of a 2-input OR gate, whose inputs are pseudo-random signals. The signal of weight 0.875 can be got from the output of the 3-input OR gate, whose inputs are pseudo-random signals. Weights assigned to the test signals of the scan chains do not need to be updated in the process of

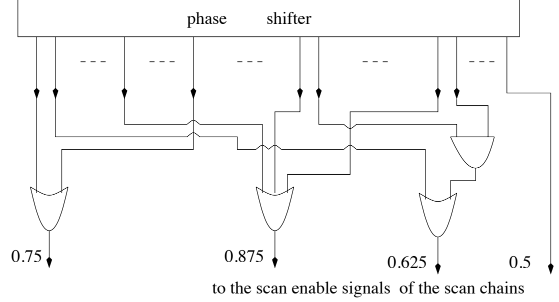

Figure 3: Logic to generate different weights.

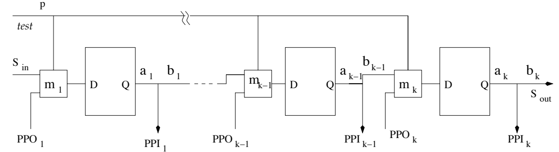

Figure 4: A scan chain with a weighted test signal.

test, therefore, all scan chains that need to be assigned the same weight should be driven by the same signal. Area overhead to generate different weights should be trivial.

4 Testability Issues

We would like to illustrate how to estimate testability when assigning different weights on the test signals. Testability estimation is based on the COP [4] measure. Much attention would be paid to testability analysis with respect to the scan chains.

4.1 Controllability Estimation

As shown in Fig. 4, a weight p is assigned to the test signal of the scan chain. Let k be the length of the scan chains, the signals PPI_i and PPO_i are the pseudo-primary inputs and pseudo-primary outputs of the ith scan flip-flop for $i = 1, 2, \ldots, k$. Signal probability of the signal PPI_1 can be calculated as follows,

$$C_1(PPI_1) = \frac{1}{2} \cdot p + C_1(PPO_1) \cdot (1 - p), \qquad (2)$$

where p is the weight of the test signal. In Equation (2), the first term on the right hand indicates the probability for the signal PPI_1 to be set as value 1 by the pseudo-random input S_{in} when the scan chain is set as the test mode, and the second term represents the probability for the signal PPI_1 to be assigned value 1

by its data input PPO_1 when the scan chain is controlled to be the functional mode. The signal probability of PPI_2 can be calculated as follows,

$$C_1(PPI_2) = p \cdot C_1(a_1) + C_1(PPO_2) \cdot (1-p), \quad (3)$$

where $C_1(a_1) = C_1(PPI_1)$. The first term in Equation (3) represents the probability for the pseudo-primary input PPI_2 to be set as value 1 when the scan chain is set as the test mode, and the second term in Equation (3) stands for the probability for the signal PPI_2 to be assigned value 1 by its data input when the scan chain is controlled to be the functional mode. Similarly, we can obtain testability measure of signal PPI_k as follows,

$$C_1(PPI_k) = p \cdot C_1(a_{k-1}) + (1-p) \cdot C_1(PPO_k). \quad (4)$$

where $C_1(a_{k-1}) = C_1(PPI_{k-1})$. Signal probability calculation for combinational nodes should be the same as the conventional *test-per-scan* BIST using the COP [4] measure.

4.2 Observability Estimation

Observability measures of all nodes corresponding to the scan chains with the weighted test signals can be obtained as follows. First, let us consider the last scan flip-flop as shown in Fig. 4.

$$O(a_{k-1}) = 1-(1-O(PPI_{k-1}))\cdot(1-O(b_{k-1})), (5)$$

$$O(b_{k-1}) = p \cdot O(a_k) = p, \quad (6)$$
$$O(PPO_k) = O(a_k) \cdot (1-p) = 1-p. \quad (7)$$

In Equation (5), we think the fault effect on a_{k-1} can be observed if it is able to be observed from either of PPI_{k-1} and b_{k-1}. The fault effect on b_{k-1} can be observed if the node a_k is observable and the scan chain is set as test mode. The fault effect on the pseudo-primary output of the kth scan flip-flop is observable if the node a_k is observable and the scan chain is set as the functional mode. Observability corresponding to the second scan flip-flop can be calculated as follows,

$$O(a_2) = 1-(1-O(PPI_2))\cdot(1-O(b_2)), \quad (8)$$

$$O(b_2) = p \cdot O(a_3), \quad (9)$$
$$O(PPO_2) = O(a_2) \cdot (1-p). \quad (10)$$

Similarly, observability of signals corresponding to the first scan flip-flop can be evaluated as follows,

$$O(a_1) = 1-(1-O(PPI_1))\cdot(1-O(b_1)), \quad (11)$$

$$O(S_{in}) = p \cdot O(a_1), \quad (12)$$
$$O(PPO_1) = O(a_1) \cdot (1-p). \quad (13)$$

Equations (2)-(13) are utilized to evaluate the cost function, which is used to select weights for all scan chains by minimizing the cost function as presented in Equation (1). It should be noted that iterative testability calculation may be necessary, which can be converged very quickly.

5 Experimental Results

The proposed weighted-test-signal-based (WTS) method has been implemented. In all our experiments, the length of all scan chains is set as 10. A pseudo-random test pattern generator (PRTG) of 24 stages is adopted to generate test patterns for all circuits. The phase shifter is generated exactly according to that in [15]. All experimental results in this paper are collected after 500k clock cycles. All extra faults of the DFT logic are excluded and all methods uses the same PS and PRTG in order to present fair comparison. The same fault simulator is adopted for all methods.

As shown in Table 1, the original area of the circuit (*area (orig.)*), area of the phase shifter (*area (PS)*), area of the weight generator (*area (connect)*), area overhead (AO), fault coverage of the circuit without test point, the number of test points (ntp), and fault coverage after the given number of test points have been inserted (FC(test point)) are given after 500k clock cycles. The area of the weight generator includes the extra gates as shown in Fig. 3. The area overhead in Table 1 includes area overhead of the phase shifter and the extra logic to generate the weighted test signals, where areas of the PRTG and MISR are not included. It is shown in the fourth column in Table 1 that the hardware overhead introduced by the new test generation scheme for the weighted test signals is almost trivial for a ll circuits. Extra area overhead introduced by the proposed method should be much less than that of previous weighted test generators. The area overhead produced by the phase shifter (PS) is presented in the third column as shown in Table 1.

The proposed method obtains very good test effectiveness for most circuits without test point. Circuit s4863 even get complete test effectiveness, while circuits s1269, s1423, s3271 and s5378 obtain close to complete fault coverages. Circuits s3330, s13207.1, s15850, s38417, and s38584 also get up to 97.58%, 98.55%, 95.01%, 97.27%, and 96.33% fault coverages, respectively.

Comparison of the new method with two test schemes with multiple capture cycles MTS [17] and TTS [9] and the conventional *test-per-scan* (STS) test scheme is also presented in Table 1. Implementation

Table 1: Performance evaluation of the proposed method.

circuits	area (orig.)	area (PS)	area (connect)	AO(%)	CPU (second)	no test point (FC)				with test points					
										WTS		MTS[18]		STS	
						WTS	MTS[18]	TTS[10]	STS	ntp	FC(%)	ntp	FC(%)	ntp	FC(%)
s1269	1417	168	9	12.46	0.10	99.87	98.99	99.31	98.99	—	—	—	—	—	—
s1423	1904	192	9	10.56	0.28	99.25	98.95	99.25	98.30	—	—	—	—	—	—
s1512	1834	272	9	15.32	0.22	96.92	96.86	96.28	96.28	5	98.33	5	97.88	5	97.29
s3271	3859	292	9	7.80	1.35	99.95	99.57	99.91	98.25	—	—	—	—	—	—
s3330	4136	412	9	10.18	1.16	97.58	94.33	94.41	91.51	5	99.57	5	98.40	5	97.73
s3384	4619	472	9	10.41	1.62	97.65	97.62	97.87	96.36	5	98.25	5	97.65	5	97.47
s4863	5123	456	9	9.06	1.41	100	99.25	99.29	97.54	—	—	—	—	—	—
s5378	6002	404	9	6.88	2.23	99.30	98.93	98.89	98.18	—	—	—	—	—	—
s9234	10207	320	9	3.22	12.43	91.88	90.70	89.71	88.02	20	93.65	20	93.61	20	92.50
s13207.1	17687	972	9	5.55	48.64	98.55	97.31	98.10	97.31	—	—	—	—	—	—
s15850	19643	564	9	2.92	43.16	95.01	93.86	93.85	93.64	15	97.32	15	96.51	15	96.19
s15850.1	19011	1012	9	5.37	56.86	95.42	94.12	94.01	93.48	15	97.51	15	96.58	15	96.28
s38417	48824	1480	9	3.05	573.0	97.27	97.06	97.26	95.85	15	99.07	15	98.86	15	98.05
s38584	47584	1216	9	2.57	472.2	96.33	95.91	95.88	95.46	13	97.34	13	97.12	13	96.83
b14	21323	432	9	2.07	25.3	92.12	91.49	91.62	89.93	—	—	—	—	—	—
b20	43003	628	9	1.48	161.1	95.41	94.00	94.70	93.28	—	—	—	—	—	—
b21	43811	628	9	1.45	162.4	93.39	93.01	94.26	91.83	—	—	—	—	—	—
b22	63957	628	9	1.25	347.9	94.99	94.37	94.80	93.54	—	—	—	—	—	—
average	—	—	—	—	—	96.72	95.91	96.08	94.88	—	97.63	—	97.08	—	96.54

of the STS test scheme is similar to the WTS scheme except weighted test signals.

The WTS, MTS and TTS test schemes get better fault coverage for all circuits than the STS when no test point is inserted. WTS gets much better results than STS for most circuits. It is shown that WTS outperforms MTS for all circuits. It obtains much better fault coverage than MTS for circuits s9234, s13207.1, b20, s15850, s15850.1, and s3330. Compared with the TTS test scheme, our method gets better fault coverage for all circuits except circuits s3384 and b21. The new method gets a little better results for circuits s3271 and s38417. However, WTS gets much better results for circuits s3330, s9234, s15850, and s15850.1. Comparison of WTS with MTS, and STS is also presented in Table 1 after a number of test points have been inserted. The WTS works better than MTS and STS for all circuits.

Fig. 5 presents fault coverage comparison of four BIST schemes with the number of test cycles from 10k to 500k. Results of circuits s3330, s15850.1, s38584, and b20 are presented. It is shown from the curves that the proposed method consistently gets better fault coverage than all other methods. Fault coverage difference between the WTS and all other ones seems more apparent in earlier phase. Fault coverage of MTS and TTS changes sharply when they turn from the first test session to the second. However, fault coverage increment is not so clear when the MTS and TTS turn from a test session later than the first to the next one. All test schemes change fault coverage quickly at eralier stage. It is should be noted from the curves that the proposed method can get the expected fault coverage much earlier.

6 Conclusions

An effective scan-based BIST method was proposed by assigning different weights to the test signals of the scan chains, which generates weighted test vectors for the pseudo-primary inputs. The proposed method does not need to shift a test vector to the scan chains completely, where capture cycles can be inserted at any time if necessary. The proposed method does not need to insert any extra logic to the functional path or any complicated hardware to generate the weighted test vectors. Neither the number of shift cycles nor the number of capture cycles of a test cycle is fixed using the proposed test scheme. The proposed test scheme has completely jumped out of the frame of the conventional *test-per-scan* test schems. Sufficient experimental results showed that the method can improve the test effectiveness of scan-based BIST greatly and outperform two of the recent methods with multiple capture cycles.

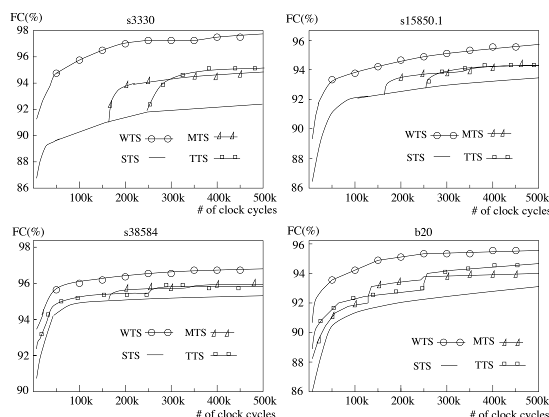

Figure 5: Fault coverage curves of the four BIST schemes.

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