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Design for Cost-Effective Scan Testing By Reconstructing Scan Flip-Flops

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Abstract

A new scan architecture called reconfigured scan forest is proposed for cost-effective scan testing. Multiple scan flip-flops can be grouped based on structural analysis that avoids new untestable faults due to new reconvergent fanouts. The proposed new scan architecture makes all scan flip-flop groups have similar size because of flexibility of the scan flip-flop grouping scheme, where many scan flip-flops become internal scan flip-flops. The size of the exclusive-or trees can be reduced greatly compared with the original scan forest. Therefore, area overhead and routing complexity are reduced greatly. It is shown that test application cost and test power with the proposed scan forest architecture can be reduced to even less than 1% of the conventional full scan design with a single scan chain.

1 Introduction

Scan design makes test generation of the circuit to be that of a combinational one, which can obtain complete fault coverage and make the test application cost prohibitively high. Recently, a lot of new scan testing methods have been proposed to reduce test application cost and test power. Papers [5] inserted extra logic into the circuit to block transition propagation from the scan chain into the combinational part. Most recently, we proposed a new scan architecture called scan forest [9] to reduce test application time and test power, and test data volume greatly. However, the scan forest may cause area and routing complexity problems and produce some aliased faults due to XOR trees. Scan tree has been used to reduce test application time and test power in several recent papers [2,3,9]. Let *#vectors* and *levels* be the number of test vectors and the depth of the scan forest. The test application cost TAT is,

$$TAT = \#vectors \cdot (levels + 1) + levels. \qquad (1)$$

In this paper, we introduce a new scan architecture called reconfigured scan forest to resolve the routing complexity and area overhead problems of the scan forest [9], and avoid the aliased faults due to the XOR trees. The proposed reconfigured scan forest can reduce the size of XOR trees significantly compared with the scan forest [9] and can avoid aliased faults effectively, while it can reduce test power, test application cost, and test data volume significantly.

2 The Reconstructed Scan Forest

The scan forest connects all leaf scan flip-flops to the XOR trees, which can cause routing problem and introduce non-trivial area overhead and produce some new aliased faults. A new scan architecture called reconfigured scan forest is introduced that can resolve the routing problem, reduce area overhead and obtain complete fault coverage.

Fig. 1(a) shows the tree structure of the scan tree constructed in the above section. All leaf nodes should still be connected with the XOR trees. It is known that the XOR gates inserted into the circuit may make the area overhead not trivial. Also, the potential routing complexity may be unacceptable. Connecting all scan flip-flops with the XOR trees may also make fault coverage of the circuit not good enough. A large number of scan flip-flops may fan out from the same scan flip-flop in the scan forest, which can make test power consumption of the same node too large.

The scan tree is reorganized into a new tree as shown in Fig. 1(b). Each scan flip-flop group can be split into multiple subgroups. Scan flip-flops in each subgroup can be driven by a scan flip-flop in the scan flip-flop group that contains their predecessor. Scan flip-flops in the same level should be contained in the same group. It is clear that the number of internal

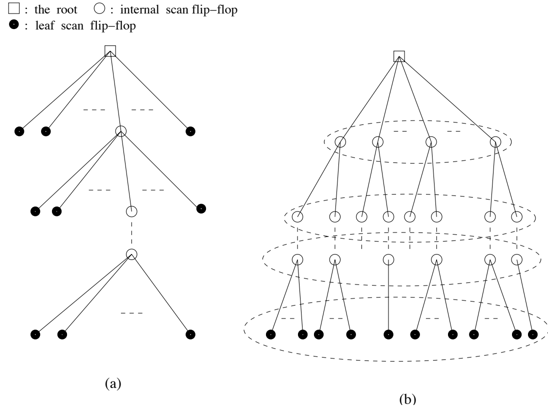

Figure 1: Scan flip-flop group reorganization: (a) The original scan tree, (b) the reorganized scan tree.

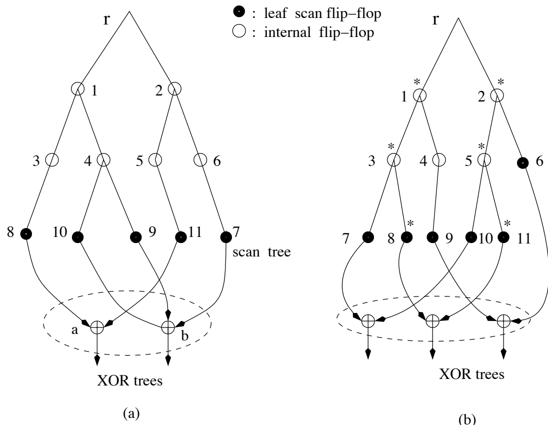

Figure 2: Only the leaf scan flip-flops are not enough.

scan flip-flops has increased greatly. Area overhead and routing overhead can be reduced greatly.

3 XOR Tree Construction to Avoid Aliased Faults

In the original scan forest [9], outputs of the leaf scan flip-flops are randomly selected to connect with the XOR trees. It is clear that this scheme can generate a number of aliased faults. A table $pred()$ can be calculated first where $pred(i, j) = 0$ represents that flip-flops i and j do not have any common predecessor, using which the *cpu* time can be reduced greatly when constructing the XOR trees.

Let us consider the reconfigured scan tree as shown in Fig. 2(a), two XOR gates are constructed. Outputs of scan flip-flops 7, 9, and 10 are connected with the XOR gate b. And outputs of scan flip-flops 8 and 11 are connected with the XOR tree a if flip-flops 8 and 11 do not have any common combinational predecessor. However, it is quite possible for flip-flops 3 and 5 to have the same predecessor v, where fault effects propagated through v can be propagated to both scan flip-flops 3 and 5 simultaneously. It is quite possible for the fault effects to be masked at the output of b. As for any fault effect captured at scan flip-flop 4, it is propagated to 9 and 10 simultaneously. The fault effect must be masked at the the output of the XOR gate b no matter whether 9 and 10 have any common combinational predecessor. Therefore, a lot of aliased faults may occur if only the leaf scan flip-flops are considered when constructing the XOR trees.

As for two leaf scan flip-flops a and b in the same scan tree, there exists a common predecessor v in the scan tree that can be the root. There exists two paths from both leaf scan flip-flops to the node v in the scan forest $(a, v_1, v_2, \ldots, v_i, v)$ and $(b, v_1^{'}, v_2^{'}, \ldots, v_j^{'}, v)$. Generally, it is required that all pairs of flip-flops (a, b), $(v_1, v_1^{'})$, $(v_2, v_2^{'})$, ..., have no common predecessor in the combinational part of the circuit, respectively in order to avoid aliased faults.

It is unnecessary for each group of flip-flops to meet the above condition when constructing the scan tree properly. As shown in Fig. 2(b), both flip-flops 8 and 11 are connected with the XOR gate b. It is necessary to check whether (8,11) and (3,5) have any common predecessors. Let (7,10) and (3,4) not have any common predecessors in the combinational part of the circuit. Consider flip-flops 7 and 10, it is sufficient to check whether 7 and 10 have any common predecessor. As for XOR gate c, we need to consider flip-flop pair (6,9). There should be no combinational predecessor for (6,9) in order to avoid aliased faults. However, flip-flop pair (2,4) do not need to have no common predecessor because any fault effects captured at 2 can also be observed at the output of gate b. Any fault effects captured at flip-flop 2 can also be propagated through path 2-5-11-6.

There may still exist some aliased faults even though the above conditions have been met. Let us consider scan flip-flop 1 in Fig. 3. As for any fault effects propagated to scan flip-flop 1, they can also be propagated to scan flip-flops 7 and 8 simultaneously, which are masked by the XOR gate a as presented in Fig. 3(a). All fault effects propagated to flip-flop 1 are masked in this case. This kind of aliased faults can be avoided as follows: (1) All leaf scan flip-flops connected with the same XOR tree should be in different scan trees if possible; and (2) any pair of leaf scan flip-

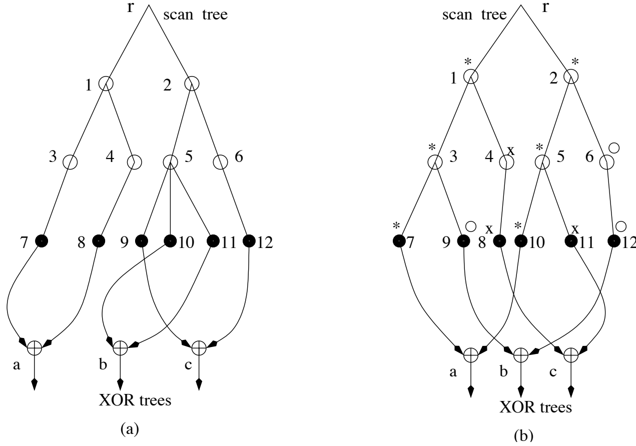

Figure 3: Avoid aliased faults.

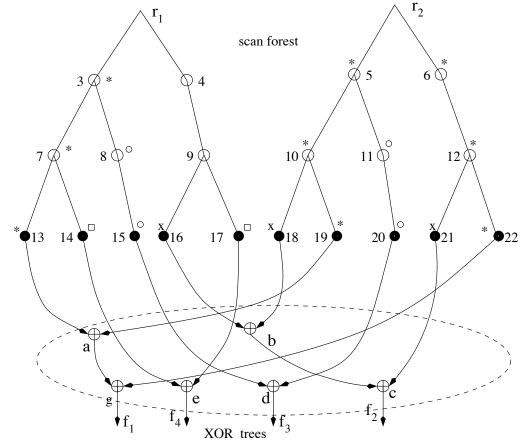

Figure 4: XOR tree construction in multiple scan trees.

flops connected with the same XOR tree should be in different subtrees that are driven by the root directly if two leaf scan flip-flops in the same scan tree must be connected with the same XOR tree.

The known compatible scan path information can be used to construct XOR trees. Let scan flip-flop pairs (7,10), (3,5), and (1,2) not have any common combinational predecessor as shown in Fig. 3(b), connection of scan flip-flops 7 and 10 with the same XOR gate generates no aliased fault. Let scan paths (1,3,7) and (2,5,6) be compatible. It is better to reconstruct the XOR tree and reconfigured scan tree as shown in Fig. 3, where scan flip-flop 9 is connected with flip-flop 7 instead of 5. As shown in Fig. 3(b), it is necessary for the flip-flop pair (8,11) to have no common combinational predecessor in order to connect scan flip-flops 8 and 11 with the same XOR gate. It is unnecessary to check whether scan flip-flops 4 and 5 to have no common combinational predecessor because fault effects captured at scan flip-flop 5 can also be observed at a. As for the XOR tree c, it is enough if scan flip-flops 9 and 12 have no common combinational predecessor without checking scan flip-flop pair (3,6).

More attention should be paid to XOR tree construction for multiple scan trees. As shown in Fig. 4, three leaf scan flip-flops are connected to the same XOR tree f_1. Each pair of scan flop-flops in the groups (13, 19, 22), (7, 10, 12), and (3,5,6) do not have any common predecessor in the combinational part of the circuit. All three compatible scan paths should be very helpful to further XOR tree construction. Leaf scan flip-flops 14 and 17 can be connected with the same XOR tree if scan flip-flops 14 and 17 do not have any common combinational predecessor. It is unnecessary to check whether scan flip-flop groups (7, 9) and (3,4) have any common combinational predecessors because fault effects of their common predecessors can be propagated along the proven compatible path 3-7-13-f_1. Similarly, three leaf scan flip-flops 16, 18, and 21 can be connected to the same XOR tree f_2 only if any pair of scan flip-flops 16, 18, and 21 do not have any common combinational predecessor. It is unnecessary to check whether any two of the scan flip-flops in the groups (9, 10, 12) and (4, 5, 6) have a common combinational predecessor. The situation for the XOR tree f_3 is similar. It is necessary to check whether each of the scan flip-flop groups (15, 20) and (8, 11) have any common combinational predecessors.

4 Experimental Results

The proposed reconfigured scan architecture has been implemented, and the ATALANTA test generator is adopted to generate tests [6]. After the XOR trees have been added to the circuit, the HOPE fault simulator [6] is utilized to do fault simulation using the test vectors on the reconfigured scan forest designed circuit. It is found that the number of leaf scan flip-flops is reduced greatly after using the reconfigured scan architecture.

Performance of the reconfigured scan forest is presented in Table 1. TA, TE, vec, #red, *naf*, AO, and *nef* represent test application cost reduction ratio, test energy reduction ratio corresponding to full scan design with a single scan chain, the number of test vectors, the number of redundant faults, the number of aliased faults, area overhead, and the number of redundant

Table 1: Performance Comparison with the *scanforest* [9]

circuits	full scan			scan forest [9]								reconfigured scan forest							
	FC(%)	#red	vec	#red	*naf*	*nef*	AO (%)	vec	TA(%)	TP(%)	PTP(%)	#red	*naf*	*nef*	vec	AO(%)	TA(%)	TP(%)	PTP(%)
s13207	98.46	151	466	244	53	40	11.40	443	1.13	1.13	1.21	151	0	0	458	4.17	1.17	1.19	1.19
s15850	96.68	389	436	484	60	35	9.18	434	2.31	2.28	2.45	389	0	0	413	3.38	2.30	2.30	2.49
s35932	89.81	3984	63	4852	0	868	16.17	26	0.05	0.10	0.11	3984	0	0	43	16.17	0.08	0.13	0.15
s38417	99.47	165	899	1640	1376	99	14.19	574	0.20	0.28	0.31	165	0	0	833	6.98	0.23	0.22	0.25
s38584	95.85	1506	651	2131	619	6	10.94	649	0.95	0.92	0.96	1506	0	0	653	3.47	0.96	0.98	0.97
b17	97.01	2293	2301	2857	570	32	8.98	2170	0.67	0.63	0.67	2207	0	0	2321	3.22	0.71	0.66	0.71
b18	96.11	7334	2944	50080	42854	0	10.13	2879	0.33	0.43	0.42	7220	0	0	2879	3.53	0.33	0.54	0.52

Table 2: Performance Comparison with the Previous Methods

circuits	reconstructed scan forest			BO [1]		FDR [4]
	TA(%)	TE (%)	TDR(%)	TA(%)	TDR(%)	TDR(%)
s13207	1.06	1.13	27.80	16.20	13.77	12.33
s15850	1.48	2.31	16.36	21.54	18.29	28.05
s35932	0.08	0.13	0.43	17.60	16.34	—
s38417	0.23	0.22	4.88	20.51	19.07	34.65
s38584	0.61	0.95	6.58	16.02	14.48	35.33

faults in the DFT logic.

The proposed reconfigured scan forest is compared with the scan forest [9] as presented in Table 2. As for the original scan forest, scan flip-flop groups are not regulated and the XOR trees are constructed randomly. It is found from the experiments that the proposed XOR tree construction scheme incurs no aliased faults and much less area overhead for all circuits.

The proposed method is compared with two recent test compression methods [1] (BO) and [4] (FDR) on test application cost and test data volume reduction ratios. The advantage of the proposed method over the previous ones is very apparent.

5 Conclusions

A new scan architecture called the reconfigured scan forest was proposed for low test application cost and test power consumption. The reconfigured scan forest can have much more internal scan flip-flops that do not need to be connected to the XOR trees to observe test responses of them. Therefore, the area overhead and routing complexity of the original scan forest can be reduced greatly. A new procedure was proposed to construct the reconfigured scan forest and the XOR trees concurrently, which avoids aliased faults effectively. Experimental results showed that the proposed reconfigured scan forest outperforms the recent methods on test application cost, test power and test data volume.

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