Electrical Behavior of GOS Fault affected Domino Logic Cell

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Abstract: *Gate-Oxide Shorts (GOS) have an increasing impact on the integrated circuit production yield due to the reduction of the related dimensions. The detection of GOS is a challenging issue in the field of testing. This paper presents a detailed study of the impact of a GOS fault affecting a Domino logic circuit. Indeed, Domino logic specific clocked operating principle induces a different behavior from standard full CMOS cells under the effect of a GOS, which can enable GOS detection. Finally, some clues to enhance GOS detection in Domino cells are proposed.*

I. Introduction

Testing is a key factor to guarantying Integrated Circuits (IC) proper operation. It should ensure the correct function of the device as well as the targeted performances in terms of delay and current consumption. Defects can affect the function and/or the performances of the circuit. In order to detect the potential failures of the IC, it is necessary to study the behavior of the circuit affected by a defect, and define a model of the defect impact. The influence of a defect on an IC may depend on the IC nature. In particular, the behavior of Domino logic cells affected by a defect can be different from standard full CMOS cells affected by a similar defect. It is thus necessary to find out a dedicated fault model for each type of IC. In this paper, we present an electrical study of a Domino logic cell affected by a Gate-Oxide Short (GOS) and investigate the achievable detection of GOS in Domino cells.

Unlike standard full CMOS gates, which include both NMOS and PMOS complementary functions, Domino gates [1] are implemented with only one type of function (NMOS or PMOS), which is inserted between a precharge PMOS transistor and an evaluation NMOS transistor (see Fig. 1, example with NMOS function). Precharge and evaluation transistors are connected to a clock signal ϕ, leading the operation of the Domino gate as a succession of precharge and evaluation phase. In order to enable cascading of gates, the dynamic node is connected to a static inverter. Therefore, only non-inverting functions can be implemented with Domino logic. The operation principle of Domino logic gates is developed in section II.

Open defects in Domino logic cells have been studied and some detection methods have been proposed [2, 3]. Resistive short influence on Domino cells and detection through Very Low Voltage (VLV) testing have been presented in [4]. However, this paper deals with gate-to-drain and gate-to-source shorts, and gate-to-channel shorts are not considered. GOS and more precisely gate-to-channel shorts are the focus of this paper.

The effects of a GOS on the behavior of a MOS transistor have been studied in detail, and some models have been proposed [5, 6, 7]. The impact of GOS at the transistor level consists in voltage level and time performance degradations as well as quiescent current increase. These effects are detailed in section III.

A detailed analysis of the behavior of a full CMOS logic gate with a GOS and its possible detection have recently been proposed [10, 11]. Nevertheless, the results obtained in case of a full CMOS logic gate cannot be transferred to Domino logic. The detailed study of the behavior of a Domino logic cell under the influence of a GOS is then shown in section IV. Finally, section V gives some concluding remarks.

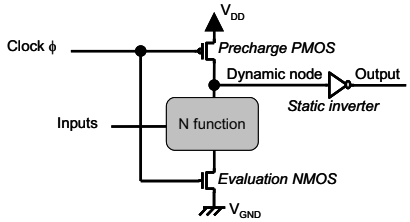

Figure 1: Domino logic gate (N type)

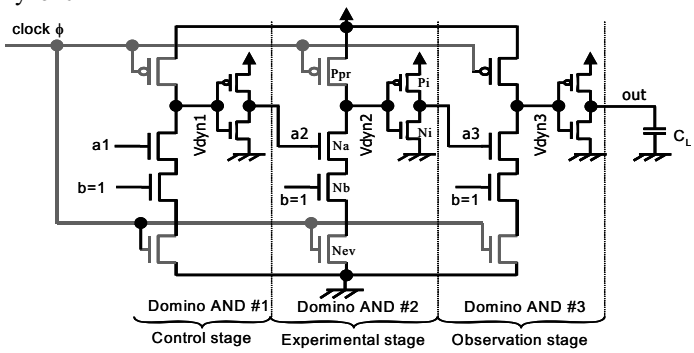

Figure 2: Domino logic structure of study (chain of 3 AND cells)

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II. Domino Logic Cell

In order to investigate the impact of a Gate-Oxide Short on the behavior of a Domino logic cell, we consider the elementary circuit presented in Fig. 2. We consider a chain of three Domino AND gates. Indeed, this structure is composed of a small number of transistors per gate, so the exhaustive electrical study is achievable. Note that extension of the analysis to Domino NOR gates is straightforward.

The first Domino AND cell has a role of control stage. It should be considered as a buffer for the following stage. The second Domino AND cell constitutes the experimental stage in which the GOS will be injected. Finally, the third cell stands as an observation stage. This last cell enables us to observe whether the local degradations of the voltage levels, induced by the defect, will spread downstream and result in a faulty behavior of the structure at the primary output. The primary output has been identified as *out* in Fig. 2. The primary inputs are *a1* and *b*. The load capacitance C_L has been designed to be equivalent to one cell input capacitance. The clock signal ϕ is buffered by a small sized static inverter. The structure has been designed in 0.18µm technology (model card from ST Microelectronics). The operating voltage is 1.8V, and the nominal threshold voltage is 0.565V.

Each Domino AND cell is composed of 6 transistors: two signal NMOS (named *Na* and *Nb* in the central gate, Fig. 2), one precharge PMOS (*Ppr*) and one evaluation NMOS (*Nev*), and two complementary transistors forming a static inverter (*Ni* and *Pi*). The length of the channel is the same for every transistor, and the width ratios are the standard ones for Domino logic (*Ni*=1, *Pi*=4, *Ppr*=2, *Na*=*Nb*=*Nev*=6). All the transistors that are not part of the static inverter (*Ppr*, *Na*, *Nb* and *Nev*) constitute a dynamic NAND gate. The association of a dynamic gate with a static inverter results in a Domino cell. The node between the dynamic gate and the static inverter is usually called the dynamic node. Dynamic nodes of the first, second and third Domino cells of the structure are respectively designated by *dyn1*, *dyn2* and *dyn3*. Similarly, the first signal inputs of the successive gates are respectively indicated by *a1*, *a2* and *a3*, *a2* being also the output of the first Domino stage and *a3* corresponding to the output of the central AND gate. The second signal input, named *b*, is common to all the cells, and is fixed to the high voltage level. Consequently, the result of the AND functions is led by the value of the first signal input *a1*.

In the case of a healthy structure, i.e. the circuit is not affected by any defect, the circuit of study behaves as follows. When ϕ=0, the precharge PMOS are active whereas the evaluation NMOS are locked. Therefore, whatever the primary inputs are, all dynamic nodes are charged to the high level. This constitutes the precharge phase of operation. Thanks to the static inverters, the secondary inputs of gates #2 and #3, respectively *a2* and *a3*, are set to the low level. When ϕ=1, the evaluation phase begins. The precharge PMOS are locked while the evaluation NMOS are active. As *a2* and *a3* are at the low level, the gates #2 and #3 and locked at first. If the primary input *a1* is at the low level, the first Domino AND keeps the same state as previously. Indeed, the dynamic node *dyn1* cannot be discharged, so *a2* stays at the low level and gate #2 remains locked, and so on. On the contrary, if *a1* is at the high level, the dynamic node *dyn1* is discharged through the active NMOS of the dynamic gate, resulting in a commutation of *a2* to the high level. Consequently, the second Domino cell evaluates its function, discharges its dynamic node, and so on and so forth, producing a chain effect similar to a falling row of dominos.

The time diagram of the simulated healthy structure of study is shown in Fig. 3. The nominal operating frequency is 10MHz During the precharge phase, whatever *a1*, the dynamic nodes are set at the high level and the secondary inputs *a2* and *a3* as well as the primary output out are set to the low level. When *a1*=0 (left half of the diagram), all the Domino gates are locked. The dynamic nodes remain at the high level while *a2*, *a3* and *out* stay at the low level during the evaluation phase. The small overshoot of the dynamic node voltage levels is due to capacitive couplings and can be considered as irrelevant in the operation. When *a1*=1 (right half of the diagram), all the nodes switch during evaluation, and switch back at precharge.

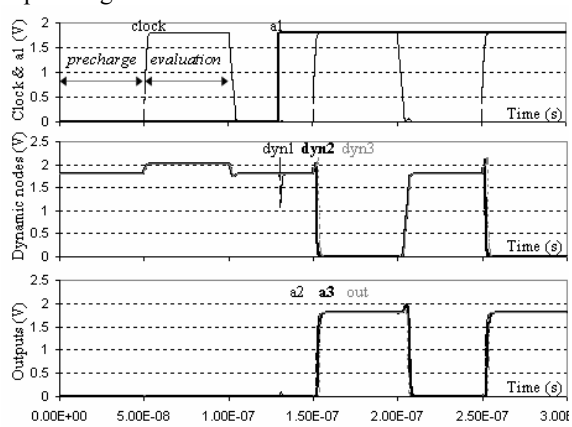

Figure 3: Timing diagrams of the healthy Domino structure at 10MHz

It should be pointed out that complex Domino gates often include keepers and internal prechargers. Keepers aim at avoiding floating dynamic nodes, preventing from leakage and noise problems. Internal prechargers remove charge sharing problems. For the sake of clarity, we have not taken these elements into account in this study.

But, extension of our analysis to the domino cells with keeper is straightforward.

III. GOS in standard CMOS

As previously said, Gate-Oxide Shorts consist in a failure of the isolation in the oxide layer resulting in a resistive path between the gate and substrate of MOS transistors. Consequently, a current can flow between the gate and the substrate (Fig. 4). The classical equations ruling the operation of a healthy MOS being based on the oxide layer isolation, these equations should therefore not be considered in the case of a transistor affected by a GOS.

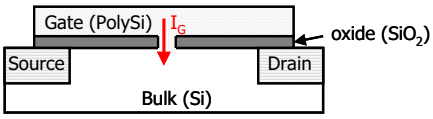

Figure 4: Side view of a MOS affected by a GOS

The behavior of a MOS transistor affected by an oxide isolation failure has been widely investigated by many researchers [5-9]. At the transistor level, the impact of a GOS on the MOS operation induces a modification of the transistor characteristics. The typical alteration of the drain current ID and gate current IG characteristics are illustrated in Fig. 5-a and Fig. 5-b respectively in case of a NMOS. One should note that the defect has no impact on the characteristics when the transistor is off.

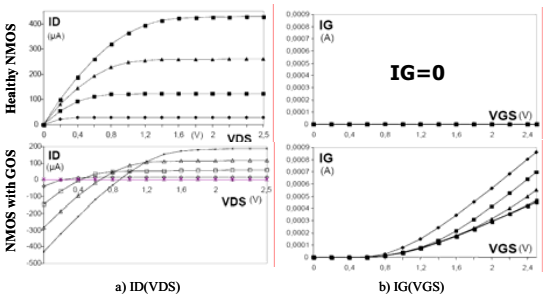

Figure 5: Typical characteristics of Drain (a) and Gate (b) currents for a healthy NMOS (top) and a NMOS affected by a GOS (bottom)

The classical models of defective transistors affected by a GOS are based on the division of the transistor into an array of smaller transistors as illustrated in figure 6. A resistance connecting the common gate to one of the array nodes represents the defect. Note that these models have been extensively studied and validated in [8] and we just reuse these published models.

The resistance can be given any desired value. The position of the defect can be easily adjusted by moving the connection node in the array. Finally, the size of the defect can be increased by connecting together several neighboring nodes of the transistor array. Therefore, every unpredictable parameter of the GOS defect can be taken into account in the model.

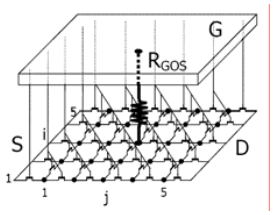

Figure 6: Scheme of the lumped MOS model

IV. GOS in dynamic CMOS

We have studied the behavior of the Domino logic structure presented in section II (Fig. 2) for Gate-Oxide Shorts affecting each transistor of the central cell. We assume single fault, in other words we inject only one GOS at once. For each case, the unpredictable parameters of the defect have been considered. The results of the behavioral study are presented in this section, and some hints are proposed in the view of GOS detection.

1. GOS in the signal transistor

The first MOS in which we inject a GOS defect is the signal NMOS transistor *Na*. In a first place, we consider a small GOS defect of size one node in the lumped MOS model, located in the center of the array, with a very low resistance of 1Ω. As mentioned in section III, the defect has no impact on the behavior of the MOS if the transistor is off. Then, the effect of the GOS on the behavior of the transistor *Na* (and consequently on the behavior of the Domino cell) should be observed when the gate of *Na* is at the high logic level. It implies that the primary input *a1* should be at the high level. In addition, the observation should be made during evaluation phase. Indeed, during evaluation phase, the evaluation NMOS *Nev* is on, which enables the short current *Ishort* to flow, from the PMOS of the upstream static inverter through the defective gate of *Na* to the ground (as shown in Fig. 7).

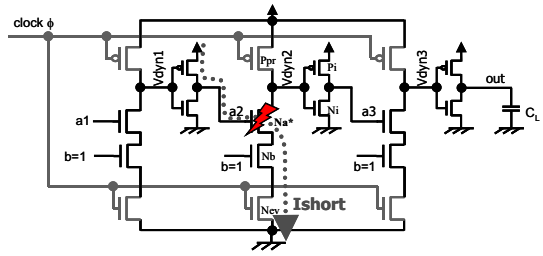

Figure 7: Conductive path of the short current Ishort (GOS in signal transistor Na)

On the contrary, during precharge phase, *Nev* is off, opening the conductive path between the power supply and the ground.

The time diagrams of the voltage levels involved in the signal path of the Domino structure are illustrated in Fig. 8 at nominal operation frequency (10MHz). As expected, the injected GOS has no impact on the Domino cell behavior during precharge phase or when the primary input *a1* is at

the low level. On the contrary, some degradations of the voltage levels of nodes *a2* and *dyn2* can be observed during evaluation when *a1*=1. These two nodes are located directly upstream and downstream, respectively, of the affected transistor. The secondary input *a2*, corresponding to the gate of the faulty transistor, reaches only 63% of its nominal voltage. The dynamic node *dyn2*, connected to the drain of *Na*, which should be at the low level in this configuration, reaches 26% of the voltage range. Although the voltage alterations are severe, they are not sufficient to induce a false logic state. Therefore, the defect is not detectable via a Boolean test.

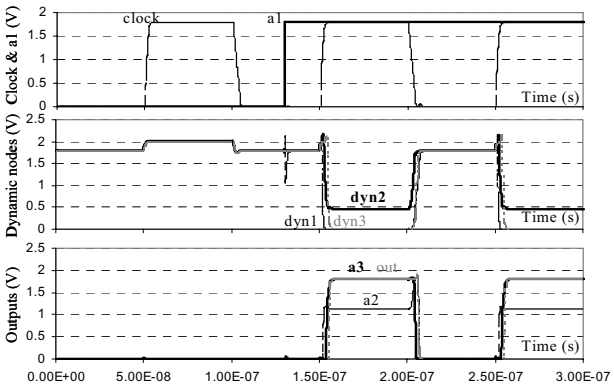

Figure 8: Time diagrams of the voltage levels, GOS in Na (1 node centered, 1Ω, 10MHz)

We now take into account the unpredictable parameters of the GOS defect injected in the signal transistor *Na*. In a first place, we investigate the influence of the GOS resistance. The values of all the voltage levels measured when the defect is activated are presented in Fig. 9 for GOS resistance varying from 0 to 30kΩ.

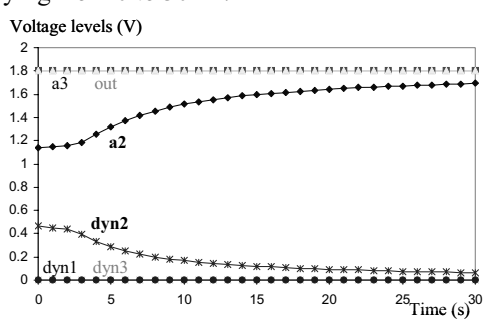

Figure 9: Influence of the GOS resistance

The defect size is still 1 node, located in the center of the lumped transistor model array, and the operation frequency is nominal (10MHz). Simulations show that the nodes *a2* and *dyn2* exhibit the only voltage levels that are significantly affected by the defect. When the resistance of the defect increases, the value of these node voltage levels get closer to their nominal values. Whatever the resistance, the presence of the GOS defect never induces a false logic state. Therefore it cannot be detected via Boolean test.

The position of the GOS along the gate has not a great influence in this case, as shown in Fig. 10. This figure presents the evolution of the voltage levels of nodes *a2* (a) and *dyn2* (b) along the value of the GOS resistance (ranging from 0 to 30kΩ) for the five locations along the gate in the array. The simulation and measurement conditions are the same as previously. Concerning the position, "D" indicates a location of the defect very close to the drain, while "S" corresponds to a position neighboring the source of the faulty transistor. We can observe that the impact of the GOS on the voltage level *a2* (gate voltage of the faulty transistor) is more significant when the defect is located close to the source. In this case, *a2* reaches only 58% of its nominal voltage level. On the contrary, the voltage level *dyn2* is more affected when the GOS is closer to the drain (up to 30% of the voltage range). These observations match the results obtained in the context of standard CMOS cells [10]. Nevertheless, the defect cannot be detected via Boolean test.

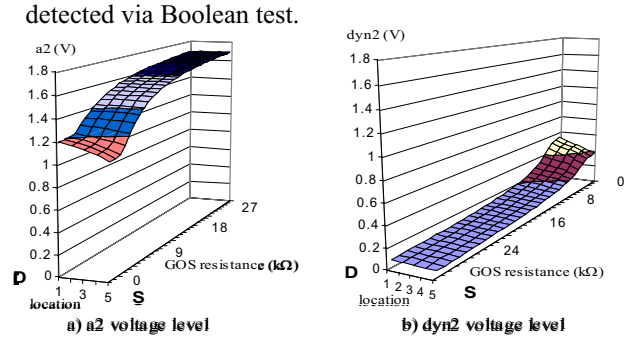

Figure 10: Influence of the GOS position on voltage levels a2 (a) and dyn2 (b)

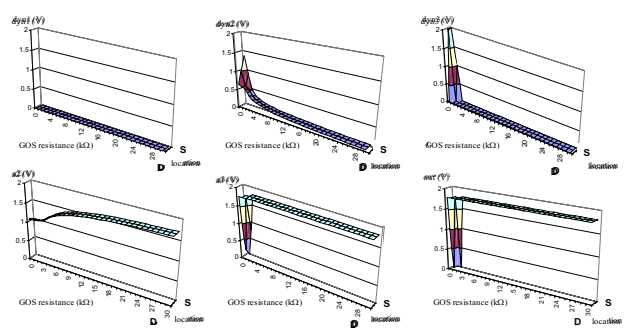

Figure 11: Influence of a 9-node GOS in Na on voltage levels

Finally, we take into account the size of the defect. We consider defect sizes of 9 nodes of the lumped model array and of 21 nodes. In case of a 9-node defect, the GOS can have three different locations along the gate. In case of a 21-node GOS, only one position is possible. The impact of a 9-node GOS on the voltage levels of all nodes in the structure along the resistance and position in the channel are presented in Fig. 11. When the resistance of the defect is very low (inferior or equal to 1kΩ) and the defect is located in the center of the gate or close to the source, a false logic stat

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can be observed on all nodes downstream the defective transistor (*dyn2*, *a3*, *dyn3* and *out*). Then, the detection of the defect is possible on the primary output via a Boolean test. But the range of detection is extremely narrow.

We obtain similar results in case of a 21-node defect (results are not shown in this paper).

To summarize, a GOS defect in the signal transistor of a Domino cell can be detected via Boolean test only when the short resistance is lower than 1kΩ, the defect size is at least 40% of the gate surface and the defect is not close to the drain.

2. GOS in the evaluation transistor

We now investigate the effect of a GOS affecting the evaluation NMOS transistor *Nev* of the central Domino cell. In this case, the gate of the faulty transistor *Nev* is connected to the clock signal ϕ. Therefore the defect is activated during every evaluation phase (ϕ=1). In this configuration, the short current flows from the power supply via the PMOS transistor of the clock buffer, through the faulty gate of *Nev*, to the ground. The voltage levels of the clock signal ϕ as well as the internal node between the transistors *Nev* and *Nb* are affected by the defect. As we assume the primary input *b* to be at the high voltage level, the transistor *Nb* is on and consequently the voltage level of the internal node between *Nb* and *Na* is also influenced. Whatever the unpredictable parameters, the voltage levels of the nodes upstream from the faulty transistor (*dyn1* and *a2*) are not affected by the defect.

In case the primary input *a1* is at the low voltage level, and consequently so is *a2*, the signal transistor *Na* is off. Therefore, the effect of the GOS is not spread downstream. It should be pointed out that the small overshoot the the dynamic node voltage levels mentioned in section II are partially discharged toward the nominal high voltage level 1.8V. Indeed, the voltage level of the clock signal is affected, therefore the precharge transistor compensates for the capacitive couplings. Whatever the GOS unpredictable parameters, no impact of the defect is noticeable on the signal node voltage levels.

In case the primary input *a1* is at the high voltage level, the dynamic node dyn2 is not fully discharged after the precharge phase as far as *Nev* is defective. The behavior of the Domino structure is very similar to the one observed when the GOS affects the signal transistor *Na*, except that the node *a2* is not affected. Thus, results are not shown here. The same conclusions as in section IV.1 can be derived.

3. GOS in the precharge transistor

Symmetrically, we study the impact of a GOS located in the precharge PMOS transistor *Ppr* of the central Domino gate. Under this condition, the defect is active during precharge phase, in other words when the clock signal ϕ connected to the gate of the faulty PMOS is at the low level. The nominal level of the dynamic nodes is then the high level. The short current flows from the power supply through the defective gate of *Ppr* to the ground via the NMOS of the clock buffer. The influence of the defect upon the voltage levels downstream depends on the logic level of the primary input *a1*.

When *a1*=0, the signal transistor *Na* is off. The voltage level of the dynamic node *dyn2* is directly affected by the leakage through the faulty *Ppr*. But whatever the unpredictable parameters, the degradation of the voltage level of *dyn2* is never severe enough to have an impact on the nodes downstream. Indeed, the minimal value of *dyn2* is still 58% of its nominal value (obtained for a 9-node defect located close t the drain). A GOS affecting the precharge transistor could therefore not be detected by Boolean test in these conditions.

When *a1*=1, the signal transistor *Na* is on. As we assume *b*=1, *Nb* is also on. Moreover, the impact on the defect in *Ppr* upon the voltage level of the clock signal ϕ prevents *Nev* from being completely off. As a result, a conductive path between the power supply and the ground through the dynamic gate appears. Consequently, the degradation of *dyn2* voltage level is more severe than previously. In addition, the degradation of the clock level also impacts the control and observation Domino cells. All the dynamic gates in the structure exhibit a short path, resulting in a degradation of the logic levels of all the dynamic nodes.

A defect sized 1 node does not induce any of the static inverters to commute. The voltage levels of *dyn1* and *dyn3* are defined only by the level of ϕ. The clock signal is connected to the gate of the faulty PMOS, so the worst deviation should be obtained when the defect is close to the source. Indeed, we obtain the minimal value of *dyn1* and *dyn3*, 87% of the nominal value, in this case. On the contrary, *dyn2* is also directly influenced as the drain of the faulty transistor. The minimal value of *dyn2*, 66% of the nominal precharge level, appears when the defect is close to the drain.

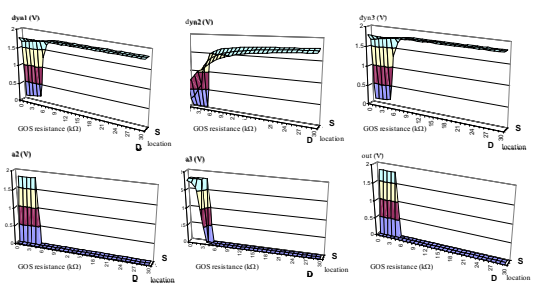

Figure 12: Influence of a 9-node GOS in Ppr on voltage levels

Bigger sized GOS can induce Boolean errors as shown in Fig. 12 in case of a 9-node defect. If the test is carried out on the primary output *out*, the

defect can be detected only if it is located close to the source and if its resistance is inferior to 5kΩ. The internal nodes *dyn1*, *a2* and *dyn3* exhibit the same sensitivity to the GOS impact. The closest nodes downstream the defect, *dyn2* and *a3*, are more affected and commute to a wrong state also when a defect of resistance lower than 4 kΩ affects the center of the gate. Similar results can be observed in case of a 21-node sized defect.

It should be pointed out that we can observe a degradation of the voltage level on node *dyn2* during the evaluation phase when *a1*=0. Indeed, although the defective transistor *Ppr* should be off (ϕ=1), the GOS affects the upstream voltage level. Consequently, the transistor is partially on and a voltage drop appears between power supply and node *dyn2*. Nevertheless, the voltage level never drops lower than 60% of the voltage range. Consequently, the degradation is not spread downstream and the defect cannot be detected via Boolean test.

To summarize, a GOS in a precharge transistor can be detected only during precharge phase when the primary input is at the high level. Even under these conditions, the achievable detection range is still very narrow.

4. GOS in the PMOS of the static inverter

To activate the GOS when the defect affects the PMOS of the central static inverter *Pi*, the voltage level at the gate of the transistor should be at the low level. In other words, the effects of the fault can be observed during evaluation phase when *a1*=1 in order to discharge the dynamic node *dyn2*. In this case, the short current flows from the power supply, through the gate of *Pi*, via *Na*, *Nb* and *Nev* which are all on, to the ground. Consequently, the dynamic node *dyn2* is not properly discharged. The output *a3* of the static inverter is more sensitive to the degradation of *dyn2* than previously as far as the inverter transfer function is affected by the GOS.

For a 1-node sized defect, the maximal voltage level of *dyn2* reaches 34% of the voltage range for a null resistance when the defect is close to the source. The most significant decrease of *a3* to 66% of its nominal value happens for a null resistance when the defect is close to the drain. The other nodes are not affected. In any case, a 1-node sized defect in *Pi* is not detectable by a Boolean test.

When the size of the defect is superior, defect resistances lower than 1kΩ can lead to a false logic state. The detailed observations are very similar to the ones made in case of a GOS affecting *Na*.

5. GOS in the NMOS of the static inverter

A GOS in the NMOS of the central static inverter *Ni* is activated when the nominal value of the dynamic node *dyn2*, connected to the gate of the faulty transistor, is at the high logic level. This condition is fulfilled both during precharge phase whatever the primary input and during evaluation phase when *a1*=0. The behavior of the Domino structure is different depending on the operational conditions, thus we will consider each case separately.

During precharge phase, the short current flows from the power supply, via the precharge transistor *Ppr*, through the defective gate of *Ni*, to the ground. The voltage levels of the nodes *dyn2* and *a3*, connected respectively to the gate and drain of the defective transistor, are significantly affected. A GOS sized 9 nodes or more induces a false logic state of *a3* if its resistance is inferior to 5kΩ whatever its location along the gate. Nevertheless, the defect has no impact at all upon the voltage levels of the nodes downstream during the precharge, as far as the precharge of node *dyn3* neither depends on *dyn2* nor on *a3*.

Notwithstanding, the defect can be detected under these conditions (size 9 nodes or more and resistance lower than 5 kΩ) during evaluation with *a1*=0. Indeed, the Domino structure behaves as shown in Fig. 13 in case of a 9-node GOS with a null resistance located close to the drain. The dynamic node *dyn1* is normally charged during precharge (a), and suffers no leakage during evaluation. Then, *a2* stands at the nominal low level during the whole clock cycle (b). On the contrary, *dyn2* level of precharge is severely affected by the defect (c). Moreover, the leakage through the defective gate leads to an additional discharge of the dynamic node *dyn2*. Indeed, during evaluation (ϕ=1) when *a1*=*a2*=0, both *Ppr* and *Na* are off, leading to a floating node *dyn2*. This high impedance state of the dynamic node is particularly interesting and additional details are given hereafter. The degradation of *dyn2* voltage level results in a wrong logic state of *a3* both during precharge and during evaluation (d). As mentioned in the previous paragraph, the influence of the wrong state during precharge has no effect on the following voltage levels.

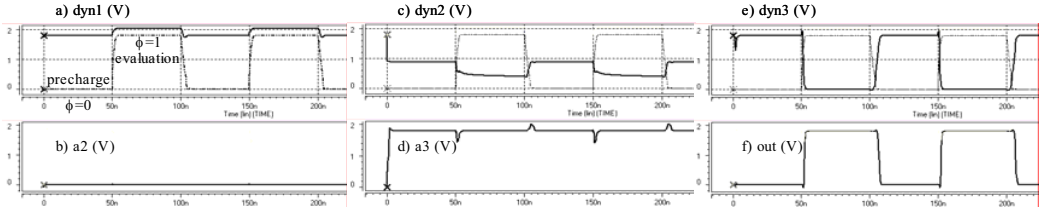

Figure 13: Time diagrams for a 9-node GOS close to the drain in Ni with a1=0 (10MHz)

On the contrary, during evaluation, the error is spread downstream. Indeed, *a3* being at the high level, the signal transistor of the observation cell is on and the dynamic node *dyn3* is fully discharged (e), resulting in a high level on *out* (f) while the nominal level is low (*a1*=0).

The discharge of high impedance node *dyn2* during evaluation depends on the unpredictable parameters. The time constant of the discharge decreases with the resistance of the defect or when the size of the defect increases. The location of the defect along the gate does not influence significantly the discharge time constant. The voltage level obtained at the end of the evaluation phase has been measured for all nodes varying the unpredictable parameters at nominal frequency 10MHz. Results in case of a 1-node defect are shown in Fig. 14. The voltage levels of nodes *dyn1* and *a2* are not affected by the defect and are thus not illustrated hereafter. A false Boolean state on the primary output *out* can be observed for defect resistances up to 24kΩ. In case of a bigger defect, the resistance limit for the detection of a wrong logic state on *out* is very similar (25kΩ).

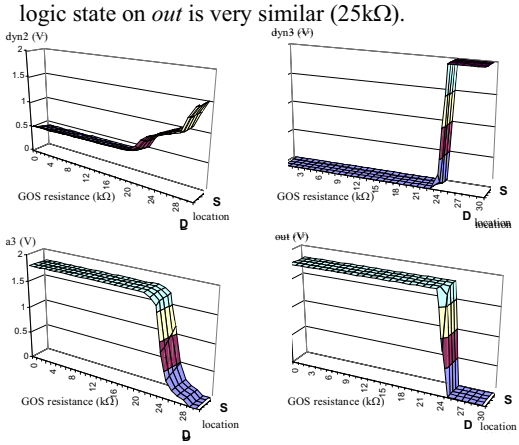

Figure 14: Influence of a 1-node GOS in Ni (10MHz)

When the resistance is superior to the detection limit, the discharge time constant prevents the voltage level from decreasing significantly during the evaluation phase. In a test view, we can then consider decreasing the frequency in order to enlarge the resistance detection range. Indeed, with a reduced frequency, the evaluation phase becomes longer and the charge transfer has more chances to be fully achieved. We perform the same measures as previously with a frequency 10 times lower (1MHz). As expected, the resistance detection is extended up to 7MΩ for a defect as small as 4% of the gate (1 node). We can therefore consider that a GOS located in the NMOS transistor of a static inverter in a Domino cell can be detected via a Boolean test whatever the unpredictable parameters if the test frequency is set to one order of magnitude below the nominal frequency. Obviously, this solution increases drastically the test time and the test engineers should consider the whole advantages and drawbacks.

V. Conclusion

We have carried out a detailed electrical study of an elementary Domino logic circuit affected by a Gate-Oxide Short. We expected beforehand that the clocked operation principle combined to the reduced noise margins of Domino circuits would lead to better possible detection via Boolean test than obtained in standard CMOS cells. Nevertheless, it has been shown in this study that GOS is a defect which detection remains particularly difficult to achieve. The achievable resistance detection ranges are globally comparable to the ones obtained for standard CMOS. One interesting case, when the defect affects the NMOS of the static inverter, leads to a high impedance state that can be detected whatever the defect parameters. Extension to the case of Domino cells with keepers is straightforward.

We will investigate in future work the possibility of GOS detection by quiescent current test (I_{DDQ}) and delay faults.

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