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A New Test Generation Model for Broadside Transition Testing of Partial Scan Circuits

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***Abstract*— This paper proposes a new test generation model for broadside transition testing of partial scan circuits. In the proposed scheme, given a partial scan circuit whose kernel circuit is acyclic, the kernel circuit is transformed into some combinational circuits which are called broadside test generation models. These circuits are constructed by using a time-expansion model of the kernel circuit. All the broadside transition tests are generated by performing constrained stuck-at test generation on the transformed circuits. This means that, without developing a special test generation tool, existing combinational stuck-at test generation tools can be used to generate broadside transition tests for partial scan circuits. Experimental results show that the proposed scheme can reduce area overhead compared with the fully enhanced scan and full scan methods, and can generate broadside transition tests in reasonable test generation time.**

I. Introduction

Fully enhanced scan design [1] is known as a straightforward design for testability (DFT) method for delay testing. This method can drastically reduce test generation complexity of a given circuit by replacing all the flip-flops (FFs) with enhanced scan FFs (ESFFs) which can store any two consecutive vectors. However, due to the considerable penalties of area and delay incurred by ESFFs, its use is limited. For delay faults as well as stuck-at faults, full scan design is widely accepted by industry as an effective DFT method. In delay testing, unlike in stuck-at testing, an additional consideration must be taken into account. That is, two consecutive vectors (two-pattern tests) are needed to detect delay faults, and those vectors have to be applied by using scan flip-flops (SFFs) which can store any one vector. The *skewed-load technique* [2] and *broadside technique* [3] have been proposed as techniques to apply two-pattern tests to full scan circuits. In both of the techniques, the first vectors of two-pattern tests can freely be set to the SFFs through the scan chain. The second vectors are derived by shift operation in the skewed-load technique. In contrast, the broadside technique creates the second vectors by normal operation. In terms of feasibility, the broadside technique is more desirable than the skewed-load technique. This is because, in skewed-load testing, the scan signal is operated at the rated speed and it forces the scan chain to be designed judiciously. There are several broadside test generation methods for full scan circuits [4], [5], [6], [7], [8], [9].

Partial scan design is an alternative to full scan design to reduce the penalties of area and delay. Although many researchers have considered partial scan design for stuck-at faults from various aspects, there are few works for delay faults in partial scan circuits. In [10], a transition test generation method for partial scan circuits has been proposed. This method is based on skewed-load testing. As mentioned previously, since skewed-load testing has some undesirable properties, a test generation method based on broadside testing is also needed for partial scan circuits. However, to the best of our knowledge, there have been no systematic approaches to generate broadside transition tests for partial scan circuits so far. In this paper, we tackle this problem. It is notable that broadside transition testing for partial scan circuits has a possibility of alleviating over-testing, which is one of the main concerns during testing [11], [12], in addition to reducing the penalties of area and delay.

This paper proposes a method of broadside test generation for transition faults in partial scan circuits. This method targets partial scan circuits whose *kernel* circuits are acyclic. To generate broadside transition tests for a partial scan circuit, we transform its kernel circuit into some combinational circuits. This transformed circuits, which are called *broadside test generation models*, are constructed by using a *time-expansion model* [13] of the kernel circuit. All the broadside transition tests are generated by performing constrained stuck-at test generation on the broadside test generation models. In this paper, we give a theorem to show the correctness of the proposed method and its proof. Our method is effective in terms of ease of use because commercial test generation tools, which are usually capable of handling combinational stuck-at test generation efficiently, can be used to generate broadside transition tests. Through experiments, we show that our method can reduce area overhead and can generate broadside transition tests for partial scan circuits efficiently.

II. Preliminaries

This section describes our target circuits and faults, and explains some related works.

A. Target Circuits and Faults

This paper targets partial scan circuits whose kernel circuits are acyclic. A sequential circuit can be represented as

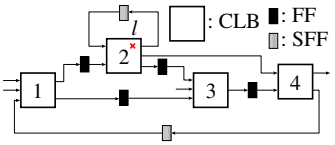

Fig. 1. Partial scan circuit: S

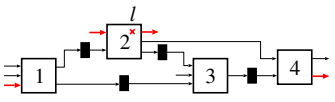

Fig. 2. Kernel circuit of Figure 1: S_K

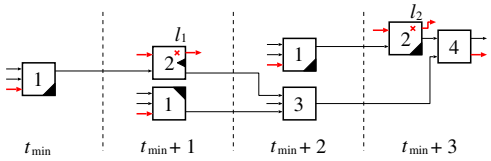

Fig. 3. Time-expansion model of Figure 2: $C^T(S_K)$

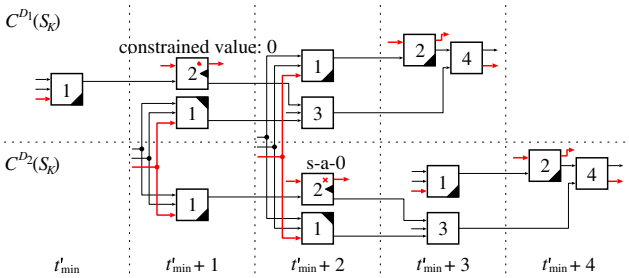

Fig. 4. Double time-expansion model of Figure 2: $C^D(S_K)$

combinational logic blocks (CLBs) connected with each other directly or through FFs. A CLB is a region of connected combinational logic gates. Figure 1 is an example of a partial scan circuit S, and its kernel circuit S_K is shown in Figure 2. The input (resp. output) of an SFF in Figure 1 is treated as a primary output (PO) (resp. primary input (PI)) in Figure 2, which is represented as a bold arrow and called a pseudo primary output (PPO) (resp. pseudo primary input (PPI)). Note that, our method is also applicable to a full scan circuit with multiple scan chains. This is because, by enabling a subset of scan chains such that the kernel circuit is made acyclic and treating SFFs on the other chains as normal FFs, we can apply our method to the kernel circuit. We handle a broadside test generation problem for *transition faults* in a partial scan circuit. There are two transition faults associated with each line in a circuit: a *slow-to-rise fault* and a *slow-to-fall fault*. It is assumed that, under the transition fault model, the extra delay caused by a transition fault is large enough to prevent the transition through the faulty site from reaching any FF or any PO within a specified period. In this paper, we assume that transition faults in a partial scan circuit are tested in the slow-fast-slow testing manner [14]. Under this assumption, we can consider a sequential circuit to be delay fault-free in both of the fault initialization and fault effect propagation phases. Note that if a transition fault is testable under the at-speed testing manner, the fault is also testable under the slow-fast-slow testing manner [14]. Hence, slow-fast-slow testing never misses any fault testable in at-speed testing.

B. Double Time-Expansion Model

A *double time-expansion model* [15] has been proposed to generate transition tests for an acyclic sequential circuit. Given an acyclic sequential circuit, a double time-expansion model of the circuit is constructed from a *time-expansion model (TEM)* [13] of the circuit. In the following paragraphs, we briefly explain those two models.

A TEM of an acyclic sequential circuit is a combinational circuit in which the behavior of the original circuit within a specific time span is simulated. Figure 3 is a TEM $C^T(S_K)$ of the kernel circuit S_K shown in Figure 2. TEM $C^T(S_K)$ is a combinational circuit derived by connecting CLBs according to their sequential depths. A sequential depth between two CLBs is defined as the number of FFs on a path between the CLBs. If a CLB has paths to another CLB in S_K whose sequential depths are different, the CLB is duplicated in $C^T(S_K)$. For example, in Figure 2, since CLB 2 has two paths to CLB 4 whose sequential depths (zero and two) are different, CLB 2 is duplicated in $C^T(S_K)$. A shaded part of a CLB in Figure 3 represents a portion of the lines and gates being removed. There is no path from the portion to any input of CLBs or any PO and PPO of $C^T(S_K)$. The character placed at the bottom of each frame in Figure 3 is the label of CLBs in the frame, where $t_{\min}$ denotes an arbitrary integer. The label of a CLB v is denoted as $t(v)$ which corresponds to a specific time.

A double time-expansion model is defined as follows [15].

Definition 1: Let S be an acyclic sequential circuit, and $C^T(S)$ be a TEM of S. Then, a combinational circuit obtained by the following procedure is said to be a double time-expansion model (DTEM) $C^D(S)$ of S.

S1: Make two copies of $C^T(S)$: $C^{D_1}(S)$, $C^{D_2}(S)$.

S2: Connect each pair of PIs u in $C^{D_1}(S)$ and v in $C^{D_2}(S)$ such that $t(u) - t(v) = 1$ and $l(u) = l(v)$, and feed a new primary input w into them, where $l(u) = l(v)$ means that u and v are identical in S. ■

For example, a DTEM $C^D(S_K)$ of S_K (Figure 2) is constructed as Figure 4 according to the above definition. Note that although two copies of CLB 1 in $t'_{\min}+1$ (also in $t'_{\min}+2$) can be merged into one CLB, $C^D(S_K)$ is expressed as Figure 4 to differentiate $C^{D_1}(S_K)$ and $C^{D_2}(S_K)$ from each other. If one wants to test the slow-to-rise fault on line l in S_K, test generation for one of the corresponding stuck-at 0 fault is performed on $C^D(S_K)$ under the constrained value of 0 that must be satisfied during test generation. In this way, transition tests for an acyclic sequential circuit can be generated by using

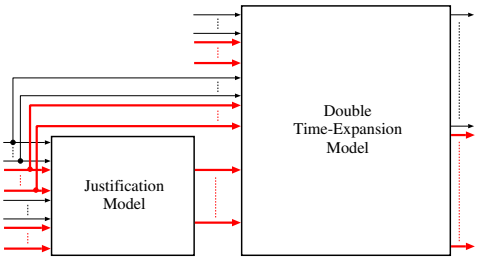

Fig. 5. Overview of a broadside test generation model

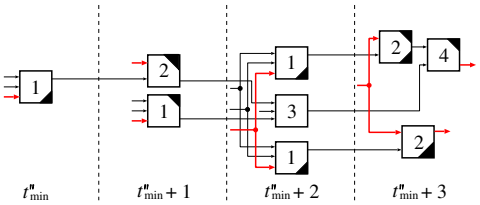

Fig. 6. Justification model with respect to $t'_{\min}+2$ in Figure 4: $C^J_{t'_{\min}+2}(S_K)$

a DTEM.

In [15], an acyclic sequential circuit is assumed to be obtained as a kernel circuit of a given circuit by using enhanced scan technique. Thereby, for example, two consecutive vectors V_1 and V_2 for the PPIs at the times corresponding to $t'_{\min}+1$ and $t'_{\min}+2$ in Figure 4 are stored in ESFFs. Here, suppose a given circuit is designed by using standard scan technique. In this case, although only V_1 can be stored in SFFs, V_2 must be justified by using some technique. In the next section, we discuss this problem.

III. Proposed Method

In this section, we discuss a new test generation model for broadside transition testing of partial scan circuits, and present a test generation procedure using the new model.

A. Broadside Test Generation Model

As pointed out in Section II-B, vectors for PPIs in a frame, where a stuck-at fault exists, of a DTEM, must be justified by using some technique. Note that this frame is called a *test frame*. In order to achieve this requirement, we propose a *broadside test generation model*. The overview of a broadside test generation model is shown in Figure 5. A broadside test generation model is composed of a DTEM and a *justification model* which is used for the above requirement. The justification model and the broadside test generation model are defined as follows.

Definition 2: Let S and S_K be a partial scan circuit and its acyclic kernel circuit, respectively. Let $C^T(S_K)$ and $C^D(S_K)$ be a TEM of S_K and a DTEM of S_K, respectively. Let t be the label value of a test frame in $C^D(S_K)$. Then, a combinational circuit obtained by performing the following procedure is said to be the justification model (JM) $C^J_t(S_K)$ with respect to t.

S1: For each PPI which belongs to only $C^{D_2}(S_K)$ in t, extract the logic cone of the corresponding PPO in $C^T(S_K)$. Also, for each PPI shared by $C^{D_1}(S_K)$ and $C^{D_2}(S_K)$ in t, extract the logic cone of the corresponding PPO in $C^T(S_K)$.

S2: For each pair of the logic cones, connect each pair of PIs (resp. PPIs) u in one cone and v in the other cone such that $t(u)=t(v)$ and $l(u)=l(v)$, and feed a new PI (resp. PPI) w into them. ■

Definition 3: Let S and S_K be a partial scan circuit and its acyclic kernel circuit, respectively. Let $C^D(S_K)$ and $C^J_t(S_K)$ be a DTEM of S_K and the JM with respect to the label value t of a test frame in $C^D(S_K)$. Then, a combinational circuit obtained by performing the following procedure is said to be the broadside test generation model (BTGM) $C^B_t(S_K)$ with respect to t.

S1: For each PPI which belongs to only $C^{D_2}(S_K)$ in t, connect the corresponding PPO of $C^J_t(S_K)$ to the PPI. Also, for each PPI shared by $C^{D_1}(S_K)$ and $C^{D_2}(S_K)$ in t, connect the corresponding PPO of $C^J_t(S_K)$ to the PPI.

S2: Connect each pair of PIs (resp. PPIs) u in $C^J_t(S_K)$ and v in $C^D(S_K)$ that $t(u)=t(v)$ and $l(u)=l(v)$, and feed a new PI (resp. PPI) w into them. ■

Notice that, for a given circuit, $d+1$ JMs are created, where d denotes the sequential depth of its kernel circuit. Hence, $d+1$ BTGMs are also created.

Figure 6 shows the JM $C^J_{t'_{\min}+2}(S_K)$ of Figure 4. This JM is composed of the logic cone of the PPO of CLB 4 in $t_{\min}+3$ (Figure 3) and that of the PPO of CLB 2 in $t_{\min}+3$. Note that although those two logic cones can share CLBs 1 and 2, we explicitely express the two logic cones for simplicity. Figure 7 shows the BTGM $C^B_4(S_K)$ of Figure 4. In creating this BTGM, the value of 2 is assigned to $t'_{\min}$ of Figure 4 and the value of 0 is assigned to $t''_{\min}$ of Figure 6. As shown in Figure 7, CLBs in a frame are not shared to differentiate the DTEM and the JM. Patterns that are needed to activate stuck-at faults in a test frame and propagate those effects to a PO or a PPO can be justified by using its JM.

B. Test Generation Flow

Given a partial scan circuit S whose kernel circuit S_K is acyclic, broadside transition tests for S are generated as follows:

S1: Create a transition fault list F^T of S.

S2: Construct $d+1$ BTGMs $C^B_{t_1}(S_K),\ldots,C^B_{t_{d+1}}(S_K)$ of S_K, where d is the sequential depth of S_K.

S3: Create stuck-at fault lists F^S_1 for $C^B_{t_1}(S_K)$,..., F^S_{d+1} for $C^B_{t_{d+1}}(S_K)$ corresponding to F^T, and constrained value lists C_1 for F^S_1 ,..., C_{d+1} for F^S_{d+1}.

S4: For each stuck-at fault $f^S \in F^S_i$ $(i=1,\ldots,d+1)$,

(a): generate a test pattern t^S under the corresponding constraint $c \in C_i$, and

(b): transform t^S into a broadside test t^T for the corresponding transition fault f^T $\in$

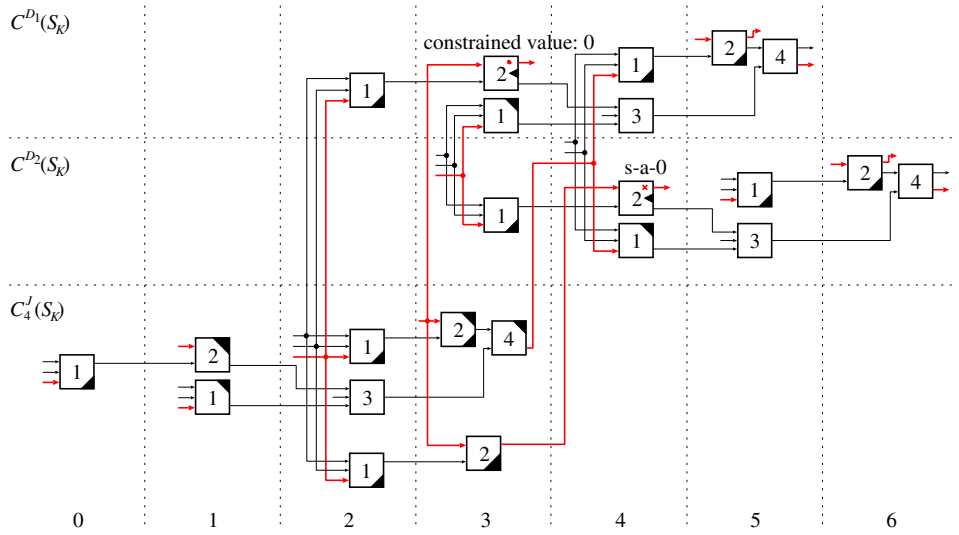

Fig. 7. Broadside test generation model with respect to $t'_{\text{min}}+2$ ($t'_{\text{min}}=2$) in Figure 4: $C_4^B(S_K)$

F^T according to the label information of $C_{t_i}^B(S_K)$.

Note that, in S3, even if a transition fault in a given circuit corresponds to some stuck-at faults in its BTGMs, we can handle the respective stuck-at faults one by one because generated broadside transition tests are applied in the slow-fast-slow testing manner. In S4, if all the stuck-at faults corresponding to a transition fault are identified as untestable, the transition fault is also untestable. Moreover, it is sufficient to generate a test pattern for one of the stuck-at faults corresponding to a transition fault. In S4 (b), t^S is transformed into t^T as follows. For example, in Figure 7, a pattern for the PIs and the PPI of CLB 1 in frame 0 is transformed into a pattern for the PIs of CLB 1 and the corresponding SFF at time 0 in Figure 1. Notice that, the pattern for the SFF is set by scan-in operation before time 0. Other patterns in frames from 1 to 6 are transformed in the same way.

The following theorem shows the correctness of our test generation method.

Theorem 1: Let S and S_K be a partial scan circuit and its kernel circuit which is acyclic, respectively. Let $f_{\uparrow}^T$ (resp. $f_{\downarrow}^T$) be a slow-to-rise (resp. slow-to-fall) transition fault in S. Let $F_{\text{s-a-0}}^S$ (resp. $F_{\text{s-a-1}}^S$) be the set of stuck-at 0 (resp. 1) faults corresponding to $f_{\uparrow}^T$ (resp. $f_{\downarrow}^T$). Then, $f_{\uparrow}^T$ (resp. $f_{\downarrow}^T$) is testable under the broadside testing manner if and only if at least one $f_{\text{s-a-0}}^S \in F_{\text{s-a-0}}^S$ (resp. $f_{\text{s-a-1}}^S \in F_{\text{s-a-1}}^S$) in the corresponding BTGM $C_t^B(S_K)$ is testable under the constrained value of 0 (resp. 1).

Proof: Broadside transition test generation for $f_{\uparrow}^T$ (resp. $f_{\downarrow}^T$) in S can be viewed as test generation for the stuck-at 0 (resp. 1) fault in S corresponding to $f_{\uparrow}^T$ (resp. $f_{\downarrow}^T$) in a situation where (a) the constrained value of 0 (resp. 1) must be set to the faulty site at time $t_{1\text{st}}$, and (b) no scan operation must be performed between $t_{1\text{st}}$ and $t_{2\text{nd}}$. Here, $t_{2\text{nd}}$ denotes a time at which the stuck-at 0 (resp. 1) fault in S is activated, and $t_{1\text{st}} = t_{2\text{nd}} - 1$. In [13], it has been shown that the stuck-at test generation problem for an acyclic sequential circuit can be reduced to that for its TEM. The properties of a TEM still hold in a BTGM because the BTGM is constructed by using the TEM. Hence, to demonstrate this theorem, we need to show that (a) and (b) are satisfied in test generation for the BTGM.

First, under the slow-fast-slow testing manner, it is sufficient to consider whether at least one $f_{\text{s-a-0}}^S \in F_{\text{s-a-0}}^S$ (resp. $f_{\text{s-a-1}}^S \in F_{\text{s-a-1}}^S$) is testable. Since, in $C_t^B(S_K)$, stuck-at test generation for $f_{\text{s-a-0}}^S$ (resp. $f_{\text{s-a-1}}^S$) is performed under the constrained value of 0 (resp. 1), (a) is satisfied. Furthermore, since patterns for $f_{\text{s-a-0}}^S$ (resp. $f_{\text{s-a-1}}^S$) in the test frame of $C_t^B(S_K)$ are justified by its JM, (b) is also satisfied. Thus, the theorem is demonstrated. ■

C. Test Application

In this subsection, we describe how to apply broadside transition tests to a partial scan circuit.

Broadside transition tests generated by the method of Section III-B are applied to a partial scan circuit S whose kernel circuit S_K is acyclic as follows. Let $C^D(S_K)$ be a DTEM of S_K, and t be the label value of a test frame. In test application, the circuit is operated at a slow clock speed except when its rated clock is applied at the time corresponding to t. If there exists a PPI in a frame before the test frame, scan-in operation is performed before the corresponding time. Also, if there exists a PPI which belongs to only $C^{D_2}(S_K)$ in a frame after the test frame t, scan-in operation is performed before the corresponding time. Scan-out operation is performed after the corresponding time if there exists a PPO which belongs to only $C^{D_2}(S_K)$ in a frame between the test frame t and the last frame. Note that, in order to keep the values of normal FFs during scan operation, the system clock must be separated from the scan clock or all the normal FFs have to be redesigned

such that the values can be held during scan operation. For example, a broadside transition test generated by performing test generation on the BTGM $C_4^B(S_K)$ shown in Figure 7 is applied to the partial scan circuit shown in Figure 1 as follows. Scan-in operation is performed before each time from 0 to 3, then the circuit is operated at a slow clock speed. The transition to activate faults is created between times 3 and 4, then between times 4 and 5, its fault effect is captured at the rated clock speed. Before each time of 5 and 6, scan-in and scan-out operations are performed simultaneously, then the circuit is operated at the slow clock speed. After time 6, scan-out operation is performed. Let d be the sequential depth of S_K. The length of a broadside transition test can range from $d+2$ to $2d+2$. In the case of Figure 2, it ranges from 5 to 8.

IV. Experimental Results

In this section, we evaluate the proposed method in terms of area overhead, fault coverage, fault efficiency and test generation time.

The following experiment was performed on a Sun Fire V890 workstation (CPU: UltraSPARC IV 1.35GHz $\times$ 8, Memory: 64GB). TetraMAX from Synopsys was used as a stuck-at test generation tool, and its backtrack limit was set to 100. We applied our method to six 32bit datapath circuits [16]. The characteristics of the circuits are shown in Table I. Columns "#PIs," "#POs," and "#FFs" list the number of PIs, POs and FFs, respectively. Column "Area" gives the area of a circuit which is estimated by Design Compiler from Synopsys, where the area of a 2-input NAND gate is considered to be 2. In this experiment, we compared the proposed method to fully enhanced scan testing and broadside testing based on the full scan method.

First, we show area overheads needed for the three methods considered. In our method, acyclic kernel circuits for all the circuits were obtained by using the exact algorithm in [17]. In Table I, the last two columns show method names and those area overheads, respectively. Fully enhanced scan testing, broadside testing based on the full scan method and the proposed one are denoted by "ES," "SS" and "Our Method" respectively. In estimating area overhead, the areas of an ESFF and an SFF were 27 and 17, respectively. For all the circuits, we achieved the lowest area overheads. Since the proposed method is based on partial scan design, we can achieve low area overhead compared with the other methods.

Next, we show test generation results. In this experiment, we compared fault coverage, fault efficiency and test generation time of our method with those of the other two methods, and fault simulation was not invoked. In "ES," to generate transition tests, constrained stuck-at test generation were performed on a combinational circuit that consists of two independent copies of the combinational part of a given circuit. For example, to generate a two-pattern test for a slow-to-rise transition fault, we performed stuck-at test generation for the stuck-at 0 fault in the second copy under the following constraint: the value of 0 must be set to the corresponding site in the first copy. Similarly, in "SS," we performed constrained stuck-at test generation on a combinational circuit corresponding to the two time frames of a given circuit. For example, to generate a two-pattern test for a slow-to-rise transition fault, we performed stuck-at test generation for the stuck-at 0 fault in the second time frame under the following constraint: the value of 0 must be set to the corresponding site in the first time frame. Table II lists the test generation results. Columns "#flt," "#det" and "#unt" give the number of targeted transition faults, detected faults, identified untestable faults, respectively. Columns "FC [%]," "FE [%]" and "TGT [s]" denote fault coverage ($= 100 \times$ #det/#flt), fault efficiency ($= 100 \times$ (#det+#unt)/#flt) and test generation time, respectively. The last column "Model Size" represents the average area of broadside test generation models in "Our Method," and the area of the test generation model used in each case of "ES" and "SS," which are estimated by Design Compiler. In Table II, all the methods achieved complete fault efficiency. Since our broadside test generation model is larger (about 2.0 times larger on average) than the test generation models used in the other two methods, the test generation time of our method increased in some circuits. However, we consider our method to be comparable to the other two methods in test generation time. The reason is as follows. In [18], the time complexity for practical instances of the test generation problem for combinational circuits was claimed to be $O(n^3)$, where n is the size of a combinational circuit. Nevertheless, it was not observed in our method. For example, in IIR, the test generation time of our method was only about 2.2 times longer than that of the other two methods, although the size of our broadside test generation model was about 2.9 times larger than that of the test generation models used in the other two methods.

From the experimental results, we can see that our method can provide a good trade-off between area overhead and test

TABLE I
Original circuit characteristics and area overhead results

Circuit	#PIs	#POs	#FFs	Area	Method	Area OH [%]
EWF	57	32	352	9,276	ES	64.5
					SS	26.6
					Our Method	16.9
IIR	48	32	224	16,519	ES	23.1
					SS	9.5
					Our method	5.4
JWF	44	32	224	6,947	ES	54.8
					SS	22.6
					Our Method	16.1
LWF	35	32	96	2,614	ES	62.4
					SS	25.7
					Our Method	8.6
Paulin	41	64	192	19,174	ES	17.0
					SS	7.0
					Our Method	4.7
Tseng	104	32	160	12,150	ES	22.4
					SS	9.2
					Our Method	3.7

TABLE II
TEST GENERATION RESULTS

Circuit	#flt	Method	#det	#unt	FC [%]	FE [%]	TGT [s]	Model Size
EWF	17,646	ES	17,622	24	99.86	100.00	27.69	11,512
		SS	17,622	24	99.86	100.00	23.34	11,512
		Our Method	17,622	24	99.86	100.00	32.62	26,268
IIR	38,444	ES	38,388	56	99.85	100.00	106.31	28,558
		SS	38,388	56	99.85	100.00	104.27	28,558
		Our Method	38,388	56	99.85	100.00	229.43	83,574
JWF	13,692	ES	13,676	16	99.88	100.00	15.76	9,414
		SS	13,676	16	99.88	100.00	14.65	9,414
		Our Method	13,676	16	99.88	100.00	14.35	16,788
LWF	4,804	ES	4,796	8	99.83	100.00	3.51	3,308
		SS	4,795	9	99.81	100.00	3.64	3,308
		Our Method	4,795	9	99.81	100.00	2.77	6,171
Paulin	46,248	ES	46,248	0	100.00	100.00	165.33	34,508
		SS	46,248	0	100.00	100.00	164.12	34,508
		Our Method	46,248	0	100.00	100.00	252.15	51,762
Tseng	28,592	ES	28,592	0	100.00	100.00	83.07	21,100
		SS	28,501	91	99.68	100.00	101.81	21,100
		Our Method	28,501	91	99.68	100.00	154.58	33,051

generation effort. It is conceivable that the proposed method can also work efficiently for more complex circuits because combinational stuck-at test generation is performed.

V. CONCLUSIONS AND FUTURE WORK

In this paper, we proposed a method of broadside test generation for transition faults in partial scan circuits, and showed the correctness of the method by the theorem. The proposed scheme can utilize existing combinational stuck-at test generation tools to generate broadside transition tests of partial scan circuits. This feature is very useful from the practical point of view. Through experiments, we showed that our method can reduce area overhead and can generate broadside transition tests in reasonable test generation time.

Our future work is to handle a more general delay fault model, i.e., the path delay fault model, in this frame work.

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