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Diagnosing At-Speed Scan BIST Circuits Using a Low Speed and Low Memory Tester

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Abstract

Numerous solutions have been proposed to reduce test data volume and test application time during manufacturing testing of digital devices. However, time to market challenge also requires a very efficient debug phase. Error identification in the test responses can become impractically slow in the debug phase due to large debug data, slow tester speed and limited memory of the tester. In this paper, we investigate how a relatively slow and limited memory tester can observe the at-speed behavior of fast circuits. Our method can identify all errors in at-speed scan BIST environment without any aliasing and negligible extra hardware while taking into account the relatively slower speed of the tester and the re-load time of the expected data to the tester memory due to limited tester memory. Experimental results show that the test application time by our method can be reduced by a factor of 10 with very little hardware overhead to achieve such advantage.

1. Introduction

Built-in self-test (BIST) has become one of the major test techniques for today's large scale and high speed designs. Since BIST compacts test responses, BIST requires only small tester memory and it can perform at-speed test even if the tester frequency is substantially lower than the frequency of the circuit during test.

On the other hand, BIST causes problems in diagnosis due to its compacted responses. Indeed, pass/fail information obtained from a BIST response analyzer is insufficient for diagnosis. Two kinds of information are required to identify a fault in a circuit under test (CUT), namely the time information, and the space information. High resolution diagnostic for a given fault model can be achieved by diagnosis techniques combining space information with time information [4, 5]. A number of methods to identify space information have been proposed, especially for scan-based BIST architecture [6-11], however, only a few practical techniques have been developed to identify time information.

Some of the existing techniques are based on signature analysis using cycling register [11,12] and error correcting codes [13]. These methods compact the complete test response into one signature and attempt to identify errors from the signature. Since they observe signature only once, they are usable even if the circuit frequency is much higher than the tester frequency. However, for large number of error bits, say r errors, they need as many as r-LFSRs or signature registers and may have over 40% diagnostic aliasing if the actual number of errors is higher than r [13]. Thus, they either have poor diagnostic resolution or require impractically high hardware overhead to achieve maximum diagnostic resolution. An alternative approach trades off overhead for time by repeating the test sequence and compacting it at each iteration into a different signature [14]. Thus, instead of using $r-$LFSRs, the test sequence is repeated r times using programmable LFSR to identify r errors. Since it is mathematically equivalent to [13], diagnostic aliasing is same as using r-LFSRs. Thus, identifying all the errors requires repeating the test sequence an impractically large number of times. Techniques that use two phases for diagnosis have also been proposed [15-17]. During the first phase, intermediate signature is checked a few times during test in order to narrow down the failing candidates within some windows of fixed or variable size. The failing patterns are then identified inside the windows by applying the corresponding patterns one at a time [15]. These methods use small hardware overhead and/or reduce test application time but they assume the existence of a mechanism to observe the at-speed behavior inside of failing windows. Enhancement of these methods has also been studied using multiple signature analyzers [17], but they do not achieve maximum diagnostic resolution. A commonly used diagnosis technique requires and collects the failing space and time information, without compacting responses, during the diagnosis phase [18] but suffers from the following two problems.

One, it requires the circuit to operate at the tester frequency during test; therefore, the faults that affect only at-speed operation may not be diagnosable. Two, this method requires all expected responses of scan cells to be loaded into tester. Even the high-end testers often do not have sufficient memory to store all expected scan cell data of all BIST sequences. Therefore, expected data in such a scheme must be re-loaded many times to the tester memory. Clearly, this can be very time consuming. The method proposed in [19] solves the first problem, but the second problem remains.

In this paper, we investigate methods to identify every error occurrence in at-speed scan based BIST environment. Every error can be identified even if the circuit test frequency is higher than the tester frequency. In Section 2 we briefly introduce a procedure to identify every error without any aliasing in at-speed scan BIST environment proposed in [19]. In Section 3, we formulate the problem of identifying every error occurrence in minimum test time, including tester loading time, and propose a method to reduce test application time by pattern grouping and using signature analyzers. In Section 4, we analyze the test time of the method proposed in Section 3 to find the optimal group size. In Section 5 we show the effectiveness of our method through experimental results and discuss the relationship between the error probability and optimal group size. Section 6 summarizes the conclusions of our analysis.

2. Observing Responses by a Slow Speed Tester

Before providing a formulation of the problem we describe the method given in [19] that can identify all failing responses by observing scan outputs even if the CUT test frequency is faster than the maximum tester frequency (in sequel, we will call the maximum test frequency *tester frequency limitation*). Fig. 1 demonstrate this through an example. When the CUT clock period is 2ns and the tester observing period is 6ns, a tester can observe only 1/3 of the responses. Thus, it will not be able to identify all possible failing responses in one BIST sequence. Nevertheless, there is a way to observe all responses without adding any extra hardware. We assume that the pattern generator (PG) is reset to the initial state after generating the last pattern. If the BIST sequence is 17 cycles long, as shown in Fig.1, every cycle can be observed by repeating the BIST sequence three times (i.e., applying 51 clocks). During the first sequence, the tester observes response bit 0, 3,.., 15. Then bits 1, 4,. . . , 16 are observed during the second sequence and bits 2, 5,. . . , 14 during the third sequence. Note that such a method may not always allow observing all bits by simple repetition of the sequence. For example if the length of the BIST sequence is 18, the tester cannot observe every response by simply repeating the sequence since only bits 0,3,. . . ,15 are observed repeatedly. Let N be the length of the BIST sequence, f_c be the clock frequency of the CUT,

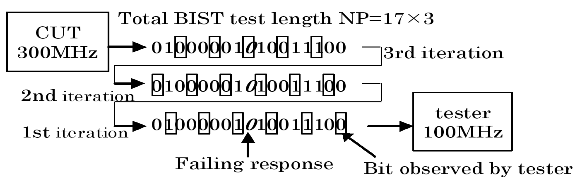

Figure 1. Multiple iteration observation

and f_t be the tester frequency limitation, then the conditions to observe all responses is $\gcd(N, P) = 1$, where $P = f_c/f_t$. The tester can observe all responses by applying the BIST test sequence P times, while observing its response at every time period P. If N is not co-prime to P, both N or P can be adjusted to make it co-prime. It is shown in [19] that increasing only the length of BIST sequence N by inserting no more than P additional dummy clock cycles achieves minimum test application time in general.

We can identify all erroneous responses with a slow speed tester using this method, albeit requiring all expected responses of scan cells to be loaded into the tester. Usual testers do not have enough memory to store all expected scan cell data of all BIST sequences. Therefore, we have to re-load expected data many times to the tester which can be quite time consuming.

3. Using Signature Analyzers

3.1. Problem Formulation

In this section, we formulate the problem of identifying failing responses in minimum testing time. We first identify some characteristics of the diagnosis process and production testing process. Diagnosis can be performed for devices that didn't pass the production test or devices that passed the production test and were found to be faulty in the field. In each case, testing during diagnosis should be performed at the speed that resulted in the failure of the device. Another characteristic is that the test application time is not the first priority for diagnosis. Rather, the quality of diagnosis is far more important than the test application time. However, the fault diagnosis must not be overloaded by the error information to achieve the required diagnostic resolution. It is imperative that the reported (required) number of errors be limited to achieve the targeted diagnosis resolution. Our formulation concerns the error identification of a scan based BIST circuit. We constrain BIST to operate at-speed during diagnosis. In the at-speed BIST environment, we assume that the CUT operates at frequency f_c, whereas the tester has a frequency limitation and cannot operate at a frequency higher than f_t, such that $f_t < f_c$. We also constrain the number of errors to be identified to E, and no error-free response should not be identified as erroneous. The objective of the problem is to minimize the testing time.

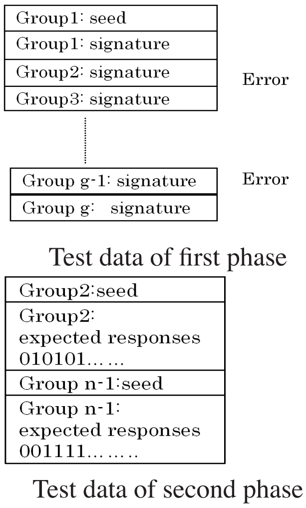

Figure 2. Test data for error identification

Note that the tester loading time should be included in test time as mentioned in Section 2.

3.2. Signature Analyzers for Error Identification

The method introduced in Section 2 does not use signature analyzers. Therefore, it can achieve maximum diagnostic resolution without aliasing; however, the test time, including tester loading time significantly increases when the test sequence becomes very long. On the other hand, the error identification methods using signature analyzer require less tester memory, i.e., fewer re-loadings, therefore, testing time will be much shorter than the method introduced in Section 2. Note that the method using signature analyzer causes diagnostic aliasing and it is undesirable when an erroneous response is miss-identified as error-free since it can lead to misdiagnosis. Also, as argued in the previous subsection, it is important that the fault diagnosis algorithm is not overwhelmed by excessive error information Therefore; it will be acceptable to base a diagnostic decision when sufficiently many erroneous responses for diagnosis are identified.

In this paper, we propose an error identification procedure that uses signature analyzers in two phases. During the first phase, the intermediate signature is checked in order to narrow down the error candidates within some windows [15-17]. The failing responses are then identified inside the windows during the second phase using the method introduced in Section 2 for at-speed BIST environment. This study aims at minimizing the test time, in particular by determining the optimal window size for use in phase one.

To enable two phase error identification, all the BIST sequences are divided into groups. Each pattern group includes the seed for the pattern generator that consists of the state of the pattern generator at the end of the previous group. Each pattern group also includes the expected signature for the group.

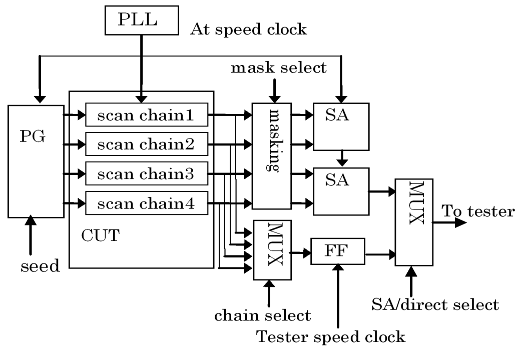

Figure 3. BIST architecture

The first phase identifies erroneous groups. The seeds of the first group and all expected signatures are loaded onto the tester as shown in Fig.2. The test pattern is then generated by the pattern generator and the scan out responses are compacted into signature analyzers. The erroneous pattern groups are identified by observing the result of the signature analyzers. The group size should be large enough to reduce the test data in first phase. The second phase identifies erroneous responses in the erroneous pattern groups. The seeds and the expected responses of the erroneous pattern group, which is identified in first phase, are loaded onto the tester. By using error identification procedure proposed in Section 2 for all erroneous groups, all errors can be identified. Note that the test data size for error identification is much smaller than the prior approach explained in Section2 since only test data of erroneous groups is loaded onto tester.

Some erroneous responses may be dropped due to aliasing of signature analyzers in the first phase; however, any error-free response cannot be identified as erroneous, thus satisfying the constraints of the problem formulation.

In the first phase, larger groups result into a larger reduction in test data and this reduces test time including tester loading time. Whereas, in the second phase, larger groups result into a smaller reduction in test data since larger groups increase the error probability of a pattern group. Therefore, there is an optimal group size for minimum test time. Later in this paper, we deduce the optimal group size for two phase error identification.

3.3. A BIST Architecture

Fig.3 shows a BIST architecture with the logic required for diagnosis. MISRs are used as signature analyzers during testing, and during diagnosis, a masking circuit allows only one scan chain to feed a signature analyzer which is selected by input “mask select”.

As shown in Fig.3, scan outs are connected to an output port via a multiplexer during diagnosis as in the noncompaction based approach [19]. A Register, FF, is inserted at the multiplexer output to synchronize the scan chain with the tester since the CUT test frequency may be higher than the tester frequency. The FF samples the signal produced by the scan chain and holds the value during one tester period.

In the first phase of identification procedure, each signature analyzer compacts responses of one scan chain which is selected by masking circuit. If there are n_{SA} signature analyzers, n_{SA} pattern groups in different scan chains can be simultaneously tested.

On the other hand, in the second phase, only one group in one scan chain, selected by multiplexer, can be tested since we don't use signature analyzers in the second phase.

3.4. Procedure of Error Identification

Summarizing Section 3.1-3.3, the procedure for identifying error occurrence is as follows.

Given condition

Test frequency of CUT : f_c

Tester frequency limitation: f_t

Number of signature analyzers: n_{SA}

BIST test length: N

Number of pattern groups: g

Number of scan cells in a scan chain: L

Target number of errors identified: E

Step 1. identify erroneous pattern groups

Step 1.1. Select untested pattern groups for each signature analyzers.

Step 1.2. Apply BIST sequence and identify erroneous signature analyzers, i.e, erroneous pattern groups.

Step 1.3. Repeat step 1.1-1.2 until all pattern groups are tested. Total number of BIST iterations is: g/n_{SA}

Step 2. Identify erroneous scan cell and pattern

Step 2-1. Select an erroneous group which is identified in Step1. The size of pattern group is $w = N/g$.

Step 2-2. Set observing time period P as $P = f_c/f_t$. Adjust the BIST test length by adding minimum α dummy clocks (i.e., $w' = w + \alpha$) such that w' and P are co-prime. Reset the BIST iteration counter $r = 0$ and tester observation counter $i = 0$.

Step 2-3. Apply Pw' clocks to BIST pattern generator, observing one scan output every P test cycles.

Step 2-4. If an error is detected at the $(i+1)^{th}$ observation, then:

Relative time of error occurrence e is: $e = iP \mod w'$

Failing scan pattern = $\lfloor e/(L+1) \rfloor$

Erroneous scan cell = e mod (L+1)

Step 2-5. Repeat Step2.1-2.4 until E errors identified.

4. Optimizing Group Size

4.1. Tester Loading Rate

Test data is prepared for each faulty chip in the fault diagnosis phase. Therefore, tester loading time can not be ignored especially in view of the fact that the tester may not have sufficient memory for all test data. In this case, the tester should load the test data several times.

The tester loading time will normally be proportional to the test data volume and the overhead associates with each tester loading. Thus the tester loading timeT_{Load} can be expressed using two constants L_C and L_V as

$$T_{Load} = L_C \cdot (\#of\, tester\, loads) + L_V \cdot V \qquad (1)$$

where V is the test volume. Let M be the tester memory size, then the number of tester loading is V/M. Therefore:

$$T_{load} = V\left(\frac{L_C}{M} + L_V\right) \qquad (2)$$

Note that L_C, L_V, M are parameters associated only with the tester. Denote $r_{Load} = M/(L_C + ML_V)$, the tester loading time is:

$$T_{load} = \frac{V}{r_{Load}} \qquad (3)$$

In this paper, we use r_{load} as the bit rate of tester loading. Note that the parameter r_{load} reflects tester memory limitation also.

4.2. Analysis of Test Time

In this section, we estimate the test time for the error identification procedure.

We use following notation in the analysis below.

N: total length of the BIST sequence

w: Size of the expected response of one group

g: number of groups of all scan chains($g = N/w$)

S_{SA}: bit size of signature

S_{PG}: bit size of pattern generator

n_{SA}: number of signature analyzers

r_{Load}: bit rate for loading to the tester

f_c : CUT test frequency

f_t: tester frequency

g_e: number of groups identified erroneous in Step1

Analysis of Step1 The error identification procedure Step1 identifies erroneous pattern groups.

The total test time including tester loading time is

Total test time = test application time + tester loading time

The test application time of Step1 can be estimated as follows. In Step1 we test n_{SA} groups simultaneously using n_{SA} signature analyzers. Therefore the BIST pattern should be applied in g/n_{SA} times. At the end of the BIST session, we read out the signature. We assume that we read out signatures on one output port as shown in Fig.3.

Therefore, the test application time of Step1 is

$$TAT_{Step1} = g\left(\frac{w}{n_{SA}f_c} + \frac{S_{SA}}{f_t}\right) + \frac{S_{PG}}{f_t} \qquad (4)$$

The total test volume for Step1 is

$$V_{Step1} = gS_{SA} + S_{PG} \quad (5)$$

Therefore total test time including loading time is:

$$T_{step1} = TAT_{Step1} + V_{Step1}/r_{Load} \quad (6)$$

Analysis of Step2 We identify erroneous responses in the error identification procedure Step2. The error identification procedure will be finished when we identify predetermined E errors. And since only erroneous groups are tested in Step2, the expected number of erroneous bit in one group is

$$E_w = \frac{w\,\Pr\{1\,bit\,error\}}{\Pr\{1\,group\,error\}} = \frac{w\,\Pr\{1\,bit\,error\}}{1-(1-\Pr\{1\,bit\,error\})^w} \quad (7)$$

Therefore, the expected number of groups contains E errors is:

$$g'_e = \frac{E}{E_w} = \frac{E\,(1-(1-\Pr\{1\,bit\,error\})^w)}{w\,\Pr\{1\,bit\,error\}} \quad (8)$$

We must apply BIST sequence f_c/f_t times for erroneous groups. Therefore the test application time of Step2 is:

$$TAT_{step2} = \frac{f_c g'_e}{f_t}\left(\frac{w}{f_c} + \frac{S_{PG}}{f_t}\right) = \frac{g'_e}{f_t}\left(w + \frac{f_c S_{PG}}{f_t}\right) \quad (9)$$

The test volume is

$$V_{Step2} = g'_e(w + S_{PG}) \quad (10)$$

Total test time including loading time is:

$$T_{step2} = TAT_{Step2} + V_{Step2}/r_{Load} \quad (11)$$

In this section, we analyze the total test time including tester loading time for Step1 and Step2. We can find the optimal grouping size w $(1 \leq w \leq N)$, which minimizes

$$T_{Step1} + T_{Step2} \quad (12)$$

by using common solver tools. However, there is a unknown parameter Pr{1bit error} in Eq.(12) which depends on the existence fault in the chip and its manifestation as an error. In the next section, we will do some experiments to show the relationship between error probability and optimal group size w, and propose a practical group size w.

5. Experimental Results

We have shown that the test time of error identification depends on the error probability. In Fig.4, we show the distribution of the error probability for a large industrial circuit which is obtained by simulating randomly selected 100 single stuck-at faults. The experimental circuit is a part of a SoC developed at NEC Electronics co. and details of the circuit are provided in Table 1.

Table 1. Experimental circuit

No. of gates	6M gates
No. of FFs	54505
No. of external ports	317
No. of Scan chains	65
Size of PG and SA	64 bit LFSR
No. of SAs	5
clock frequency of CUT	800MHz
clock frequency of tester	40MHz
bit rate of tester loading	140Mbps

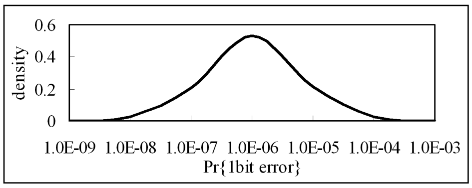

Figure 4. The distribution of error probability

As shown in Fig.4, the error probability is almost in the range of $10^{-8} < \Pr\{1\,bit\,error\} < 10^{-4}$, and typically near 10^{-6}.

We plot the total testing time including tester loading time using equations deduced in Section 4. The parameters reflect the experimental circuit shown in Table 1. Fig.5 shows the Step1, Step2 and total testing time as a function of group size w, to identify 200 errors which is enough error information for diagnosing scan based design [3-5]. Fig.5 shows that there is an optimal point of group size to minimize total testing time. In typical and low error probability cases, 5860bit is the optimal grouping size. The optimal grouping size for high error probability case may be as large as possible, i.e., no-grouping is needed. However, Fig.5 shows that when the group size is larger than 5000, which is around optimal solution for typical case, testing time is almost constant. Therefore, the solution of the optimal group size under typical error probability is also practically suitable for higher error probability case.

Therefore, we conclude that the optimal grouping size which minimizes testing time can be obtained by solving Eq.(12) under the assumption of Pr{1bit error} to be fairly low.

6. Conclusions

In this paper, we proposed a method for identifying erroneous responses for the BIST architecture in minimum testing time. Our approach is efficient even if the CUT test clock frequency is much higher than the tester frequency.

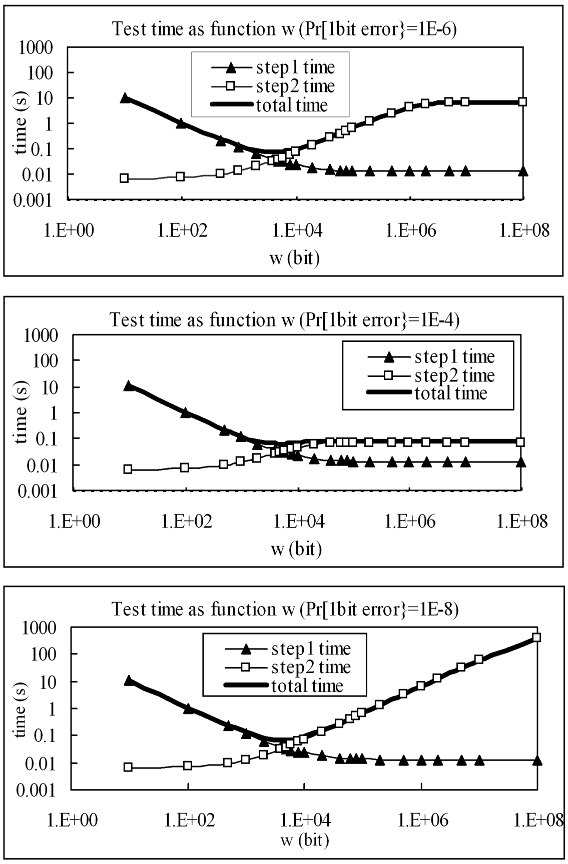

Figure 5. Test time as a function of group size (at typical,high and low error probability)

Our approach requires only multiplexer and masking circuit for diagnosis which is quite negligible hardware overhead.

We also proposed how to decide the size of pattern group to minimize testing time. We also take into account for tester loading time. The proposed equations to decide the optimal group size includes the error probability, however, the experimental results show that the group size which obtained under assumption of enough low error probability is also optimal for higher error probability cases. Experimental results also show that the test time by our method can be reduced by a factor of 10. Therefore, we can identify enough number of errors for diagnosis with minimum test application time with very little hardware overhead by using our proposed method.

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