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Compressing Test Data for Deterministic BIST Using a Reconfigurable Scan Architecture *

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Abstract — We present a new scan-based BIST technique, which is based on weighted scan enable signals and a scan forest architecture. A new testability measure is proposed to guide test pattern generation and produce patterns with fewer specified bits. This approach can effectively reduce the amount test data that needs to be stored on-chip. The proposed BIST method relies on a pseudo-random phase and a deterministic phase. The scan forest architecture is configured as a single scan tree for deterministic test vector application in the second phase. It is found that an LFSR with size equal to the maximum number of the specified bits in the deterministic patterns for the random-resistant faults is sufficient to encode deterministic vectors for the benchmark circuits. Experimental results for benchmark circuits demonstrate the effectiveness of the proposed method.

Keywords —Deterministic BIST, scan-based BIST, scan forest, testing with weighted scan enable signal.

I. Introduction

The test length for scan-based built-in self-test (BIST) is usually determined by the random-pattern-resistant (hard-to-detect) faults. Test length reduction for the hard-to-detect faults is therefore an important practical problem. Various techniques have been developed to handle this problem. The most popular techniques include: (1) weighted random testing [3]; (2) test point insertion [18]; (3) deterministic scan-based BIST. The test application time is also an important issue for scan-based BIST.

Weighted random testing refers to the application of test patterns derived using primary inputs with signal probabilities that are different from 0.5 [3]. This technique helps us to reduce test length, and thereby the test application time needed to reach high fault coverage. Weighted random testing schemes must store multiple sets of weights in most cases, and multiple test sessions are necessary [7]. Weighted random testing schemes with multiple test sessions require complex control logic [7].

It has been shown that the use of parallel scan chains alone may not be sufficient to obtain high fault coverage with low test time [3, 8]. A well-designed phase shifter (PS) has been shown to increase the fault coverage [15]. However, this approach typically requires a large number of (short) scan chains, as well as area overhead for the PS and a multiple-input signature-register (MISR). Usually, the number of stages in the pseudo-random test pattern generator (PRTG) is fixed, and a well designed phase shifter [15] can be used to avoid interdependences among the outputs of the PRTG. The storage requirement for a deterministic BIST method with a well-designed PS can however still be very large [8, 14, 16].

It is therefore necessary to design a more efficient pseudo-random test generator. It is well-known that weighted pseudo-random test pattern generation can increase fault coverage for pseudo-random testing. However, weighted random testing methods in use today apply weighted vectors only to the primary inputs. None of these methods that can generate weighted vectors for the pseudo-primary inputs without modifying the scan flip-flops.

Deterministic scan-based BIST schemes usually utilize the large number of unspecified bits in deterministic test vectors. As shown by Koenemann [10], deterministic test vectors can be encoded into LFSR seeds, whose size equals the maximum number of specified bits S_{max} in the deterministic test vectors plus 20. The requirement on the size of the LFSR can be reduced to $S_{max} + 4$ by using multiple primitive polynomials [5, 6]. Efficient test generation techniques have been presented to reduce the number of specified bits in the deterministic test vectors [6], and test vector concatenation has been proposed to encode multiple patterns with a single seed. Rajski *et al.* [16] improved encoding efficiency by using variant-length seeds and multiple primitive polynomials. Krishna, Jas, and Touba [11] proposed a new test encoding scheme based on the loading of seeds with size less than the LFSR size; this method incrementally modifies the next seed in the process of test application.

Recently, a test encoding scheme with multiple primitive polynomials and various ranks was proposed to compress deterministic test data [9]. Seed ordering and seed encoding were used to reduce storage requirement in [2], where the test vector concatenation technique was improved significantly. The states of the circuit in separate clock cycles, instead of the state after the shift cycles of separate test cycles, can be used to encode determini-tic test vectors. Li and Chakrabarty [13] proposed a reco

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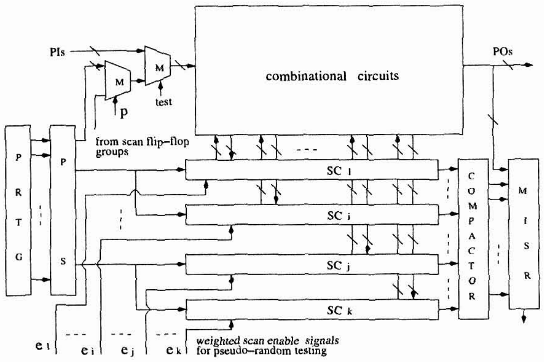

Figure 1: Weighted scan enable signals for scan-forest-based BIST.

urable scan architecture to improve the encoding efficiency of deterministic BIST, where the interconnections between the outputs of the LFSR and the inputs of the scan chains can be dynamically reconfigured.

In this paper, we propose a new scan-based BIST scheme based on the scan forest architecture and weighted scan enable signals. The proposed BIST method relies on a pseudorandom phase and a deterministic phase. The scan forest is reconfigured into a scan tree in the deterministic BIST phase. The proposed method applies different weights to the scan enable signals of all scan segments. The proposed pseudo-random testing scheme can significantly improve fault coverage in the first phase. A new testability measure is proposed to guide test generation such that test patterns with fewer specified bits are obtained. For all benchmark circuits, the proposed method is able to encode all deterministic vectors using an LFSR whose size is equal to the maximum number of specified bits in a test pattern.

The rest of this paper is organized as follows. The scan-BIST architecture based on a reconfigurable scan forest is described in Section 2. The new scan architecture using a scan forest and weighted scan enable signals is introduced in Section 3. A new testability measure is introduced to guide test generation for test vectors with fewer specified bits in Section 4. Experimental results are given in Section 5. Section 6 concludes the paper.

II. The Reconfigurable Scan Architecture for Deterministic BIST

In this section, we describe the scan-based architecture for the proposed two-phase BIST method. As shown in Figure 1, the scan forest architecture is used for pseudo-random testing in the first phase. Each stage of the phase shifter (PS) drives multiple scan segments, where all scan flip-flops at the same stage for all scan segments are driven by the same stage of the phase shifter. The test response compactor is an XOR gate network. Two scan segments (a_1, a_2, ..., a_n) and (b_1, b_2, ..., b_n) are connected to the same XOR gate if the scan flip-flop pairs (a_1, b_1), (a_2, b_2), ..., and (a_n, b_n) do not have any common combinational predecessor.

Unlike the conventional test-per-scan BIST scheme, each scan segment is driven by a separate scan enable signal. We use the set of weights $\{0.5, 0.625, 0.75, 0.875\}$ to control the scan enable signals. In the pseudo-random test-

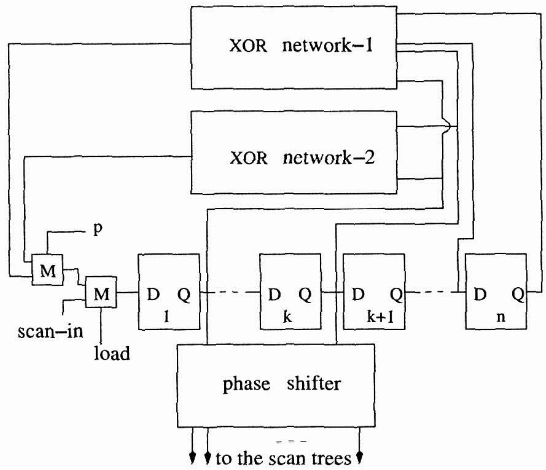

Figure 2: The linear-feedback shift-register design for the two phases.

ing phase, the primary inputs are directly driven by the phase shifter. Each of the primary inputs is driven by a scan flip-flop of a scan segment in the deterministic BIST phase. The primary inputs are also grouped with all the scan flip-flops. A primary input (PI) can be included into a scan flip-flop group if PI does not have any combinational successor with any of the scan flip-flops in the group. Let the scan flip-flops in the group be at the kth level of the scan tree. The PI in that group can be driven by any scan flip-flop at the $(k-1)$th level in the scan tree. This can be implemented by using a multiplexer for each primary input as shown in Figure 1, where the multiplexer is controlled by the signal p. The phase shifter is connected to the primary input when $p = 0$ (pseudo-random testing phase), and the primary input is connected to a scan tree when $p = 1$ (deterministic BIST phase).

Usually, a small LFSR is sufficient when a well designed phase shifter is adopted in the pseudo-random testing phase. In our method, a combination of a 24-stage LFSR and the phase shifter from [15] is used to generate test patterns in the pseudo-random testing phase. The size of the LFSR needed for deterministic BIST depends on the maximum number of specified bits for any deterministic test vector. While two different LFSRs can be used for the two phases, a composite LFSR design can be used as shown in Figure 2. The same signal p as the one presented in Figure 1 is used to switch between two XOR feeback networks. The XOR network-1 is used for the pseudo-random testing phase, while the XOR network-2 is used for the deterministic BIST phase. All seeds stored in the ROM are shifted in from the scan-in signal. The overhead needed to implement the LFSR with two polynomials involves only one additional XOR network and a multiplexer. Only a few two input XOR gates are needed if a primitive polynomial with very few terms is used to generate pseudo-random test vectors.

The phase shifter drives the scan trees and primary inputs only in the pseudo-random testing phase. The scan forest architecture is reconfigured to a single scan tree during the deterministic BIST phase, where all primary inputs are driven by some internal scan flip-flops in order to reduce the number of test inputs and the number of spec

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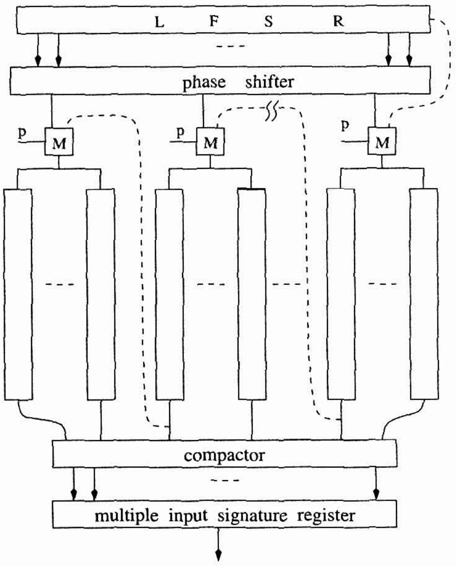

Figure 3: The reconfigurable scan architecture for pseudo-random testing and deterministic BIST.

bits in the deterministic test vectors for the hard faults. As shown in Figure 3, one extra multiplexer is inserted before the scan-in signal of each scan tree. The signal p is used for test phase selection, and it is the same as in Figure 1 and Figure 2. The pseudo-random testing phase corresponds to $p = 0$, and the deterministic BIST phase is used when when $p = 1$. The scan trees receive test signals from the phase shifter during the pseudo-random testing phase.

In the deterministic BIST phase, the scan tree receives test vectors from the scan-in signal of the rightmost scan tree; see Figure 3. The scan-in signal of the rightmost scan tree is connected to a stage of the LFSR directly in the deterministic BIST phase. The dashed lines shown in Figure 3 connect the scan-in signals of the scan trees with output of the last scan flip-flop in one of the scan segments in its right scan tree. The outputs of all scan segments are still connected to the compactor during the deterministic BIST phase; this offers additional flexibility for test encoding. The test responses of the previous test vector can be shifted out with only a few clock cycles (corresponding to the depth of the scan forest in the pseudo-random testing phase). For a single scan chain architecture, the number of clock cycles needed to shift out test responses of the previous deterministic test vector is much more—it equals the number of scan flip-flops in the circuit.

An effective seed encoding scheme is used here to reduce the storage requirements for the deterministic test patterns for the random-resistant faults. The test responses of each test vector are shifted out with k clock cycles (k is the depth of the scan forest). The test responses are captured again when the state of the scanned circuit is compatible with any other deterministic test vector.

III. Scan-Based BIST Using Scan Forest and Weighted Scan Enable Signals

The i-controllability $C'_i(l)$ ($i \in \{0,1\}$) of a node l is defined as the probability that a randomly selected input

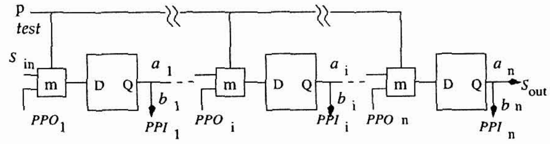

Figure 4: A scan segment with a weighted scan enable signal.

vector sets l to the value i. The observability $O'(l)$ is defined as the probability that a randomly selected input vector propagates the value of l to a primary output. The *signal probability* of a node is defined in the same manner as its 1-controllability measure.

In the scan-based architecture as shown in Figure 1, different weights $e_1, e_2, \ldots$, and e_k are assigned to the scan enable signals of the scan segments SC_1, SC_2, ..., and SC_k, respectively, where $e_1, e_2, \ldots, e_k \in \{0.5, 0.625, 0.75, 0.875\}$. We do not assign weights values less than 0.5 to the scan enable signals because we do not want to insert more capture cycles than scan shift cycles. We have developed an efficient method to select weights for the scan enable signals of the scan segments. The selection of weights for the scan enable signals is determined by the following testability gain function:

$$G = \sum_{l/i \in F} \frac{|C'_1(l) - C'_0(l)|}{O'(l)}, \tag{1}$$

where l/i represents the stuck-at i ($i \in \{0,1\}$) fault at line l. In Equation (1), F is the random-resistant fault set, defined as the set of faults whose detection probability is no more than 10 times that of the hardest fault [3]. Note that our method does not consider redundant faults according to the COP measure [4] when selecting weights. We attempt to minimize the testability gain function as given in Equation (1).

Figure 4 presents a scan chain with a weighted scan enable signal, where S_{in}, S_{out} and *test* are the scan-in signal, scan-out signal, and the scan enable signal of the scan chain, respectively. Initially, all pseudo-primary inputs are assigned signal probability 0.5, and the observability of the pseudo-primary outputs is set to $1/n$. Let p be the selected weight of the scan enable signal as shown in Figure 4. Then

$$C'_1(PPI_i) = p \cdot C'_1(a_{i-1}) + (1-p) \cdot C'_1(PPO_i). \tag{2}$$

The observability of PPO_i can be estimated as follows:

$$O'(PPI_i) = (1-p) \cdot O'(a_i), \tag{3}$$

$$O'(a_i) = 1 - (1 - O'(b_i)) \cdot (1 - O'(b_i)), \tag{4}$$

$$O'(b_{i-1}) = p \cdot O'(a_i). \tag{5}$$

We set the observability of the scan-out signal to 1. Even though the output of a scan segment is connected to the test response compactor, we can make the aliasing negligible by carefully connecting the scan segments to the XOR gates as described in Section II. We also have $O'(a_n) = 1$ and $C'_0(S_{in}) = C'_1(S_{in}) = 0.5$. Testability measures of the internal nodes and PPIs and PPOs can be calculated iteratively using the COP measures and Equations (2)-(5). We find that the testability measures fo~ ~ll nodes in the benchmakr circuits converge quickly.

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As shown in Figure 2, the BIST control logic assigns weighted signals to the scan enable signals. In functional mode, the extra pin *test* is assigned value 0. The circuit is set to the test mode when *test* is set to value 1. In this case, the selected weight is assigned to a scan chain. The scan chain works in the shift mode when the weighted scan enable signal is 1, and works under the capture mode when the scan enable signal is set to value 0. The weighted signals are produced by a phase shifter, the details of which is presented later in this section. Only one extra pin is necessary in the scan-based BIST design.

We assume that each scan segment uses separate scan enable signals. We assign weights from the set $\{0.5, 0.625, 0.75, 0.875\}$ to the scan enable signals of the scan segments. In the weight selection procedure, S is the scan segment set and SC is a specific scan segment. Initially, S contains all scan segments in the circuit. The procedure to determine weights can be described as follows: First, all scan segments use the regular *test-per-scan* scan enable signals. That is, scan enable signals are set to 1 in scan shift cycles and set to 0 in capture cycles. A test cycle for the original scan enable signals contains k scan shift cycles followed by one capture cycle, where k is the length of the longest scan segment. Our method selects a weight for the first scan segment scan enable signal to minimize the gain function. After the best weight has been selected for the first scan segment, we select aweight for the scan enable signal of the second scan segment that minimizes the cost function in Equation (1). For each scan segment, if no weight can be selected, we leave its scan enable signal as the one in conventional *test-per-scan* BIST scheme (the number of shift cycles is equal to the length of the scan segments, and a capture cycle follows). Continue the above process until appropriate weights have been chosen for all scan enable signals of the scan segments. Further details to select weights for the scan enable signals can be found from [20].

Different weights can be obtained by connecting two or more pseudo-random signals [3]. As shown in Figure 3, all weights are connected to a multiplexer which is controlled by the signal p. The selected weight is connected to the scan enable signal of the scan segment when $p = 0$ in the pseudo-random testing phase. The signal *test2* is connected to the scan enable signals of all scan segments during the deterministic BIST phase, where the scan forest is reconfigured as a scan tree (i.e., d shift cycles followed by a capture cycle, where d is the depth of the scan tree in the deterministic BIST phase).

IV. Testability Measure to Guide Test Pattern Generation with Fewer Specified Bits

All pseudo-primary inputs (PPIs) corresponding to the same scan flip-flop group are merged into a single PPI. As shown in Figure 1, each of the primary inputs shares the same PPI with the scan flip-flops in the same group. This technique reduces the number of test inputs, and it also reduces the number of specified bits in the deterministic test vectors for the hard faults left after the pseudo-random testing phase.

We next present another simple SCOAP-like testability measure to guide test pattern generation such that we obtain test vectors with even fewer specified bits. We introduce the following additional definitions. Let $RC_i(l)$ be defined as the minimum set of primary inputs (or pseudo-primary inputs) that have to be fixed to a logic value in order to set line l to value i, where $i \in \{0, 1\}$. The controllability $C_i(l)$ is defined as the minimum number of primary inputs (or pseudo-primary inputs) that must be assigned specified values in order to place control value $i \in \{0,1\}$ on line l. Let l be a primary input. We have

$$RC_1(PI) = RC_0(PI) = \{PI\}, \quad (6)$$
$$C_1(PI) = C_0(PI) = 1. \quad (7)$$

For an AND gate l with inputs A and B, we have

$$RC_1(l) = RC_1(A) \cup RC_1(B), \quad (8)$$
$$C_1(l) = |RC_1(l)|. \quad (9)$$

where $|RC_1(l)|$ is the size of the set $RC_1(l)$. We also have $RC_0(l) = RC_0(A)$ if $|RC_0(A)| < |RC_0(B)|$, $RC_0(l) = RC_0(B)$ if $|RC_0(A)| > |RC_0(B)|$. For an OR gate l with inputs A and B,

$$RC_0(l) = RC_0(A) \cup RC_0(B), \quad (10)$$
$$C_0(l) = |RC_0(l)|. \quad (11)$$

We have $RC_1(l) = RC_1(A)$ if $|RC_1(A)| < |RC_1(B)|$, $RC_1(l) = RC_1(B)$ if $|RC_1(A)| > |RC_1(B)|$, and

$$C_1(l) = |RC_1(l)|. \quad (12)$$

For a fanout s with branches $B_1, B_2, \ldots, B_k$, for $i \in \{0, 1\}$, and $j \in \{1, 2, \ldots, k\}$, we have:

$$C_i(B_j) = C_i(s).$$

The controllability calculation of the testability measure for other gates is similar. The function $RO(l)$ is defined as the smallest set of primary inputs (or pseudo-primary inputs) that need to be assigned specified values in order to propagate the fault effect at l either to a primary output or to a pseudo-primary output. The observability $O(l)$ is defined as the minimum number of primary inputs (or pseudo-primary inputs) that need to be assigned specified values in order to propagate the fault effect at l to either to a primary output or to a pseudo-primary output. For a primary output (or a pseudo-primary output) l, we have $O(l) = 0$ and $RO(l) = \emptyset$. Consider an AND gate l with inputs A and B, we have

$$RO(A) = RO(l) \cup RC_1(B), \quad (13)$$
$$O(A) = |RO(A)|. \quad (14)$$

Let l be the output of an OR gate with inputs A and B. We have:

$$RO(A) = RO(l) \cup RC_0(B), \quad (15)$$
$$O(A) = |RO(A)|. \quad (16)$$

Let s be a fanout stem with fanout branches B_1, B_2, $\ldots$, B_k. In this case, the following relationships hold:

$$O(F) = min(O(B_1), O(B_2), \ldots, O(B_k)).$$

The observability calculation for other gate types is sim- ilar. Let l/i be a single stuck-at fault at l for $i \in \{0$

We define the detectability $D(l/i)$ as the minimum number of primary inputs (pseudo-primary inputs) that need to be assigned specified values in order to generate a test pattern for the fault. Therefore,

$$D(l/i) = |RO(l) \cup RC_{\bar{i}}(l)|. \quad (17)$$

The above testability measure is used to guide test generation for test vectors with fewer specified bits. For example, any one of the inputs can be assigned to value 0 in order to set the output of a 2-input AND gate to value 0. Our method selects the input with less 0-controllability in this case. A fault effect at a fanout stem can be propagated along any fanout branch. Our method selects the fanout branch with the least observability.

A well-designed LFSR must be used in order to encode all deterministic vectors after the pseudo-random testing phase. A new scheme is presented to select a primitive polynomial with the minimum degree that can encode all deterministic test vectors for the hard faults. Let the maximum number of the specified bits of the deterministic vectors be S_{max}. This process continues until a primitive polynomial that encodes all deterministic test vectors is found. Experiments show that deterministic vectors for the hard faults for all benchmark circuits can be encoded by a primitive polynomial with degree equal to S_{max}.

The test responses of a deterministic test vector must be shifted out using L clock cycles, where L is the number of scan flip-flops in the longest scan chain. The reconfigurable scan architecture as shown in Fig. 3 offers flexibility for seed encoding for the deterministic vectors. The test responses captured by the scan flip-flops can be shifted out in only L_1 clock cycles, where L_1 is the depth of the scan forest in the pseudo-random testing phase. Our method uses up to 2^{15} shift cycles to cover more deterministic patterns between the period to load two seeds. The seed of a new test vector with the most number of specified bits is next selected to be loaded into the LFSR.

V. Experimental Results

The proposed BIST method has been implemented and experiments have been carried out using a Sun Blade2000 workstation. Table 1 presents results for the largest ISCAS89 benchmark circuits. The ATALANTA test generator [12] is used to generate deterministic test vectors of the hard faults. LFSR1 and LFSR2 denote the sizes of the LFSR in the pseudo-random testing and the deterministic BIST phases, respectively. Column 3 presents the fault coverage of the proposed pseudo-random test generation scheme after 500K clock cycles. The parameters NDTV, S_{max}, and ROM (bits) denote the number of deterministic test vectors, the maximum number of specified bits in the deterministic test patterns, and the number of bits that need to be stored on-chip in a ROM. The three columns with the *single scan chain* list the fault coverage, the maximum number of specified bits in the deterministic test patterns, and the number of deterministic test vectors for the hard faults after 10000 pseudo-random test patterns are applied. The CPU time to do fault simulation for the 10000 pseudo-random test patterns needs much more than 1 day for the largest ISCAS89 benchmark circuits, such as, s38417 and s38584 while the CPU time based on the weighted scan enable signal based test scheme is only about one hour. More pseudo-random test patterns for the pseudo-random test scheme with a single scan chain cannot get any fault coverage increment for almost all circuits. The last two columns in Table 1 show the performance of the deterministic test generator without using the new testability measure.

The results in Table 1 show that the scan forest architecture and the primary input merging scheme can significantly reduce the maximum number of specified bits in many cases. The proposed testability measure can further reduce the maximum number of specified bits in the test vectors to detect the hard faults for circuits s5378, s15850, and s38417. It is particularly noteworthy that the new testability measure can reduce the maximum number of specified bits in the deterministic test vectors from 86 to 44 for s38417. It is also seen that the proposed pseudo-random testing scheme with weighted scan enable signals can significantly increase the ifault coverage of the first phase for almost all circuits. We compare our method to a single scan chain a 10000 pseudo-random test vectors. It is shown that the proposed scan forest architecture with weighted scan enable signals can improve fault coverage significantly, especially for s9234 and s38417. Therefore, the proposed new pseudo-random testing scheme can reduce deterministic data volume considerably.

We next compare our method several previously publsihed methods, namely Koe. [10], MP [5], variant-length [16], SO [2] (seed ordering), FAST [14], partial [11], and VLMP [9]. Table 2 presents the sizes of the LFSRs and the test data volumes for all methods. The proposed method obtains the least test data volume for all circuits using LFSR with the least size. For every circuit, we are able to encode all deterministic test vectors for the hard faults using an LFSR of size equal to the maximum number of specified bits in the deterministic test vectors. We can attribute this observation to two reasons: (1) The pseudo-random test generator is highly efficient, and most hard faults that need more specified bits are detected in Phase 1; (2) selection of a proper primitive polynomial.

VI. Conclusions

We have presented a new BIST method that is based on a scan forest architecture and weighted scan enable signals for all the scan segments. The weighted scan enable signals are used to apply pseudorandom patterns in the first phase of the BIST procedure. The scan forest architecture is configured as a single scan tree in the second (deterministic) phase. A simple composite LFSR design is used to derive two different LFSRs for the two test phases. A new testability measure is proposed to generate deterministic test vectors with fewer specified bits for the hard faults. Experimental results have been presented for the benchmark circuits, and we have shown that the proposed method outperforms a number of competing BIST and compression techniques. We have also shown that for the bechmark circuits, the determinstic patterns can be generated using an LFSR whose size is equal to the maximum number of specified bits in these patterns.

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Table 1: Results obtained for the largest ISCAS89 circuits using the proposed BIST method.

circuits	LFSR 1 (size)	FC (phase1)	NDTV	S max	LFSR 2 (size)	loaded seed	encoded seed	ROM (bits)	single scan chain			no testability measure	
									FC	S max	NDTV	S max	NDTV
s5378	24	99.29	2	16	16	1	1	31	98.68	18	29	17	2
s9234	24	90.44	150	36	36	84	55	3849	84.69	51	318	36	150
s13207	24	98.35	27	18	18	4	13	267	96.72	22	97	17	27
s15850	24	95.12	152	34	34	64	88	3496	93.1	38	252	37	150
s38417	24	98.79	163	44	44	134	20	6196	94.34	86	954	86	168
s38584	24	96.44	44	54	54	20	23	1425	95.9	54	151	54	45

Table 2: Comparison of the Proposed Method with Previously Published Methods

circuits	SO [2]		VL [16]		FAST [14]		partial [11]		MP [5]		Koe. [10]		VLMP [9]		proposed	
	LFSR size	ROM (bits)	LFSR size	ROM (bits)	LFSR size	ROM (bits)	LFSR size	ROM (bits)	LFSR size	ROM (bits)	LFSR size	ROM (bits)	S max	ROM (bits)	LFSR size	ROM (bits)
s1423	50	450	—	—	—	—	—	—	—	—	—	—	—	—	**22**	**37**
s5378	61	427	—	—	29	493	38	502	27	726	38	1140	19	362	**16**	**31**
s9234	80	4560	—	4720	33	4674	81	5013	61	6923	81	11178	52	5162	**36**	**3849**
s13207	45	540	—	5784	53	2824	44	3008	24	3570	44	6908	30	1333	**18**	**267**
s15850	150	5250	—	6269	49	5092	58	5204	46	6528	58	9686	37	**2870**	**34**	3496
s38417	—	—	—	16797	81	23984	105	24513	91	24283	105	35700	92	21058	**44**	**6169**
s38584	200	3200	—	3901	77	2848	75	2942	70	3406	75	4650	54	2238	**54**	**1425**

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