IEEE Int. Test Conf., pp.1132-1133,1987.

Design for High-Speed Testability

Hideo Fujiwara

Department of Electronics and Communications
Meiji University
Kawasaki 214, Japan

Abstract

So far, many of the design-for-testability techniques have been investigated and developed mainly to ease the difficulty of test generation and application, focussing on DC functional testing. This paper suggests that design-for-testability techniques should also be investigated from a different point of view such as to cope with new and challenging problems of very high speed testing of future MOS or GaAs circuits.

Background

As the technology of the VLSI circuits advances with larger pin counts and higher speed of operation, automatic test equipment (ATE) systems are required to keep up with the fast speed as well as high pin counts. Although today's ATE systems seem to keep pace with current VLSI advances [1], with the increase of the use of very-high-speed integrated circuits (VHSIC's) such as high-speed MOS or GaAs VLSI circuits, much more powerful test equipment will be required in future for those very fast VLSI circuits [2]. Moreover, when accurate timing measurements are required for those VHSIC's, the ATE system will be faced with serious problems such as waveform distortion caused by transmission line reflections [3].

There are four types of testing for digital circuits: DC functional, DC parametric, AC parametric, and clock-rate functional. In DC functional testing, the circuit under test is exercised by applying test input patterns and analyzing the corresponding steady state outputs, i.e. only functional behavior of the circuit under test is tested. DC parametric testing is to measure such DC parameters as voltages and currents of the circuit under test at a low rate. AC parametric testing is to check time-related parameters such as rise and fall times, and propagation delay. Clock-rate testing is aimed to ensure that the circuit under test operates correctly at the maximum clock rate, i.e. to verify the time-related behavior of the circuit under test. High-speed testing is thus required for both AC parametric and clock-rate testing. Especially for VHSIC's, it is important to assure the maximum performance of circuits as well as to verify the time-related behavior at the maximum clock rate. Thus the need for high-speed testing of VLSI and VHSI circuits is as clear as day. This problem, though difficult, is unavoidable, and new technologies or approaches are expected to reach a solution. To cope with the problem that we are now faced with, the following three approaches would be considered.

(1) Further development of more powerful external test equipment which can properly test VLSI and VHSI circuits. Test equipment operating up to 1-3 GHz will be needed to test GaAs circuits [2]. This approach, though straightforward, might be very difficult and expensive to achieve.

(2) Designing IC's for testability so as to lighten the burden of external test equipment.

(3) Designing IC's for testability so as to require no external test equipment. Built-in self-test (BIST) approach belongs here.

Built-In Self-Test

A primary weakness of a conventional testing philosophy based on external testing, in which explicit test patterns are applied by test equipment external to the circuit under test, is that a technique is extremely constrained by limited access to internal points in the circuit under test. This implies some problems on test-pattern generation and application costs: (1) increasing time required to generate test pattern data, (2) the growing volume of test pattern data, and (3) the significant cost of ATE and the test application time. So far, many of the design-for-testability techniques have been investigated and

1987 International Test Conference
CH2347-2/87/0000/1132$01.00 © 1987 IEEE

developed mainly to reduce those costs or to ease those difficulties of test pattern generation and application, focussing on DC functional testing [4]. However, as mentioned above, new design-for-testability techniques are needed to cope with high-speed testing of VHSIC's as well as VLSI circuits. Built-in self-test (BIST) approaches, in which test patterns are applied internally to the circuit under test and their output responses are evaluated without the use of external test equipment, seem to be preferred over external testing and hold a good prospect for high-speed testing in future.

A BIST circuit requires that the functions of test pattern generation and output response evaluation are incorporated into the circuit under test. The most popular approach used for BIST is compact testing using pseudo-random patterns. Pseudo-random test patterns are usually generated by a linear feedback shift register (LFSR) and applied to the circuit under test. The output responses from the circuit under test are then compressed through another LFSR to form a signature. By analyzing the signature, one can determine whether the circuit under test is faulty or not [5].

BIST can alleviate the above-mentioned problems on test-pattern generation and application costs: Since test patterns are generated by a built-in random pattern generator, the time-consuming effort of test pattern generation can be removed from the design cycle. Since compact testing compresses response data and compares the signature only once, the difficulty of analysis and storage of huge amounts of test response data can be avoided.

Furthermore, BIST has another important advantage that the circuit under test is fed with random test patterns at the functional clock rate. Hence, it is possible to perform high-speed tesing using internal test equipment built in the circuit under test. BIST could provide an effective method of high-speed testing, including AC delay testing [6]. Since delay faults affect the timing operation of circuits, delay testing is performed to ensure that the circuit under test can operate correctly at the functional clock rate. BIST has the capability of this high-speed testing.

BIST approaches have been applied either partially or fully to commercial products such as microprocessors [7-8] and gate arrays [9] though focussing on DC functional testing. The current techniques on BIST, however, have some problems, e.g. the difficulty of achieving high fault coverage for sequential circuits due to randomness of test patterns, etc. Furthermore, there are some unsolved problems; BIST techniques for aiding in parametric testing or AC characterization, BIST techniques applicable to analog and hybrid circuits, etc. [10]. Further investigations are thus required to find out effective approaches capable of answering those difficult or unsolved problems. Considering the situation that testing with external test equipment has come up against a wall of "intractability" and is at a standstill, it would be natural to expect internal testing, i.e. BIST, instead of external testing. More research on BIST, including the extention of the concepts of BIST, should be done to cope with the above-mentioned problems in future.

Acknowledgments

The author wishes to thank Dr. T.Yamada of Meiji University and Mr. T.Kurobe of NEC Corp. for their valuable comments and suggestions.

References

[1] H.Bierman,"VLSI test gear keeps pace with chip advance," *Electronics/April 19*, pp.467-470, April 1984.

[2] J.Kirschling, "Testing GaAs devices with a digital in-circuit test system," *Proc. 1986 Int. Test Conf.*, pp.290-294, 1986.

[3] M.R.Barber and W.I.Satre, "Timing accuracy in modern ATE," *IEEE Design & Test of Comput.*, vol.4, no.2, pp.22-30, April 1987.

[4] H. Fujiwara, *Logic Testing and Design for Testability, The MIT Press*, 1985.

[5] E.J.McCluskey, "Built-in self-test techniques," *IEEE Design & Test of Comput.*, vol.2, no.2, pp.21-28, April 1985.

[6] J.Savir and W.H.McAnney, "Random pattern testability of delay faults," *Proc. 1986 Int. Test Conf.*, pp.263-273, Sept. 1986.

[7] J.Kuban and J.Salick, "Testability features of the MC68020," *Proc. 1984 Int. Test Conf.*, pp.821-826, 1984.

[8] P.P.Gelsinger, "Built in self test of the 80386," *Proc. ICCD-86*, pp.169-173, 1986.

[9] R.Lake,"A fast 20K gate array with on-chip test system," *VLSI Systems Design*, pp.46-55, June 1986.

[10] R.M.Sedmak, "Built-in self-test: Pass or fail?," *IEEE Design & Test of Comput.*, vol.2, no.2, pp.17-19, April 1985.