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Optimization of NoC Wrapper Design Under Bandwidth and Test Time Constraints

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Abstract

In this paper, two wrapper designs are proposed for core-based test application based on Networks-on-Chip (NoC) reuse. It will be shown that the previously proposed NoC wrapper does not efficiently utilize the NoC bandwidth, which may result in poor test schedules. Our wrappers (Type 1 and Type 2) complement each other to overcome this inefficiency while minimizing the overhead. The Type 2 wrapper uses larger area overhead to increase bandwidth efficiency, while the Type 1 takes advantage of some special configurations which may not require a complex and high-cost wrapper. Two wrapper optimization algorithms are applied to both wrapper designs under channel bandwidth and test time constraints, resulting in very little or no increase in the test application time compared to conventional TAM approaches.

1. Introduction

The NoC [1] provides abundant communication resources, which makes the traditional approach of adding extraneous Test Access Mechanism (TAM) [2, 3] overkill. Several research groups have published works on NoC test scheduling [4, 5, 6] utilizing the NoC as the test data transportation path from external testers to the CUTs. Test scheduling for the NoC router [6, 7] and crosstalk test of the interconnects [8] have also been discussed. In these approaches, each CUT is wrapped by an IEEE 1500 [9] compatible wrapper in order to provide isolation and access during the test application.

Many NoC architectures have been proposed such as SPIN [10], Æthereal [11, 12], SoCIN [13], NOSTRUM [14], QNoC [15], and HERMES [16]; all are based on a synchronous communication between nodes. Several other types of NoCs such as CHAIN [17], NEXUS [18], and ANoC [19] are based on Globally Asynchronous Locally Synchronous (GALS) communication. The copious NoC architectures highlight the growing interest in NoC as a next generation SoC interconnect.

With regard to the NoC's Design-for-Testability (DFT), the authors in [20] presented an architecture called ANoC-TEST, which targets the Asynchronous Networks-on-Chip (ANoC) [19]. In [21], the proposed NoC wrapper takes advantage of the guaranteed bandwidth and latency provided by the NoC to ensure test data integrity. Their experimental results showed that in terms of core test time, the proposed NoC wrapper is comparable to the TAM-based IEEE 1500 wrapper, and NoC-reuse [4, 5, 6] capable. However, due to the constraint of the parallel-serial conversion at the input port, the proposed wrapper requires much higher guaranteed bandwidth on the NoC than the actual rate of the test data loaded into the test wrapper. This is further explained in Sect. 4.2

In this paper, we are proposing two types of NoC wrappers based on the guaranteed bandwidth and latency. The wrappers complement each other in order to optimize the NoC bandwidth utilization and minimize the test application time. For a given bandwidth or a test application time constraint, the proposed wrapper optimization algorithm finds the optimum configuration using a binary search algorithm.

The rest of the paper is organized as follows: The NoC model and the IP core model are described in Sect. 2 and 3, respectively. In Sect. 4, a detailed description of the proposed NoC wrapper architecture is given. The wrapper optimization methodology is explained in Sect. 5. Some experimental results on selected benchmark circuits are given in Sect. 6. Finally, concluding remarks are offered in Sect. 7

2. NoC Model

The proposed wrapper utilizes the functional communication channel between a test source and a CUT. The delivery channel can be a dedicated path or a transparent virtual channel. The wrapper is topology independent; it can be used for any NoC architecture as long as minimum sustainable bandwidth and latency are guaranteed during the test application of the target CUT. The quality-of-service guarantees ensure that the test data are available at the CUT at the right time. In this paper, the Æthereal [11, 12] NoC is used to explain the wrapper design and optimization.

The Æthereal NoC routers [11] provide both guaranteed and best-effort services. The guaranteed throughput (GT) router guarantees uncorrupted, lossless, and ordered data transfer, and both latency and throughput over a finite time interval. It also implements a network interface (NI) [12]—NI kernel and NI shells—which connects the network routers to

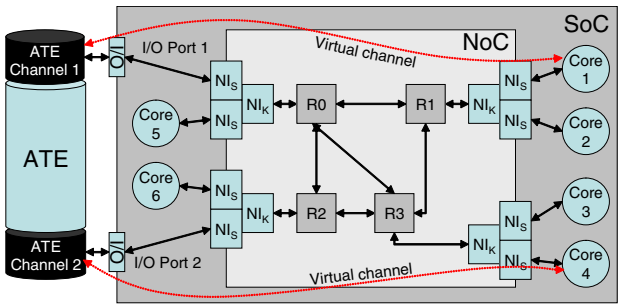

Figure 1. NoC model based on the Æthereal NoC

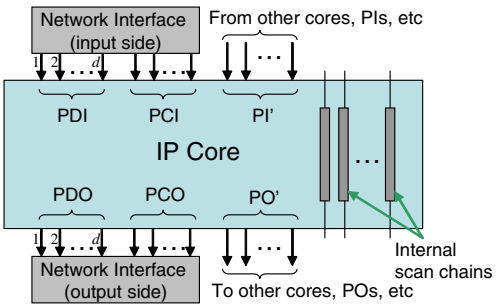

Figure 3. IP core model interfaced to the NI port

the IP cores by means of *shared-memory abstraction* (Fig. 1) utilizing a transaction-based protocol.

Figure 1 shows a NoC model based on the Æthereal architecture consisting of four GT routers $R0 - R3$. The NI supports multiple communication protocols required by the IP cores. Two of the NI shells are labelled *I/O port 1* and *I/O port 2*, which can be used to interface the external ATE ports to the NoC. Two virtual channels (VC) are shown connecting the ATE on port 1 to core 2 and the ATE on port 2 to core 3. Each VC is guaranteed a minimum bandwidth, $B^{vc}_{min} \leq min\{B^{i,j}_{max}\}$. The term $B^{i,j}_{max}$ represents the maximum link bandwidth between each pair of GT routers R_i and R_j along the VC path. If $B^{vc}_{min} < B^{i,j}_{max}$ for some link $R_i - R_j$, the remaining $B^{i,j}_{max} - B^{vc}_{min}$ can be allocated to other VCs in order to allow simultaneous test applications of multiple CUTs.

Figure 2 shows a simplified timing diagram of an AXI burst write transaction [22]. In order to reuse the NoC during test, the ATE needs to communicate with the CUT using the read/write transactions. Furthermore, the test methodology can be extended to reuse the embedded processors as test sources and sinks in place of the external ATE.

3. IP Core Model

IP core I/Os consist of primary inputs (PI), primary outputs (PO), scan inputs (SI) and scan outputs (SO). A subset of the PIs can be categorized into *primary data inputs* (PDI) and *primary control inputs* (PCI). Assuming that the CUT communicates with the NoC by means of the AXI protocol (Fig. 2), PDI would be made up of WDATA[31:0] signals, while PCI consists of ADDR[31:0], AVALID, DLAST, and DVALID signals. Some PO signals can also be categorized

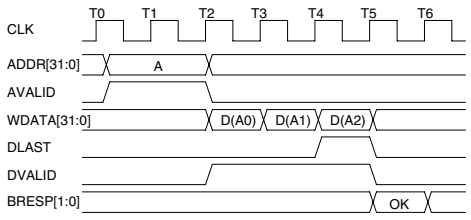

Figure 2. AXI burst-write transaction

into *primary data outputs* (PDO), consisting of RDATA[31:0] signals (not included in Fig. 2), and *primary control outputs* (PCO), consisting of BRESP[1:0] signals.

With the new classifications, core I/Os can be categorized as PDI, PDO, PCI, PCO, and other PI/POs which are not connected to the communication port of the NoC as shown in Fig. 3. The PDIs and PDOs are used to carry the test vectors from the ATE to the CUT, and the test responses from the CUT to the ATE, respectively. The PCIs and PCOs are needed to operate in the functional mode during the test application to ensure that the read/write transactions, by which the test data and responses are transmitted, execute properly. Since the CUT is not operating in the normal mode, the PCO signals must be generated by a wrapper controller. Special boundary cells proposed in [21] are used for PCOs to make the NoC operate in the normal mode to transfer the test responses. For all other PI/POs, the IEEE 1500 boundary cells are used.

4. NoC Wrapper Architecture

Core wrapper design for a TAM-based test architecture has been explained in [2, 3]. For a CUT, given k internal scan chains (ISC) of length, $l_1, l_2, ..., l_k$, i primary inputs, o primary outputs, b bidirectionals, and n_{sc} wrapper scan chains (WSC), the WSCs are formed while minimizing the maximum scan-in and scan-out depths. *Scan-in elements* consist of zero or more inputs, bidirectionals, and ISCs. *Scan-out elements* consist of zero or more outputs, bidirectionals, and ISCs.

Figure 4 shows $n_{sc} = 3$ for a CUT with $l_k = 8, 5, 5, 4$, and 3 flip-flops, $i = 8$, $o = 8$, and $b = 0$. The scan elements are optimally divided to form scan chains with *maximum scan-in depth*, $s_i = 11$, and *maximum scan-out depth*, $s_o = 11$, respectively; this is an optimal wrapper scan chain design [2]. As a result, the total test application time (TAT) can be calculated by equation (1), where n is the number of test vectors. For Fig. 4, the TAT is, $T_{TAM} = 12n + 11$ clock cycles.

$$T_{TAM} = (max\{s_i, s_o\} + 1) \times n + min\{s_i, s_o\} \quad (1)$$

When using TAMs as the delivery channel, the scan chain inputs and outputs are connected directly to the ATE input and output channels through the TAM wires. In order to reuse the

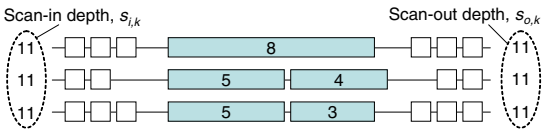

Figure 4. TAM-based wrapper scan chains made up of PI/PO boundary cells (square) and internal scan chains (rectangle)

NoC as the delivery channel, the scan chains are connected to the existing functional connections. Therefore, the test control and synchronization are no longer at the hand of the ATE, rendering the IEEE 1500 wrapper inadequate. Sections 4.1–4.3 explain how these problems are addressed in the proposed NoC wrappers.

4.1. Type 1 NoC Wrapper: Interfacing the PDI/PDO Ports to the Scan Chains

The proposed Type 1 wrapper uses the same approach as in [2, 3] when forming the wrapper scan chains which minimizes $max\{s_i, s_o\}$. For a given number of wrapper scan chains, n_{sc}, and the PDI bit-width, n_{pdi}, the number of PDI bits that can be used to carry the test data for each wrapper scan chain, n_{idbc}, is given by equation (2) [21]. To differentiate these PDI bits, those that can carry the test data are called *input data boundary cells*, IDBC (shaded black in Fig. 5). If $\hat{n}_{idbc} \neq 0$ (Eqn. (3)), some PDI bits cannot be used to carry the test data. A similar analysis can be done for the *output data boundary cells* (ODBC), resulting in equations (4) and (5).

$$n_{idbc} = \lfloor n_{pdi}/n_{sc} \rfloor \quad (2)$$

$$\hat{n}_{idbc} = n_{pdi} \; mod \; n_{sc} \quad (3)$$

$$n_{odbc} = \lfloor n_{pdo}/n_{sc} \rfloor \quad (4)$$

$$\hat{n}_{odbc} = n_{pdo} \; mod \; n_{sc} \quad (5)$$

For the CUT with 8-bit PDI/PDOs, and three wrapper scan chains (Fig. 5), $n_{idbc} = n_{odbc} = \lfloor 8/3 \rfloor = 2$ means that each wrapper scan chain is interfaced to two IDBC/ODBC cells. In addition, $\hat{n}_{idbc} = \hat{n}_{odbc} = (8 \; mod \; 3) = 2$ means that the remaining two PDI/PDO bits cannot be used to carry the test data. These unused PDI/PDO bits become part of the wrapper scan chain, with no extra functionality. Since $n_{pdi} = n_{pdo}$ in typical cases, the following discussion on the PDI on the input port also applies to the PDO on the output port.

During the test application, IDBC cells are loaded with the test data in one clock cycle, in the normal operation mode (refer to Fig. 5). The IDBC cells change into the test mode, during which the test data are serially shifted for two clock cycles to empty the contents into the scan chains. After completion, the IDBC cells change again into the normal mode to capture the next incoming data from the PDI port. This operation is controlled by a test controller which keeps track of the number of loads and shifts using counters [23].

For the NoC wrapper with a scan-in depth of nine (Fig. 5), after four repetitions of loads and shifts, the first eight bits of

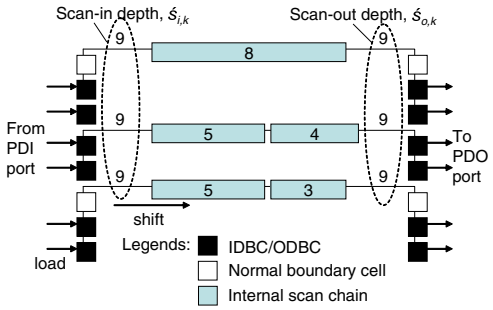

Figure 5. Type 1 NoC wrapper architecture

each scan chains are loaded with the test data. To load the last bit, the IDBC cells are loaded with new test data and a single shift clock is applied. However, before applying the capture cycle, the IDBC must also be loaded with valid test data. After the last single shift, only part of the IDBC cells contain valid test data. Reloading the IDBC data from the PDI port can corrupt the valid data currently in the IDBC cells.

To overcome this problem, the first $(s_i \; mod \; n_{idbc})$ shift cycles of every test pattern must shift in dummy bits into the scan chains. After the scan chains are completely loaded, another clock cycle is required to load the IDBC cells with valid test data before applying the capture cycle. Here, a formal definition of a new terminology based on this new scheme is given.

[***Definition***] The *Scan-in (scan-out) elements for the Type 1 NoC wrapper* consist of the unused IDBC (ODBC) cells, bidirectional cells, and internal scan chains (i.e. excluding all the IDBC/ODBC cells). The maximum scan-in and scan-out depths are denoted by $\acute{s}_i$ and $\acute{s}_o$, respectively (Fig. 5).

As a result of the new test scheme, the number of shift cycles required for the Type 1 NoC wrapper is summarized by equations (6) and (7). Equation (8) gives the total TAT, where the additional "+1" represents the final load of the IDBC data prior to the capture cycle. For the NoC wrapper in Fig. 5, $T_{Type1} = 11n + 9$ clock cycles, smaller than T_{TAM} based on equation (1).

$$\widehat{s_i} = \acute{s}_i + (\acute{s}_i \; mod \; n_{idbc}) \quad (6)$$

$$\widehat{s_o} = \acute{s}_o + (\acute{s}_o \; mod \; n_{odbc}) \quad (7)$$

$$T_{Type1} = (max\{\widehat{s_i}, \widehat{s_o}\} + 1 + 1) \times n + min\{\widehat{s_i}, \widehat{s_o}\} \quad (8)$$

4.2. Type 1 NoC Wrapper: Inefficient NoC Bandwidth Utilization

For a CUT with n_{sc} wrapper scan chains and f_m scan frequency, its scan rate/bandwidth is given by $B^{scan}_{Type1} = n_{sc} \times f_m$. As shown in the previous example (Fig. 5), some PDI bits cannot be used to carry the test data due to the Type 1 wrapper's input architecture constraint. In order to supply the test data to the CUT at B^{scan}_{Type1} rate, the required channel bandwidth on the NoC is given in equation (9). For the NoC wrapper in Fig. 5, the scan and required bandwidths are $3f_m$ bits-per-second (bps) and $4f_m$ bps, respectively.

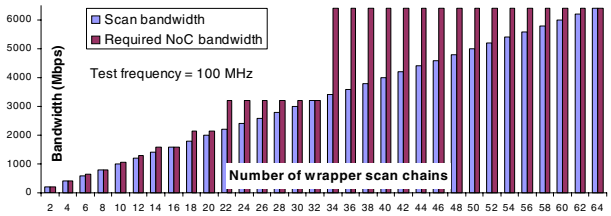

Figure 6. Scan rate and required bandwidth of a Type 1 NoC wrapper for p93791's Core 6 [25]

$$B^{req}_{Type1} = B^{scan}_{Type1} \times \frac{n_{pdi}}{n_{pdi} - \hat{n}_{idbc}} \quad (9)$$

Figure 6 shows the required bandwidth of the proposed Type 1 NoC wrapper (Fig. 5) compared to the actual scan bandwidth for an ITC'02 benchmark circuit. For some number of wrapper scan chains, the required bandwidth is almost twice that of the scan bandwidth. For these cases (i.e. $\hat{n}_{idbc} \neq 0$), the Type 1 NoC wrapper is inefficient in terms of NoC bandwidth utilization, similar to the NoC wrapper in [21]. For other cases, it is as efficient as the TAM-based wrapper while having the advantage of NoC reuse support capability with minimal area overhead. In the next section, an alternate wrapper architecture is proposed to overcome this limitation.

4.3. Type 2 NoC Wrapper: Optimizing the NoC Bandwidth Utilization

Section 4.2 has shown that the Type 1 wrapper is inefficient in terms of bandwidth utilization. The Type 2 NoC wrapper in Fig. 7, is designed to complement the Type 1 wrapper in this aspect. Extra load/shift registers are added to the PDI/PDO ports, similar to the buffer architecture in [23] for the reuse of the SoC's functional bus and the bandwidth matching registers in [24]. The load/shift registers translate the PDI bit-width into the number of wrapper scan chains using parallel-serial shift registers. As a result, the required NoC bandwidth matches the scan bandwidth. The TAT for the Type 2 NoC wrapper is also the same as the TAM-based wrappers in equation (1). This is achieved at the cost of area overhead of load/shift registers and a more complex control scheme to realize the bit-width conversion. Therefore, it is important that the Type 2 wrapper is used only when necessary. The next section looks at two proposed optimization schemes.

5. Optimization of the NoC Wrappers

Parallel core tests are performed according to an optimum test schedule under constraints. Figure 8 shows an example of a bin-packing optimization [2, 3], where a rectangle represents the bandwidth-TAT ratio for every CUT. For an optimal packing, the new entry into the bin must be selected properly, which means that all possible bandwidth-TAT combinations must be explored. For optimum results, both the available test

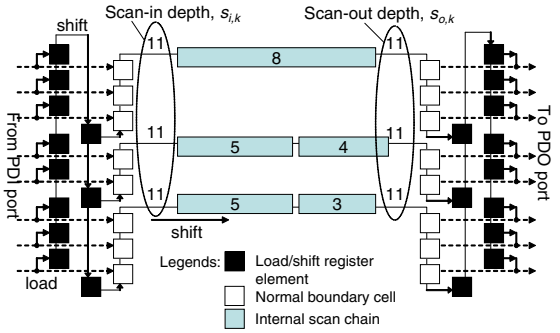

Figure 7. Type 2 NoC wrapper with an I/O interface

time (T_1 or T_2) and bandwidth (B_1 or B_2) must be considered.

The problem of optimizing the number of wrapper scan chains (n_{sc}) is formally defined as follows.

Ψ_B: Given a core with i functional inputs, o functional outputs, b bidirectionals, k internal scan chains of length $l_1, l_2, ..., l_k$, and a maximum bandwidth for the virtual channel between the core and the ATE, B_{max} bps, find the number of wrapper scan chains, n_{sc}, such that (i) the TAT is minimum, (ii) the required bandwidth, $B_{req} \leq B_{max}$, and (iii) n_{sc} is minimum subject to objectives (i) and (ii).

Ψ_T: Given a core as in Ψ_B, and a maximum TAT, T_{max}, find the number of wrapper scan chains, n_{sc}, such that (i) the required bandwidth, B_{req}, is minimum, (ii) TAT $\leq T_{max}$, and (iii) n_{sc} is minimum subject to objectives (i) and (ii).

A similar problem for a TAM-based wrapper design has been proven to be NP-complete in [2]. Therefore, heuristic algorithms are proposed to solve both Ψ_B and Ψ_T. Figure 9 illustrates graphically the search steps for Ψ_B (when $B_{max} = 5600\ Mbps$) for core 17 of the p93791 [25] benchmark circuit. Since the TAT and the required bandwidth are monotonic decreasing and increasing with respect to n_{sc}, respectively, binary search algorithms can be used to find the optimal value of n_{sc}. At each search step, the optimal wrapper scan chains which minimizes $max\{s_i, s_o\}$ are formed using the proposed algorithm in [2], described in Sect. 4. For the Type 1 wrapper, binary search takes place in steps 1 and 2 (refer to Fig. 9). In step 1, the maximum number of scan chains, n^{max}_{sc}, such that $B^{req}_{Type1} \leq B_{max}$ is located. In step 2, the search is restricted to $n_{sc} = [1, n^{max}_{sc}]$ to find the optimal

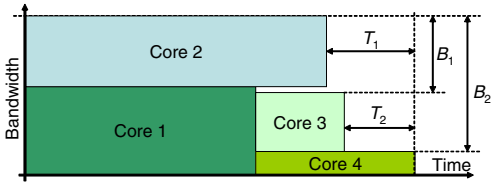

Figure 8. Test schedule optimization

Table 1. p93791's Core 6 [25] with 64-bit PDI/PDOs

n_{sc}	TAT (clock cycles)		%	n_{sc}	TAT (clock cycles)		%
	TAM [2, 3]	Type 1 NoC	increase		TAM [2, 3]	Type 1 NoC	increase
1	5,317,007	5,312,372	-0.09%	13	451,577	452,452	0.19%
2	2,658,613	2,656,404	-0.08%	14	451,358	451,576	0.05%
3	1,809,815	1,812,442	0.15%	15	447,197	448,072	0.20%
4	1,358,456	1,359,988	0.11%	16-19	341,858	342,076	0.06%
5	1,126,316	1,127,848	0.14%	20-21	337,478	338,134	0.19%
6	907,097	909,286	0.24%	22	333,317	333,754	0.13%
7	793,217	794,749	0.19%	23	231,478	231,258	-0.10%
8	679,337	680,212	0.13%	24-38	227,978	228,196	0.10%
9	674,957	676,489	0.23%	39-42	223,598	223,816	0.10%
10	565,457	566,770	0.23%	43-45	219,218	219,436	0.10%
11	561,077	562,171	0.19%	46	115,848	115,847	0.00%
12	455,738	455,956	0.05%	47-64	114,317	114,535	0.19%

value for n_{sc}. The progression of the binary search is graphically illustrated in Fig. 9. As a result, $n_{sc} = 22$ (Type 1) with a TAT of 65,098 clock cycles.

For the Type 2 wrapper, n_{sc}^{max} is directly calculated since B_{Type2}^{req} is a linear function of n_{sc}. Binary search in step 2 (similar to the Type 1 wrapper) results in $n_{sc} = 45$ with a TAT of 32,766 clock cycles. Clearly a better result for the Type 2 wrapper. In this case ($B_{max} = 5600\ Mbps$), the Type 1 wrapper is unable to utilize efficiently the allocated bandwidth because of the constraint in its I/O architecture.

A similar heuristic is implemented for Ψ_T and some selected cases for both algorithms are presented in Sect. 6.

6. Experimental Results

In order to evaluate the effectiveness of the proposed methodology, we have conducted experiments on three IP cores. Core 17 and core 6 (the largest of p93791 circuit) from the ITC'02 benchmark [25] are selected in order to offer comparisons with TAM-based approaches [2, 3]. Another IP core—an example core from [21]—allows some comparison with an NoC wrapper to be offered.

A TAT comparison between the proposed Type 1 NoC wrapper and TAM-based approaches is given in Table 1, for core 6 with $n_{pdi} = 64$ bits. In all cases, the differences are always less than 0.25%; the proposed Type 1 NoC wrapper does not incur noticable penalty on the TAT. In fact, some reductions are achieved for $n_{sc} = 1, 2$, and 23 scan chains. For the Type 2 NoC wrapper, the TAT is the same as the TAM-based approach because the added interface between the CUT and the NoC port does not constraint the scan chain design. The Type 2 wrapper's required bandwidth matches the scan bandwidth—an improvement due to the extra load/shift registers.

For the circuit from [21], the TAT is given in Table 2. Compared to the TAM-based wrapper, the proposed Type 1 NoC wrapper is better for smaller number of wrapper scan chains. For wider scan chains, the TAT's are about 3% longer. However, compared to the NoC wrapper design in [21][1], the Type 1 wrapper is always superior.

[1] Based on the corrected results obtained from the paper author because of reporting error in the original published literature.

Table 2. TAT comparison for the circuit in [21]

n_{sc}	TAM	Amory	Proposed		% increase	
	[2, 3]	[21][1]	Type 1	Type 2	Type 1 / TAM	Type 1 / Amory
1	5,532	5,532	5,300	5,532	-4.19%	-4.19%
2	2,771	2,771	2,660	2,771	-4.01%	-4.01%
3	1,858	1,858	1,780	1,858	-4.20%	-4.20%
4	1,396	1,451	1,428	1,396	2.29%	-1.59%
5	1,363	1,429	1,406	1,363	3.15%	-1.61%
6	1,363	1,418	1,395	1,363	2.35%	-1.62%

Further, we implemented the wrapper architecture proposed in [21] and compared the results (Table 3) for the a larger IP core (core 6 of p93791). The TAT and the required bandwidth, B_{Amory}^{req}, (column 3) are obtained for selected n_{sc} (column 1). Using $B_{max} = B_{Amory}^{req}$ (column 4) as input to Ψ_B, the corresponding n_{sc}, B_{Type2}^{req}, and TAT for the proposed Type 2 wrapper are obtained. Using at most the bandwidth required by [21], the proposed wrapper gives shorter TATs. For $n_{sc} = 24$ scan chains (last row), [21] requires 33% more bandwidth to obtain a comparable TAT.

Table 4 compares the Type 1 and Type 2 wrappers when Ψ_B and Ψ_T are applied. For $B_{max} = 1700\ Mbps$, both wrappers result in similar performance—a slight advantage for Type 1 in terms of area overhead. At $B_{max} = 3000\ Mbps$, Type 2 is clearly the winner, with only 0.8% bandwidth overhead to achieve 32.5% TAT reductions. For $T_{max} = 7000$, Type 2 requires 31% smaller bandwidth with less than 0.7% TAT overhead. On the other hand, at $T_{max} = 200000$, Type 1 wrapper is superior due to its minimal wrapper hardware overhead. The results illustrate the tradeoffs between the two types of NoC wrappers for a given constraint, which can be explored during the test schedule optimization.

7. Conclusion

We have proposed two versions of the NoC wrapper that requires minimal overhead on the test application time and area overhead. The previously proposed wrapper design did not handle the problem of inefficient bandwidth utilization. In this paper, we have proposed two heuristics that find the optimal wrapper design for a given maximum bandwidth or maximum test application time—important for test schedule optimization.

Table 3. TAT comparison with [21] (Core 6)

Amory [21]			Proposed (Type 2)				
n_{sc}	TAT	B_{req}	B_{max}	n_{sc}	B_{req}	TAT	%incr. TAT
11	562,172	1,280	1,280	12	1,200	455,738	-18.9%
15	448,073	1,600	1,600	16	1,600	341,858	-23.7%
22	333,755	3,200	3,200	24	2,400	227,978	-31.7%
24	228,416	3,200	3,200	24	2,400	227,978	-0.2%

Table 4. Selected optimization results (Core 17)

	Given:	Type 1			Type 2		
Ψ_B	B_{max} (Mbps)	n_{sc}	B_{req} (Mbps)	TAT	n_{sc}	B_{req} (Mbps)	TAT
	1,700	15	1,600	97,648	15	1,500	97,215
	3,000	21	2,133	96,129	23	2,300	64,882

	T_{max}	n_{sc}	B_{req} (Mbps)	TAT	n_{sc}	B_{req} (Mbps)	TAT
Ψ_T	70,000	22	3,200	65,098	22	2,200	65,530
	200,000	8	800	193,128	8	800	192,912

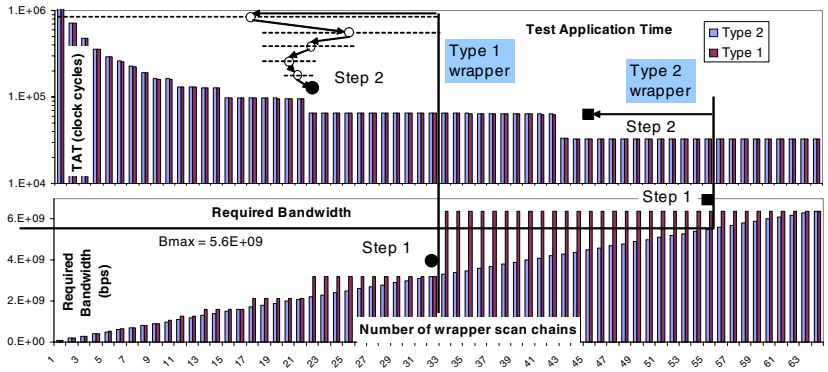

Figure 9. Optimization of NoC wrapper design for a given B_{max}. In step 2 (Type 1), the dotted lines represent the search space which halves in every progression of the binary search

The proposed wrapper does not incur large test time overhead (against TAM-based designs) for the same number of wrapper scan chains (about 3% for a very small circuit, and less than 0.25% for larger circuits). The wrappers scale well for large circuits. The advantage of the proposed wrapper is that NoC reuse is possible with only small test time overhead. With additional allowances on the area overhead, the proposed wrapper (Type 2) can efficiently utilize the NoC bandwidth with zero overhead on the test application time.

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