Scan Testing for Complete Coverage of Path Delay Faults with Reduced Test Data Volume, Test Application Time, and Hardware Cost

Dong Xiang
School of Software,
Tsinghua University,
Beijing 100084, China
dxiang@tsinghua.edu.cn

Krishnendu Chakrabarty
ECE Dept.,
Duke University
Durham, NC 27708, USA
krish@ee.duke.edu

Dianwei Hu
CS Dept.,
Tsinghua University
Beijing 100084, China
hdw@mails.tsinghua.edu.cn

Hideo Fujiwara
Grad. Sch. of Inf. Sci.,
NAIST, Ikoma
Nara 630-0101, Japan
fujiwara@is.naist.jp

Abstract

A new scan architecture, called enhanced scan forest, is proposed to detect path delay faults and reduce test stimulus data volume, test response data volume, and test application time. The enhanced scan forest architecture groups scan flip-flops together, where all scan flip-flops in the same group are assigned the same value for all test vectors. All scan flip-flops in the same group share the same hold latch, and the enhanced scan forest architecture makes the circuit work in the same way as a conventional enhanced scan design. The area overhead of the proposed enhanced scan forest is greatly reduced compared to that for enhanced scan design. A low-area-overhead zero-aliasing test response compactor is designed for path delay faults. Experimental results for the ISCAS benchmark circuits are presented to demonstrate the effectiveness of the proposed method.

I. Introduction

Path delay faults can detect many defects that escape detection by test sets that target only single stuck-at fault tests [**?**]. The detection of a path delay fault requires the application of pairs of test patterns. However, it is difficult to use standard scan design for at-speed application of arbitrary pairs of test patterns; hence it is difficult to obtain complete path delay fault coverage. Pomeranz and Reddy [9] proposed test generation and test application techniques for at-speed testing of delay faults. Savir and Patil proposed a model to analyze skew-load scan-based transition test [10] . Liou et al. proposed an effective two-phased multiple-clocked schemes to improve delay fault testing [7]. Lin et al. proposed new techniques for at speed scan testing that can be applied with internal PLLs [8]. Wang and Chakradhar proposed a test point insertion technique to improve the quality of transition fault testing in the standard scan designed circuits [11]. Girard et al. [4] handled scan-based BIST of delay faults in sequential circuits. Datta et al. [2] proposed a tri-state scan architecture by using a tri-state buffer driver to replace the buffer driver of each scan flip-flop, which can store the other bit of a test pair at the scan flip-flops.

In order to apply arbitrary pattern pairs, each scan flip-flop in the circuit can be implemented by modifying a scan flip-flop to an enhanced scan flip-flop [3]. A hold latch must be inserted at the output of each scan flip-flop in order to implement an enhanced scan flip-flop [3]. Such a design is seldom used in practice due to high area overhead. An optimization algorithm was presented in [1] to minimize the number of enhanced scan flip-flops so as to obtain the required level of delay fault coverage. To reduce area overhead, broadside or skewed-load testing are typically used in practice, but since the launch pattern is obtained either through the scan path or through the circuit, the fault coverage is often inadequate for these methods.

In addition to fault coverage and area overhead, test data volume and test application time are also important considerations for delay testing. We present a new path delay test technique that provides complete coverage with less area overhead than enhanced scan, as well as reduced test data volume and test application time. The proposed method is based on an enhanced scan forest architecture, where scan flip-flops are grouped together. All scan flip-flops in the same group are assigned the same value for all test vectors. All scan flip-flops in the same group share the same hold latch, and the enhanced scan forest architecture makes the circuit operate in the same way as a conventional enhanced scan design. A low-area-overhead zero-aliasing test response compactor is designed for path delay faults. The proposed technique can addresses test application issues for both robust and non-robust tests.

II. Preliminaries

Let a path $p = g_1$-g_2- ... -g_n be a path in the circuit under test, where g_1 and g_n are the source (a primary input or a pseudo-primary input) and the sink (a primary output or a pseudo-primary output) nodes, respectively. The off-inputs are the inputs of g_i, $1 \leq i \leq n$, that are not on the path p. The path p has a path delay fault if the propagation time for a rising or falling transition through the path exceeds a maximum threshold. Definitions of robust and non-robust pairs of test patterns for path delay faults can be found in [6].

The scan forest was proposed recently to reduce test application time and test data volume, and to compact test responses for single stuck-at faults. A generic architecture of a scan forest is presented in Figure 1 [12], where a scan-in signal drives a number of scan segments simultaneously. The scan flip-flops at the same level in any given scan tree are as-

1081-7735/07 $25.00 © 2007 IEEE
DOI 10.1109/ATS.2007.20

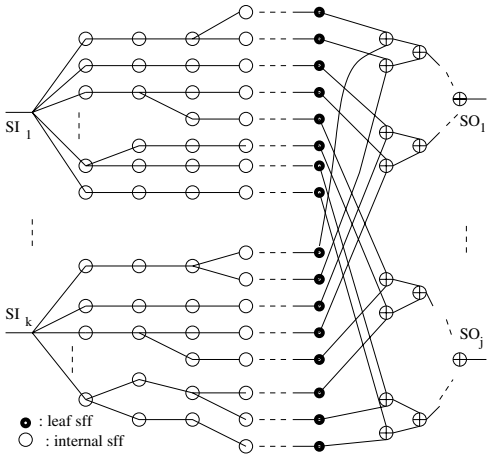

Figure 1. The scan forest scan architecture [12].

signed the same value for all test vectors without any loss of fault coverage. Only the leaf scan flip-flops are connected to the XOR-trees to compact test responses without any ATPG loss.

Delay fault testing is based on pairs of test patterns, and the circuit has to be clocked at-speed after each pair of patterns is applied. The circuit can be designed with enhanced scan flip-flops that can store two bits of a test pair (V_1, V_2) in order to apply an arbitrary test pair. For the conventional enhanced scan architecture, a hold latch is inserted into the output of each scan flip-flop. The initial pattern of a test pair is applied to the circuit and stored in the hold latches first, and then the second vector is serially shifted into the scan chain. Let nff and vec be the number of scan flip-flops in a scan chain and the number of test vector pairs, respectively. The number of clock cycles required to apply all test pairs can be estimated as follows:

$$TAP = vec \cdot (2 \cdot nff + 1) + nff - 1. \quad (1)$$

However, the enhanced scan design suffers from high area overhead. This makes it hard to use it in practice. The test application time, test stimulus data volume and test response data volume for enhanced scan design must be reduced in order to make it practical.

III. Enhanced Scan Forest for Path Delay Fault Testing

We propose a new scan architecture for path delay faults, which can effectively reduce test application time, test stimulus data volume, and test response data volume with acceptable area overhead. Figure 2 presents the new scan architecture called enhanced scan forest, where only a part of the scan element is inserted in a hold latch. This scan architecture is proposed here for path delay fault testing with compressed test stimulus test data, reduced test application time, and compacted test responses. The enhanced scan architecture of Figure 2 is an extended version of the scan forest presented in Figure 1. The area overhead for the new scan architecture is much less compared to conventional enhanced scan design, where a scan-in signal drives several scan segments. A number of scan flip-flops are assigned identical values for all test pairs, which are placed at the same level of the same scan tree. Only a single hold latch is used for all scan flip-flops at a given level in the same scan tree as shown in Figure 2. The routing overhead can be reduced greatly when grouping scan flip-flops because of the flexibility provided by the enhanced scan forest architecture. The extra interconnections between a hold latch and the extra multiplexers at the same level of a scan tree incur some routing overhead. The hold latch can be inserted into any scan flip-flop at the same level of a scan tree in order to reduce routing overhead. All other scan flip-flops with no hold latch connect to an extra multiplexer. The leaf scan flip-flops of the enhanced scan forest architecture are connected to the XOR trees for the compaction of test responses.

The test application scheme for the enhanced scan forest is as follows: Apply the initial pattern of a test pair from the scan-in signal to all scan trees in parallel until all scan flip-flops get their corresponding values of the initial pattern. All hold latches are deactivated during scan shift cycles of the initial pattern. The initial pattern is transferred to all hold latches by activating all hold latches simultaneously at the last shift cycle while the stimulus bits are applied at the primary inputs (PIs). The signal hold is then deactivated in order for all hold latches to keep the initial pattern when the stable vector V_2 is applied to the scan trees in parallel. All scan flip-flops are disabled when the stable pattern V_2 has been applied to the enhanced scan forest. At this point, the hold latches are activated and the initial pattern is applied to the circuit simultaneously, while the stable pattern is transfered to the hold latches at the end of the cycle. Simultaneous deactivation of the hold signals of the hold latches and application of the PI bits corresponding to V_2 provides the transition caused by $V_1 \rightarrow V_2$ at the inputs of the combinational logic. The circuit is set to normal mode for exactly one rated clock period to capture the combinational output at the flip-flops. The primary outputs are observed directly, and the internal states are captured at the flip-flops are scanned out when the first pattern of the next vector pair is shifted in. The above process is continued until all test pairs have been applied.

Let d and vec be the depth of the enhanced scan forest and the number of test vector pairs, respectively. The number of clock cycles TAP required to apply all test pairs with the enhanced scan forest is as follows:

$$TAP = vec \cdot (2d + 1) + (d - 1). \quad (2)$$

where two test vectors of each test pair are applied to the scan architecture serially. The control signals for the hold latch and the extra multiplexer are shown in Figure 3. The hold latch takes the value at its input when the signal *hold* is set to 1, and retains its value when the signal *hold* is set to 0. The output of the extra multiplexer selects the output of the hold latch when the hold latch is deactivated or the extra input x_1 is set to 1; otherwise, it selects its predecessor scan flip-flop. Each scan flip-flop has an inserted multiplexer. The data

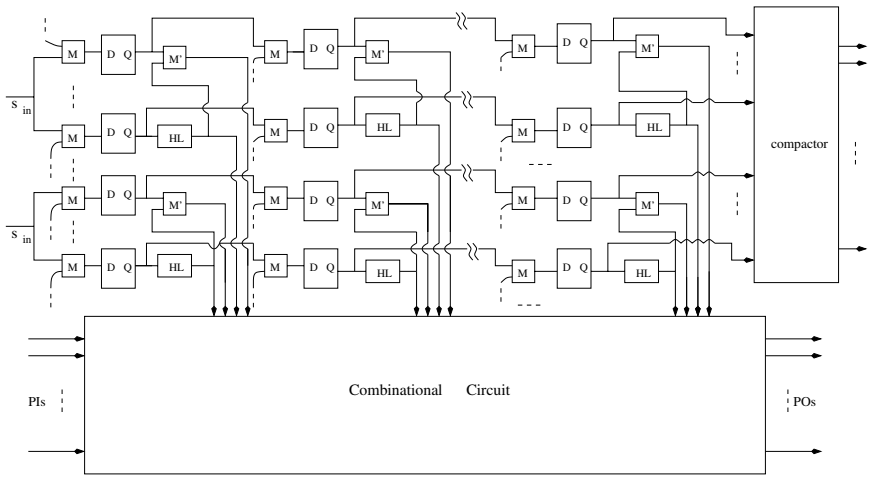

Figure 2. The enhanced scan forest architecture for path delay faults.

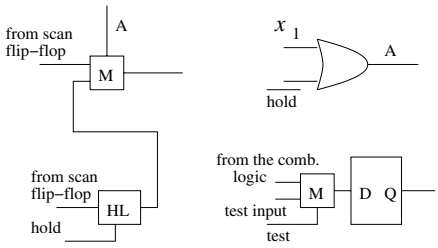

Figure 3. Extra control signals for the enhanced scan forest.

input D of a scan flip-flop selects test input when the circuit is set to the test mode (*test* is assigned value 1).

IV. Techniques for Test Stimulus Data Reduction

Two separate techniques are used here to reduce test stimulus data volume: (1) Enhanced scan forest construction, and (2) dynamic test compaction. For the enhanced scan forest, a number of scan flip-flops are assigned the same values for all test pairs; therefore, the test stimulus data volume can be reduced greatly if the number of test pairs does not increase much a consequence. The enhanced scan forest can greatly reduce the number of test inputs. The size of the test set can be reduced using test compaction schemes presented in [13]. We next show that the enhanced scan forest has no adverse impact on path delay fault testability.

Theorem 1 *Let* $\{(f_{1,1}, f_{1,2}, \ldots, f_{1,n}), \ldots, (f_{k,1}, f_{k,2}, \ldots, f_{k,n})\}$ *be the scan flip-flop groups in the enhanced scan forest circuit, where scan flip-flops in each group do not have common combinational successor in the original circuit, the enhanced scan forest does not make any robustly testable or non-robustly testable path untestable.*

Proof: Let the source node of a path p be $f_{i,j}$, $i \in \{1, 2, \ldots, k\}$ and $j \in \{1, 2, \ldots, n\}$, and all scan flip-flop groups be merged in the test circuit with the enhanced scan forest design. As for a non-robustly testable path p, each of the off-path line should still be assigned the sensitization value for the 3-valued system $\{0, 1, \times\}$. Justification of all off-path line assignments does not have any signal requirement on any other fanout branch $f_{i,l}$ for $l \neq j$ (they are pseudo-primary inputs in the original circuit) because $f_{i,1}, f_{i,2}, \ldots, f_{i,n}$ do not have any common combinational successor. Also justification of the off-path assignments can have signal requirement on at most one of the scan flip-flops in each group because of the same reason. Therefore, path p is still non-robustly testable in the enhanced scan forest designed circuit. Similarly, any robustly testable path p in the original circuit is still robustly testable in the enhanced scan forest designed circuit. The only difference is that for each of the off-path assignments (l, v), v is one of the 10 values in a 10-valued logic system [13]. ∎

A greedy procedure is used to group scan flip-flops in the circuit. Each scan flip-flop keeps a list of primary outputs or pseudo-primary outputs that can be reached from it. Two scan flip-flops have any common successor if and only if they have any common reachable primary output or pseudo-primary output. Two scan flip-flops cannot be included into the same group if they reach a common primary output or pseudo-primary output. The subcircuit that can be reached from the same pseudo-primary input is traversed only once using the above scheme. We construct the enhanced scan forest for test stimulus compression and the XOR trees for test response compaction concurrently. Effective dynamic test compaction techniques are used to reduce the number of test pairs for robust and non-robust path delay fault test generation based on the SPC test generator [13], which can also greatly reduce test stimulus test data volume.

V. Test Response Compaction for Robust Tests and Non-Robust Tests

Test response compaction for non-robust delay testing and robust delay testing should be dealt with separately. An XOR tree with a single output is used to compact test responses

for non-robust delay testing. All primary outputs and the leaf scan flip-flops of the enhanced scan forest are connected to the XOR tree as shown in Figure 4. The test response data volume can be reduced to $vec \cdot d$ using the test compactor as shown in Figure 4, where vec is the number of non-robust test pairs and d is the depth of the enhanced scan forest. The test response volume for non-robust delay testing can be reduced drastically compared with that of the original enhanced scan design with a single scan chain. The test response data volume of the enhanced scan design with a single scan chain is $vec \cdot (\#sff + \#pos)$, where vec, $\#sff$, and $\#pos$ are the number of test vector pairs, the number of scan flip-flops, and the number of primary outputs in the original circuit. The following lemma proves that the proposed test response compactor does not introduce any aliasing for non-robust delay testing.

Lemma 1 *Without loss of generality, consider a test pair without any don't-cares. (Don't-care bits can be mapped to 1s and 0s before test application.) All primary outputs and scan-out signals can be merged into a single output as shown in Figure 4 with no aliasing for non-robustly-testable path delay faults.*

Proof: As shown in Figure 4, all leaf scan flip-flops of the scan segments in the enhanced scan forest and the primary outputs are connected to the XOR tree with a single output. Therefore, only a single output receives test responses for non-robust test pair application. As shown in Figure 5, the bold-faced lines present a non-robustly testable path. The sensitization condition for an off-path line of an XOR gate for non-robust test is any specified value. Therefore, the non-robustly testable path does not have any signal requirement on line d. Therefore, the non-robustly testable path is still non-robustly testable after passing the XOR gate because any test pair does not contain any don't care. Therefore, we conclude that the test response compaction structure as presented in Figure 4 does not make any non-robustly testable path non-robustly untestable. ∎

As for test response compaction for robust delay testing, two scan segments $(v_1, v_2, \ldots, v_k)$ and $(v'_1, v'_2, \ldots, v'_k)$ can be connected to the same XOR tree if (v_1, v'_1), (v_1, v'_1), ..., and (v_1, v'_1) do not have any common combinational predecessor. The following theorem shows that a test response compactor that meets the above condition introduces no aliasing for robust delay fault testing.

Theorem 2 *A test response compactor, in which two scan segments $(v_1, v_2, \ldots, v_k)$ and $(v'_1, v'_2, \ldots, v'_k)$ can be connected to the same XOR tree if (v_1, v'_1), (v_1, v'_1), ..., and (v_1, v'_1) do not have any common combinational predecessor, introduces no aliasing for robust path delay testing.*

Proof: As shown in Figure 6, two leaf scan flip-flops of two scan segments are connected to the same XOR tree. Without loss of generality, let us consider a robustly testable path with a sink node v_1. Another input v'_1 as shown in Figure 6 must be assigned $s0$ or $s1$ in order to generate a robust test for the original path. Justification of the assignment $(v'_1, s0)$ or $(v_1, s1)$ does not have any conflict with the assignments

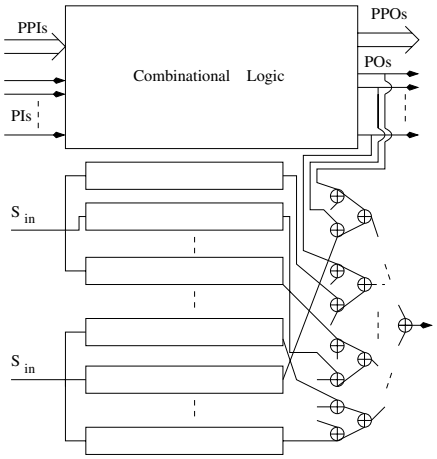

Figure 4. Test response compaction for non-robust testing of path delay faults.

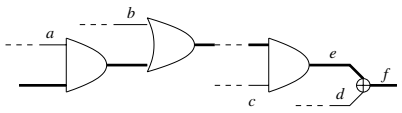

Figure 5. An illustration of the sensitization conditions for non-robust testing of path delay faults.

to generate a robust test of the original path because v'_1 does not have any common combinational predecessor with v_1 in the combinational part of the circuit according to the premise. Therefore, the robustly testable path is still robustly testable in the circuit with the test response compactor. ∎

Let a robust test pair contain no don't-care. It is easy for one to ask the following question: Is it possible to achieve zero-aliasing robust delay fault testing using the test response compaction architecture presented in Figure 4 ? Certainly, the answer is no. The reason is that it is possible to get a conflict assignment when justifying of the off-path input assignments of an XOR or XNOR gate. The off-path lines of an XOR or XNOR gate must be assigned $s1$ or $s0$ in order generate a robust test for a path in the circuit with the test response compactor as shown in Figure 4.

The test response compactor does not introduce any aliasing; however, it can affect the size of the test set. Another matrix $pred()$ is defined to group the scan flip-flops for the test response compactor like $succ()$ presented in Section 5. We define $pred(i, j) = 1$ if scan flip-flops i and j have a common combinational predecessor. The matrix $pred()$ can be obtained from $succ()$.

We call two scan segments $(v_1, v_2, \ldots, v_d)$ and $(v'_1, v'_2, \ldots, v'_d)$ are compatible if each pair of scan flip-flops (v_1, v'_1), (v_2, v'_2), ..., (v_d, v'_d) do not have any common combinational predecessor. Two scan segments $(v_1, v_2, \ldots, v_d)$ and $(v'_1, v'_2, \ldots, v'_d)$ can be connected to the same XOR tree if they are compatible, where $v_1, v_2, \ldots, v_d$ and v'_1, v'_2, ...,

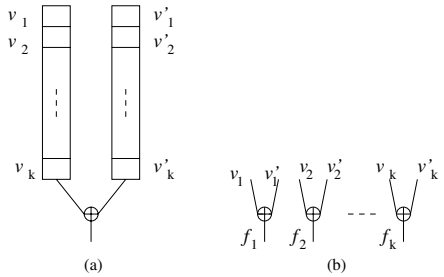

Figure 6. Test response compaction for robust testing of path delay faults: (a) connecting two scan segment to the same XOR tree, and (b) the test circuit after adding the test response compactor.

v'_d are scan flip-flops, and v_d and v'_d are leaf scan flip-flops. It is sufficient for the scan flip-flop pairs to meet only the test response compaction condition if two scan segments are driven by different scan-in signals. Two segments driven by the same scan-in signal can also be compatible. As for two scan segments $(v_1, v_2, \ldots, v_d)$ and $(v'_1, v'_2, \ldots, v'_d)$ driven by the same scan-in signal, they are compatible if scan flip-flop pairs (v_1, v'_1), (v_2, v'_2), …, (v_d, v'_d) meet the test signal condition and the test response compaction condition simultaneously. That is, any pair of the scan flip-flops do not have any common combinational successor or predecessor. Our method tries to first combine as many as possible compatible scan segments as possible. It is better to construct compatible scan segments in different scan trees. All remaining scan flip-flops can be connected to one of the scan segments based on the compatible scan segment condition. Two primary outputs can also be connected to the same XOR tree in order to reduce the test response data volume if they do not have any common combinational predecessor.

The average size of the scan flip-flop groups at each level of the scan trees determines the amount of test data compression. As for the test response compaction ratio, it is determined by $d \cdot n_{out}$, where d is the depth of the scan trees and n_{xor} is the number of XOR trees plus the number of merged primary outputs. The average size of the scan flip-flop groups in the scan trees and the number of XOR trees are determined by the structural features of the circuit. No aliasing fault is produced by the enhanced scan forest and the XOR trees.

VI. Experimental Results

The test application schemes corresponding to the proposed enhanced scan forest architecture and the conventional enhanced scan architecture have been implemented based on the SPC test generation algorithm [13]. Table 1 and Table 2 compare our method with the conventional enhanced scan design in terms of ATPG time (seconds), fault simulation time (seconds), the number of test pattern pairs (vec), the compactness (comp., defined as the average number of path delay faults covered by a test pair), area overhead AO(%), test application time reduction ratio (TAP), test stimulus data reduction ratio (TDR), and test response data volume reduction ratio (TDR'). Our method, which uses the SPC test generator [13], obtains complete coverage for all circuits for both robust and non-robust testing. ATPG based on broadside testing for non-robust testing yields fault coverage of only 34.7%, 100%, 84.88%, 88.73%, and 51.72% for circuits s13207, s15850, s35932, s38417, and s38584, respectively. For robust testing, the fault coverage obtained using the broadside method for the five circuits is only 22.82%, 8.76%, 77.13%, 41.82%, and 26.72%, respectively. The parameters S_{in} and *paths* represent the number of scan-in pins and the number of path delay faults. The AO is denotes the percentage increase in the area with respect to area of the original circuit based on the cell library "class.lib" of Synopsys Design Compiler. Interconnects are not included in the area estimates at this time, but they will included in the final version. The parameters TAP, TDR, and TDR' denote the test application time, test stimulus data volume, and test response data volume reduction ratios, expressed as a percentage of the corresponding parameters for the enhanced scan forest, respectively. For example, if the value of TAP is 4, it implies that a 25x reduction in test application time is obtained. Likewise, a TDR value of 12 implies a greater than 8x reduction in the stimulus data volume.

Table 1 (for non-robust testing) shows that the compactness for the proposed Method is slightly less for all circuits, except s38417 and s35932. The stimulus test data volume, test response volume, and test application time are reduced significantly in all cases. The area overhead is also noticeably less for all circuits. Table 2 presents experimental results for robust path delay fault testing. The test response compactor for robust path delay fault testing is different from that for non-robust delay testing, therefore the area overhead figures in Table 2 are different that in Table 1. The compactness for robust path delay ATPG is similar to that for non-robust delay testing; it decreases a little for circuits s9234, s13207, s15850, and s38584 for the enhanced scan forest and increases substantially for circuits s35932 and s38417. The test application time, test stimulus data volume, and test response data volume are reduced greatly compared with those of the original enhanced scan design. For example, for robust testing of s38417, the test stimulus volume is reduced 30x, the test response data volume is reduced 25x, and the test application time is reduced 300x compared with the original enhanced scan architecture.

VII. Conclusions

We have proposed a new scan architecture, referred to as the enhanced scan forest, for testing path delay faults. The proposed test architecture inserts only a small number of hold latches in the circuit and it allows us to assign any arbitrary test pair to the scan flip-flops. The scan forest consists of multiple scan trees, where a scan-in signal drives a number of scan segments. All scan flip-flops at the same level in a given scan tree of the enhanced scan forest share the same hold latch. XOR trees are constructed to compact test responses by connecting only the leaf scan flip-flops a scan segments to the XOR trees. The proposed enhanced scan forest architecture reduces the test stimulus data volume, the test re-

Table 1. Performance Comparison with the Enhanced Scan for Non-robust Path Delay Fault Testing

circuits	S_{in}	*paths*	enhanced scan					enhanced scan forest							
			ATPG	Fsim	vec	comp.	AO (%)	ATPG	Fsim	vec	comp.	TDR(%)	TDR'(%)	TAP (%)	AO (%)
s9234	19	59854	1217	91	1107	54.1	14.86	2262	435	1456	41.1	55.38	3.16	3.45	9.91
s13207	16	476145	7108	1238	2439	195.2	25.01	7453	1330	2622	181.6	34.53	1.83	2.16	14.79
s15850	7	121525	10227	3583	2417	50.3	20.26	11606	3529	2692	45.1	22.97	2.77	3.17	10.78
s35932	1	58657	1130	9.97	69	850.1	28.16	1359	15.5	64	916.5	2.42	0.5	0.59	11.41
s38417	4	1138194	79661	23946	18878	60.3	23.17	55123	9510	8020	141.9	2.86	0.51	0.55	9.46
s38584	12	334922	6351	1281	3842	87.2	20.85	7793	1765	3923	85.4	7.53	0.53	0.63	9.77

Table 2. Performance Comparison with the Enhanced Scan for Robust Path Delay Fault Testing

circuits	S_{in}	*paths*	enhanced scan					enhanced scan forest							
			ATPG	Fsim	vec	comp.	AO(%)	ATPG	Fsim	vec	comp.	TDR(%)	TDR'(%)	TAP(%)	AO(%)
s9234	19	21389	5599	42	1728	12.4	14.86	2613	107	1913	11.2	46.6	11.5	2.90	9.78
s13207	31	27603	19811	79	2727	10.1	25.01	5498	118	3244	8.51	38.9	9.64	1.24	13.79
s15850	14	182673	41207	5813	7557	24.2	20.26	34965	5951	8395	21.8	22.9	7.47	1.67	7.63
s35932	1	21738	16463	16	278	78.4	28.16	3149	11	126	172.9	1.18	2.81	0.16	10.81
s38417	8	598062	225335	20626	32348	18.5	23.17	135885	5429	14734	40.6	3.07	3.97	0.31	9.42
s38584	12	92239	23115	282	3484	26.5	20.85	27282	892	4551	20.3	9.64	5.74	0.81	9.78

sponse data volume, and the test application time for robust and non-robust path delay fault testing. At the same time, it provides complete coverage of path delay faults by applying all two-pattern pairs generated by an ATPG tool. We have compared the proposed scan forest architecture with the conventional enhanced scan design.

REFERENCES

[1] K. T. Cheng, S. Devadas, and K. Keutzer, "A partial enhanced-scan approach to robust delay fault test generation for sequential circuits," in *Proc. of ITC*, pp. 403-410, 1991.

[2] R. Datta, R. Gupta, A. Sebastine, and J. A. Abraham, "Tri-Scan: A novel DFT technique for CMOS path delay fault testing," *Proc. of ITC*, pp. 1118-1127, 2004.

[3] B. Dervisoglu and G. E. Stong, "Design for testability using scan path techniques for path delay test and measurement," in *Proc. of ITC*, pp. 365-374, 1991.

[4] P. Girard, C. Landrault, V. Moreda, S. Pravossoudovitch, A. Virazel, and V. D. Agrawal, "Scan-BIST structure to test delay faults in sequential circuits," *JETTA*, vol. 14, no. 1, pp. 95-102, 1999.

[5] S. Kajihara, M. Fukunaga, X. Wen, T. Maeda, S. Hamada, and Y. Sato, "Path delay test compaction with process variation tolerance," in *Proc. of 42th DAC*, pp. 845-850, 2005.

[6] A. Krstic and K. T. Cheng, *Delay Fault Testing for VLSI Circuits,* Kluwer Academic Publishers, 1998.

[7] J. J. Liou, L. C. Wang, K. T. Cheng, J. Dworak, M. R. Mercer, R. Kapur, and T. W. Williams, "Enhancing test efficiency for delay fault testing using multiple-clocked schemes," in *Proc. of 39th DAC*, pp. 371-374, 2002.

[8] X. Lin, R. Press, J. Rajski, P. Reuter, T. Rinderkneck, and N. Tamarapalli, "High-frequency, at-speed scan testing," *IEEE Design and Test*, Sept.-Oct., vol. 20, pp. 17-25, 2003.

[9] I. Pomeranz and S. M. Reddy, "At-speed delay testing of synchronous sequential circuits," *Proc. of DAC*, pp. 177-181, 1992.

[10] J. Savir and S. Patil, "Scan-based transition test," *IEEE Trans. on CAD*, vol. 12, no. 8, pp. 1232-1241, 1993.

[11] S. Wang and S. T. Chakradhar, "A scalable scan-path test point insertion technique to enhance delay fault coverage for standard scan design," *Proc. of ITC*, pp. 574-583, 2003.

[12] D. Xiang, K. Li, J. Sun, and H. Fujiwara, "Reconfigured scan forest for test application cost, test data volume, and test power reduction," *IEEE Trans. on Computers*, vol. 56, no. 4, pp. 557-562, April 2007.

[13] D. Xiang, K. Li, H. Fujiwara, and J. Sun, "Generating compact robust and non-robust tests for complete coverage of path delay faults based on stuck-at tests," *Proc. of ICCD*, pp. 446-451, Nov., 2006.