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TESTING LOGIC CIRCUITS WITH COMPRESSED DATA

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Abstract

Recently, several testing schemes such as one's count testing, transition count testing and edge count testing have been proposed to compress the test response data with simple test equipments. Although these schemes succeed in logarithmic compression of the response data, they require in the worst case twice the number of tests required for conventional testing, and thus the total length of the test data is not compressed in general. In this paper we present testing schemes which provide logarithmic compression of test response data without increasing the number of tests. We also present some simple testing schemes which provide considerable compression of test response data such that the response data can be reduced to two bits independently of the number of tests by adding only two tests. Test data compression for multiple output circuits is also considered and relatively effective testing schemes are presented.

I. Introduction

In most conventional methods, in order to test any logic circuit, an input sequence is applied and the resulting output response is compared with the correct response sequence. Recently, several testing schemes such as one's count testing, transition count testing, edge count testing and modified transition count testing have been proposed to compress the response data with very simple test equipments. These schemes may be classified as either deterministic [1]-[4] or probabilistic [5]-[6] in the methods for test pattern generation. In deterministic methods, all these schemes provide logarithmic compression of the response data. However, in the worst case, the length of input sequences for one's count testing [2] is approximately n^2, and for both transition count testing [1] and edge count testing [4] their length is approximately 2n where n is the number of tests. Therefore, the compression of overall test data is not achieved in general. Only modified transition count testing [3] has succeeded in the response data compression without increasing the length of the input sequence.

In this paper we restrict our discussion to deterministic testing and present the following testing schemes: 1) testing schemes which provide logarithmic compression of test response data without increasing the number of tests, and 2) testing schemes which provide considerable compression of test response data such that the response data can be reduced to two bits independently of the number of tests by adding only two tests. Test data compression for multiple output circuits is also considered and relatively effective testing schemes are presented. Section II, III and IV consider single-output combinational circuits, and then multiple-output combinational circuits are considered in Section V.

II. Testing Schemes and Count Functions

All the schemes considered in this paper can be represented by the functional block of Figure 1. A sequence of tests is applied to the circuit under test. The response of the circuit is transformed by some data compression function and then compared against a previously obtained reference value. The circuit under test is certified to be fault-free if and only if the two values are identical.

We consider the following data compression functions which are used in the data compression box of Figure 1.

Definition 1: Let $R = r_1 r_2 \ldots r_m$ be any binary sequence. The following seven functions are count functions.

$$c_1(R) = \sum_{i=1}^{m} r_i$$

$$c_2(R) = \sum_{i=2}^{m} r_{i-1} \oplus r_i$$

$$c_3(R) = \sum_{i=2}^{m} \overline{r_{i-1} \oplus r_i}$$

$$c_4(R) = \sum_{i=2}^{m} \bar{r}_{i-1} \cdot r_i$$

$$c_5(R) = \sum_{i=2}^{m} r_{i-1} \cdot \bar{r}_i$$

$$c_6(r_0, R) = c_2(r_0 R)$$

$$c_7(r_0, R) = c_3(r_0 R)$$

Let T be any multiple fault test set for a single-output combinational circuit. Let $T_0(T_1)$ be all tests in T producing output 0 (1), and let $n=|T|$, $n_0=|T_0|$ and $n_1=|T_1|$ where $|A|$ is the cardinality of the set A. Then we define three type of test input sequences using the test set T as follows.

Definition 2: A test sequence denoted by α_T is

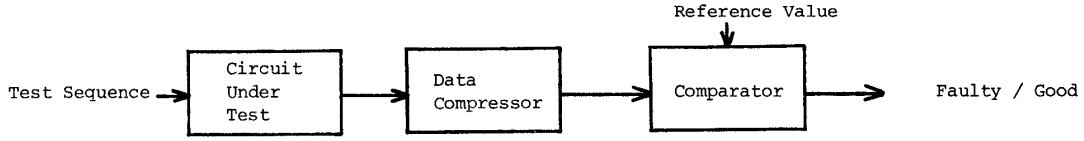

Figure 1. General testing schemes.

a sequence of length p satisfying the following conditions:

1) α_T includes every member of T,
2) α_T is an alternating sequence of tests from T_0 and T_1, and
3) $p \leq 2 \max\{n_0,n_1\} \leq 2n-2$.

Definition 3: A test sequence denoted by β_T is a sequence

$$t_{01}t_{02}\cdots t_{0n_0}t_{11}t_{12}\cdots t_{1n_1}$$

where $T_0 = \{t_{01},t_{02},\ldots,t_{0n_0}\}$ and $T_1 = \{t_{11},t_{12},\ldots,t_{1n_1}\}$.

Definition 4: A test sequence denoted by γ_T is a sequence

$$t_{01}t_{02}\cdots t_{0n_0}t_{01}\ t_{11}t_{12}\cdots t_{1n_1}t_{11}\ .$$

In the schemes proposed in this paper, one or more count functions will be used to implement the data compressor box of Figure 1. In general, we assume that an m-tuple

$$C = (c_{i_1},c_{i_2},\ldots,c_{i_m}),\quad m \geq 1$$

of count functions is being used for testing.

Definition 5: For a given class of faults, a circuit under test will be called testable by a count function C and a test sequence S if for every fault in the class, the value of C is different from the reference value.

III. Fault Detection

Both the test input sequence and the correct response sequence can be considered as the test data. Hence an overall data compression should be the compression of total test data, that is, the test input sequence plus the response data. Most of the testing schemes reported previously have not achieved the overall data compression as Theorems 1-4 shown below.

The simplest count function c_1 is used in one's count testing [2], and the following theorem is reported.

Theorem 1 (Hayes[2]): Let T be any multiple fault test set for a single-output combinational circuit. Let S be a sequence of $(n-n_0)(n_0+1)+n_0$ tests from T with the following properties:

1) S contains one copy of every test in T_0, and
2) S contains n_0+1 copies of every test in T_1.

Then the circuit is testable by the count function c_1 and S for multiple faults. The reference value of c_1 is $n_1(n_0+1)$. The length of S is at most n^2-n+1.

In this one's count testing, the number of bits required to represent $c_1(R)$ is at most $\lceil \log_2 n^2 \rceil$, where $\lceil x \rceil$ denotes the smallest integer greater than or equal to x. However the length of the test sequence is approximately n^2 in the worst case. Therefore, the compression of overall test data is not achieved in general.

Theorem 2 (Hayes[1]): Let T be any single fault test set for a single-output combinational circuit. Then the circuit is testable by the count function c_2 and test sequence α_T for single faults. The reference value of c_2 is at most 2n-3.

It is not known if Theorem 2 also holds for multiple faults. The following theorems hold for multiple faults.

Theorem 3 (Seth[3]): Let T be any multiple fault test set for a single-output combinational circuit. Then the circuit is testable by the count function c_6 and the test sequence α_T for multiple faults. The reference value of c_6 is at most 2n-2.

Theorem 4 (Reddy[4]): Let T be any multiple fault test set for a single-output combinational circuit, and let α_T be a test sequence of even length. Then the circuit is testable by the count function c_4 and the test sequence α_T for multiple faults. The reference value of c_4 is $\max\{n_0,n_1\}$.

Theorems 2,3 and 4 show that the number of bits required to represent the reference values of count functions c_2,c_6 and c_4 is at most $\lceil \log_2 2n \rceil$, and that all these testing schemes provide logarithmic compression of the response data. However, the length of the testing sequence is approximately 2n in the worst case. Therefore the test data is not totally compressed at all.

Theorem 5 (Seth[3]): Let T be any multiple fault test set for a single-output combinational circuit. Further assume that the constant r_0 of c_6 is zero. Then the circuit is testable by the pair of count functions (c_1,c_6) and the test sequence β_T for multiple faults. The reference values of c_1 and c_6 are n_1 and 1, respectively.

Since the length of the test sequence β_T is n, Theorem 5 proves that every multiple fault in a single-output combinational circuit is detectable by the pair of count functions (c_1,c_6) using the same number of tests required for conventional testing. Moreover, the number of bits required to store the reference value is compressed into $\lceil \log_2 n_1 \rceil$ and thus the test data is totally compressed.

Next, we show that the results similar to Theorem 5 are possible for such pairs of count fucntions as (c_1,c_5) and (c_1,c_7).

Theorem 6: Let T be any multiple fault test set for a single-output combinational circuit. Further assume that the constant r_0 of c_7 is zero. Then the circuit is testable by the test sequence β_T and either pair of count functions of (c_1,c_5) or (c_1,c_7) for multiple faults. The reference values of c_1, c_5 and c_7 are n_1,0 and n-1, respectively.

Proof:
1) Case of (c_1,c_5).

The fault-free response R has the form $0^{n_0}1^{n_1}$ where $n_0>0$, $n_1>0$ and $n=n_0+n_1$. Then, obviously, $c_1(R)=n_1$ and $c_5(R)=0$. Assume that another sequence S, distinct from R, also has $c_1(S)=n_1$ and $c_5(S)=0$. Now, $c_5(S)$ can be 0 only if S has the form 0^p1^q where $p\geq 0$, $q>0$ and $p+q=n$. Since $c_1(S)=n_1 < n$, we have $p>0$ and $q=n_1$. Therefore, $p=n_0$ and $q=n_1$, so R and S must be identical, which contradicts the assumption that they are distinct.

2) Case of (c_1,c_7).

The fault-free response R has the form $0^{n_0}1^{n_1}$, where $n_0>0$, $n_1>0$ and $n=n_0+n_1$. Then, with $r_0=0$ we have $c_7(r_0,R)=c_3(0R)=n-1$. Assume that another sequence S, distinct from R, also has $c_1(S)=n_1$ and $c_7(0,S)=c_3(0S)=n-1$. Since $c_3(0S)=n-1$, the sequence 0S includes exactly one transition. Hence, the sequence 0S has the form 0^p1^q where $p>0$, $q>0$ and $p+q=n+1$. Moreover, $c_1(S)=n_1$ implies $q=n_1$, and so $p=n+1-n_1=n_0+1$. Therefore, R and S must be identical, which contradicts the assumption that they are distinct. Q.E.D.

IV. Testing with Fixed Reference Values

In the previous section, we have presented testing schemes which provide logarithmic compression of test response data. However, these testing schemes need a $\lceil \log_2 n \rceil$-bit binary counter which depends on the number of tests. Thus, when the number of tests increases, the size of the counter must be increased or the test sequence must be partitioned into subsequences suitable to the counter. However, it is required additional cost to change the size of the counter or to perform multiple experiments with partitioned sequence. To overcome this, we present testing schemes which provide considerable compression of test response data such that the response data can be compressed into two bits independently of the number of tests.

Theorem 7: Let T be any multiple fault test set for a single-output combinational circuit. Further assume that the constant r_0 of c_7 is one. Then the circuit is testable by the count function c_7 and the test sequence α_T for multiple faults. The reference value of c_7 is 0.

Proof: The fault-free response R for the test sequence α_T has the form:

$$R = \begin{cases} (01)^{\ell} & \text{if the length is even.} \\ (01)^{\ell}0 & \text{if the length is odd.} \end{cases}$$

Obviously, with $r_0=1$ we have $c_7(1,R)=c_3(1R)=0$. Assume that another sequence S, distinct from R, also has $c_7(1,S)=c_3(1S)=0$. Then, S has the form either $(01)^{\ell}$ or $(01)^{\ell}0$ for some positive integer ℓ. Therefore R and S is identical, which contradicts the assumption that they are distinct. Q.E.D.

Theorem 7 shows that the reference value of count function c_7 is 0, and thus the number of bits required to represent the reference value is only one. Such testing scheme requires only an 1-bit binary counter and thus is very simple. However, the testing sequence is α_T and so its length is approximately 2n in the worst case. The same compression of test response data as Theorem 7 is possible by adding only two tests.

Lemma 1: The following conditions are equivalent.

1) $R=0^p1^q$ for some $p>0$ and $q>0$.
2) $c_4(R)=1$ and $c_5(R)=0$.
3) $c_2(R)=1$ and $c_4(R)=0$.
4) $c_2(R)=1$ and $c_5(R)=0$.
5) $c_2(R)=1$ and $c_6(0,R)=1$.
6) $c_4(R)=1$ and $c_6(0,R)=1$.

Proof: It is obvious that Condition 1 implies Conditions 2-6.

Assume that Condition 2 holds, that is, $c_4(R)=1$ and $c_5(R)=0$. Then $c_5(R)=0$ implies that R has the form 0^p1^q where $p\geq 0$ and $q>0$. Moreover, $c_4(R)=1$ implies both p and q are positive. Therefore we have Condition 2 implies Condition 1. From the definitions of count functions c_2,c_4 and c_5 we have $c_2(R)=c_4(R)+c_5(R)$. Hence it is obvious that Conditions 2,3 and 4 are all equivalent.

Assume that $c_6(0,R)=c_2(0R)=1$. Then the sequence 0R has exactly one transition since $c_2(0R)=1$. Hence the sequence 0R has the form 0^p1^q, and so $c_5(R)=0$. Therefore, we have that Condition 5 implies Condition 4, and that Condition 6 implies Condition 2. Q.E.D.

Theorem 8: Let T be any multiple fault test set for a single-output combinational circuit. Further assume that the constant r_0 of c_6 is zero. Then the circuit is testable by the test sequence γ_T and any of the following pairs of count functions: 1) (c_4,c_5), 2) (c_2,c_4), 3) (c_2,c_5), 4) (c_2,c_6) and 5) (c_4,c_6). The reference values of c_2,c_4,c_5 and c_6 are 1,1,0 and 1, respectively.

Proof: Let $T=\{T_0,T_1\}$, $T_0=\{t_{01},t_{02},\ldots,t_{0n_0}\}$ and $T_1=\{t_{11}t_{12},\ldots,t_{1n_1}\}$. The test sequence γ_T has the form

$$t_{01}t_{02}\cdots t_{0n_0}t_{01}t_{11}t_{12}\cdots t_{1n_1}t_{11}$$

and the fault-free response R is

$$0^{n_0+1}1^{n_1+1}.$$

Let (c_i,c_j) be any of the pairs of count functions presented in Theorem 8, and let e_i and e_j be reference values of c_i and c_j, respectively. Then from Lemma 1, $R=0^{n_0+1}1^{n_1+1}$ implies $c_i(R)=e_i$ and $c_j(R)=e_j$.

Conversely, assume that another sequence S also has $c_i(S)=e_i$ and $c_j(S)=e_j$. Then from Lemma 1, S has the form 0^p1^q where $p>0$, $q>0$ and $p+q=n+2$. If both sequences S and R are distinct, then either $n_0+1 > p$ or $n_0+1 < p$. In the case of $n_0+1 > p$, the output value of test t_{01} in S must be 1. Thus the left-most value of S is also 1, and this contradicts that S has the form 0^p1^q for $p>0$ and $q>0$. In the case of $n_0+1 < p$, the output value of test t_{11} in S must be 0, and similarly we have the contradiction.

Hence, R and S must be identical. This implies that any response S satisfying $c_i(S)=e_i$ and $c_j(S)=e_j$ is only $0^{n_0+1}1^{n_1+1}$. Q.E.D.

Using the test sequence γ_T of length n+2, the testing schemes suggested in Theorem 8 require storing only two bits of response since the reference values of count functions are constants 0 and 1. Thus such testing schemes have the following important properties.

1) Considerable compression of test response data is achieved.
2) Very simple test equipment is required where the reference values are independent of the circuit under test.
3) Complete fault detection is provided.

V. Multiple Output Circuits

When a logic circuit has more than one output, the problem of compressing test data is not straightforword generalization of the single output case because all the outputs are assumed to be monitored simultaneously. Thus, ordering of tests to suit individual outputs is no longer possible. Accordingly, we regard a k-output combinational circuit as a 2^k-valued output combinational circuit, and consider generalized count functions for multi-valued sequence as follows.

Definition 6: Let $R = r_1 r_2 \ldots r_m$ be any q-valued sequence. The following three functions are count functions for multi-valued sequences.

$$c_8(R) = \sum_{i=2}^{m} p(r_{i-1} < r_i)$$

$$c_9(R) = \sum_{i=2}^{m} p(r_{i-1} > r_i)$$

$$c_{10}(R) = \sum_{i=2}^{m} p(r_{i-1} \neq r_i)$$

where

$$p(\text{predicate}) = \begin{cases} 1 & \text{if the predicate is true.} \\ 0 & \text{otherwise.} \end{cases}$$

In the binary case, these count functions c_8, c_9 and c_{10} coincide with count functions c_4, c_5 and c_2, respectively, and so are the generalizations of c_4, c_5 and c_2.

Let $T = \{T_0, T_1, \ldots, T_{q-1}\}$ be any fault test set for a q-valued output circuit, where $T_i = \{t_{i1}, t_{i2}, \ldots, t_{in_i}\}$ be all tests in T producing output value i. Let $n = |T|$ and $n_i = |T_i|$ for all i. Assume that $n_i > 0$ for all $0 \leq i \leq q-1$.

Definition 7: A test sequence denoted by δ_T is a sequence

$$t_{01}t_{02}\ldots t_{0n_0}t_{01}\ t_{11}t_{12}\ldots t_{1n_1}t_{11}\ldots\ldots\ldots\ldots\ldots t_{q-1,1}t_{q-1,2}\ldots t_{q-1,n_{q-1}}t_{q-1,1}\ .$$

The fault-free response R for δ_T has the form

$$R = 0^{n_0+1}\ 1^{n_1+1}\ \ldots\ (q-1)^{n_{q-1}+1}\ .$$

In the case of q=2, the test sequence δ_T coincides with the test sequence γ_T and so is the generalization of γ_T.

Lemma 2: The following conditions are equivalent.

1) For some positive integers $k_0, k_1, \ldots, k_{q-1}$,
$$R = \overbrace{00\ldots0}^{k_0}\overbrace{11\ldots1}^{k_1}\ldots\ldots\overbrace{(q-1)(q-1)\ldots(q-1)}^{k_{q-1}}$$
2) $c_8(R)=q-1$ and $c_9(R)=0$.
3) $c_8(R)=q-1$ and $c_{10}(R)=q-1$.
4) $c_9(R)=0$ and $c_{10}(R)=q-1$.

Proof: It is obvious that Condition 1 implies Conditions 2-4.

Assume that $c_8(R)=q-1$ and $c_9(R)=0$. Since $c_8(R)=q-1$, the sequence R contains exactly q-1 ascending subsequences $r_{i-1}r_i$ such that $r_{i-1} < r_i$, and no descending subsequences $r_{i-1}r_i$ such that $r_{i-1} > r_i$. Therefore, all the values from 0 to q-1 appears in the sequence R, and for some positive integers $k_0, k_1, \ldots, k_{q-1}$,

$$R = 0^{k_0}\ 1^{k_1}\ \ldots\ (q-1)^{k_{q-1}}\ .$$

Hence we have that Condition 2 implies Condition 1.

Since $c_{10}(R)=c_8(R)+c_9(R)$, it is shown that Conditions 2,3 and 4 are equivalent. Q.E.D.

Lemma 3: If the response R for the test sequence δ_T has the form

$$R = 0^{k_0}\ 1^{k_1}\ \ldots(q-1)^{k_{q-1}}$$

where $k_0, k_1, \ldots, k_{q-1}$ are positive integers, then for each i ($0 \leq i \leq q-1$) all the output values corresponding to $t_{i1}, t_{i2}, \ldots, t_{in_i}$ are the same.

Proof: The test sequence δ_T contains the following subsequence composed of all tests in T_i

$$t_{i1}t_{i2}\ldots t_{in_i}t_{i1}.$$

Let R_i be the response of such subsequence. Since R has the form

$$0^{k_0}\ 1^{k_1}\ldots(q-1)^{k_{q-1}}$$

for some positive integers $k_0, k_1, \ldots, k_{q-1}$, we have $c_9(R)=0$ and so $c_9(R_i)=0$.

Assume that not all of the output values in R_i are the same. Then obviously, we have $c_9(R_i) \neq 0$, that is, R_i contains at least a descending subsequence. This contradicts $c_9(R_i)=0$. Q.E.D.

Theorem 9: Let T be any multiple fault test set for a q-valued output combinational circuit. Then the circuit is testable by the test sequence δ_T and any of the following pairs of count functions: (c_8, c_9), (c_8, c_{10}) and (c_9, c_{10}). The reference values of c_8, c_9 and c_{10} are q-1,0 and q-1, respectively.

Proof: Let $T=\{T_0, T_1, \ldots, T_{q-1}\}$, and let $T_i = \{t_{i1}, t_{i2}, \ldots, t_{in_i}\}$ for all $0 \leq i \leq q-1$. The test sequence δ_T is

$$t_{01}t_{02}\ldots t_{0n_0}t_{01}\ t_{11}t_{12}\ldots t_{1n_1}\ldots\ldots\ldots\ldots t_{q-1,1}t_{q-1,2}\ldots t_{q-1,n_{q-1}}t_{q-1,1}$$

and the fault-free response R is

$$0^{n_0+1}\ 1^{n_1+1}\ \ldots\ldots(q-1)^{n_{q-1}+1}\ .$$

Let (c_k, c_ℓ) be any of the pairs of count functions presented in Theorem 9, and let e_k and e_ℓ be reference values of c_k and c_ℓ, respectively. Then from Lemma 2, $R = 0^{n_0+1}\ 1^{n_1+1}\ \ldots\ (q-1)^{n_{q-1}+1}$ implies $c_k(R)=e_k$ and $c_\ell(R)=e_\ell$.

Conversely, assume that another sequence S of length n+q also has $c_k(S)=e_k$ and $c_\ell(S)=e_\ell$. Then from Lemma 2, S has the form

$$0^{k_0}\ 1^{k_1}\ldots\ldots(q-1)^{k_{q-1}}$$

where $k_0, k_1, \ldots, k_{q-1}$ are positive integers ans $k_0+k_1+\ldots+k_{q-1}=n+q$. By Lemma 3, all the output values for the subsequence $t_{i1}t_{i2}\ldots t_{in_i}t_{i1}$ of δ_T are the same. Moreover, S contains all the values from 0 to q-1. Hence, we have $k_i=n_i+1$ for all $0 \leq i \leq q-1$, that is, R and S must be identical. This implies that any sequence S satisfying $c_k(S)=e_k$ and $c_\ell(S)=e_\ell$ is only

$$0^{n_0+1}\ 1^{n_1+1}\ \ldots\ (q-1)^{n_{q-1}+1}\ .$$ Q.E.D.

Testing schemes presented in Theorem 9 have the following properties. Any pairs of count functions c_8, c_9 and c_{10} require $(\log_2 q)$-bit binary counters and $(\log_2 q)$-bit comparators. This size $\log_2 q$ depends only

on the number of outputs but is independent of the the number of tests. Conventional testing requires storing $n(\log_2 q)$ bits of response while the method suggested in the theorem requires only $\log_2 q$ bits where $n = |T|$. Thus the compression ratio

$$\frac{n(\log_2 q)}{\log_2 q} = n$$

is obtained. The length of the test sequence δ_T is n+q, and thus extra q tests are required. However this augmentation may be ignored by taking n sufficiently large, and in this case the data compression ratio becomes large.

In the above arguments we have assumed that $n_i > 0$ for all $0 \le i \le q-1$, that is, all the output values 0,1,...,q-1 appear in the test response. When this assumption does not hold, we can extend the result of Theorem 9. However in this case we cannot achieve such a good data compression as Theorem 9.

Let $T = \{T_1, T_2, \ldots, T_k\}$ be any fault test set for a q-valued output circuit, where $T_i = \{t_{i1}, t_{i2}, \ldots, t_{in_i}\}$ be all tests in T producing output value v_i. Let $V_T = \{v_1, v_2, \ldots, v_k\}$ and $\bar{V}_T = \{0,1,\ldots,q-1\} - V_T$. The output values are ascending, that is, $0 \le v_1 < v_2 < \ldots < v_k \le q-1$. Since not all the output values 0,1,...,q-1 appear in the test response, we have $k < q$. For this test set T we define a test sequence similar to the test sequence δ_T as follows.

Definition 8: A test sequence denoted by ε_T is a sequence

$$t_{11}t_{12}\cdots t_{1n_1}t_{11}\ t_{21}t_{22}\cdots t_{2n_2}t_{21}\cdots\cdots$$
$$\cdots\cdots t_{k1}t_{k2}\cdots t_{kn_k}t_{k1}\ .$$

The fault-free response of the test sequence ε_T has the form

$$\overbrace{v_1v_1\cdots v_1}^{n_1+1}\ \overbrace{v_2v_2\cdots\cdots v_2}^{n_2+1}\cdots\cdots\overbrace{v_kv_k\cdots\cdots v_k}^{n_k+1}$$

The count function for the test sequence ε_T is defined as follows.

Definition 9: Let $R = r_1r_2\ldots r_m$ be any q-valued sequence. The count function c_{11} is defined as

$$c_{11}(R,V) = \sum_{i=1}^{m} p(\, r_i \in V\,)$$

Note that if R is the fault-free response of the test sequence δ_T, that is, all the output values 0,1,...,q-1 appear in the response, then $\bar{V}_T = \phi$ and thus $c_{11}(R, \bar{V}_T) = 0$.

Theorem 10: Let $T = \{T_1, T_2, \ldots, T_k\}$ be any multiple fault test set for a q-valued output combinational circuit. Further assume that V of c_{11} is $\bar{V}_T$. Then the circuit is testable by the test sequence ε_T and any of the following count functions: (c_8, c_9, c_{11}), (c_8, c_{10}, c_{11}) and (c_9, c_{10}, c_{11}). The reference values of c_8, c_9, c_{10} and c_{11} are k-1, 0, k-1 and 0, respectively.

Proof: Let $T = \{T_1, T_2, \ldots, T_k\}$, $V_T = \{v_1, v_2, \ldots, v_k\}$ and $T_i = \{t_{i1}, t_{i2}, \ldots, t_{in_i}\}$ for all $1 \le i \le k$. Let R be the fault-free response of the test sequence ε_T. Then, obviously $c_8(R) = c_{10}(R) = k-1$ and $c_9(R) = c_{11}(R, \bar{V}_T) = 0$.

Conversely, assume that another sequence S of length n+k also has $c_8(S) = k-1$, $c_9(S) = 0$ and $c_{11}(S, \bar{V}_T) = 0$. Then, from $c_8(S) = k-1$ and $c_9(S) = 0$, we can show that S has the form

$$\overbrace{u_1u_1\cdots u_1}^{n_1+1}\ \overbrace{u_2u_2\cdots u_2}^{n_2+1}\cdots\cdots\overbrace{u_ku_k\cdots u_k}^{n_k+1}$$

where $u_i < u_j$ for $i < j$.

Since $c_{11}(S, \bar{V}_T) = 0$, we have $u_i \in V_T$ for all $1 \le i \le k$. This implies that $u_i = v_i$ for all $1 \le i \le k$, that is, R and S must be identical.

For the cases of (c_8, c_{10}, c_{11}) and (c_9, c_{10}, c_{11}), the theorem can also be proved similarly, since $c_{10}(R) = c_8(R) + c_9(R)$. Q.E.D.

There are two ways to represent the set V_T: (a) to store separately each value v_i $(1 \le i \le k)$; and (b) to represent the set V_T by q binary variables $b_0, b_1, \ldots, b_{q-1}$ such that $b_i = 1$ if $i \in V_T$ and $b_i = 0$ if $i \notin V_T$ for all $0 \le i \le q-1$. In the case of (a), the number of bits to represent the set V_T is $k(\log_2 q)$, and thus the testing schemes suggested in Theorem 10 requires storing

$$\log_2 k + k(\log_2 q)$$

bits. Conventional testing requires storing $n(\log_2 q)$ bits. Thus the compression ratio is

$$\frac{n(\log_2 q)}{\log_2 k + k(\log_2 q)} > \frac{n}{k+1}$$

In the case of (b), the number of bits to represent the set V_T is q, and thus the testing schemes suggested in Theorem 10 requires storing

$$\log_2 k + q$$

bits. Hence, the compression ratio is

$$\frac{n(\log_2 q)}{\log_2 k + q}$$

These data compression ratios are not so good as that of Theorem 9. However, when n is sufficiently larger than k or q, substantial data compression is achieved.

VI. Conclusion

In this paper, we have considered test data compression in logic testing. For single output circuits we presented such testing schemes that provide logarithmic compression of test response data without increasing the number of tests. We also presented some simple testing schemes which provide considerable compression of test response data such that the response data can be compressed into a constant value (two bits) independently of the number of tests by adding only two tests. For multiple output circuits, we have showed that test data comperssion can be achieved by using generalized count functions. The results presented here are applicable only to combinational circuits. Further research is needed to find effective compression functions in logic testing for sequential circuits.

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