Thermal-Uniformity-Aware X-Filling to Reduce Temperature-Induced Delay Variation for Accurate At-Speed Testing

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Abstract

It is well known that the test mode exceeds the functional mode in power consumption, which is not uniformly distributed within the circuit. The non-uniformity in spatial power distribution may cause localized heating and temperature differences within the circuit. Since gate delay depends on junction temperature, thermal differences within the circuit may lead to erroneous pass or fail in at-speed testing. This paper first discusses the importance of spatial thermal uniformity for high quality and accurate at-speed testing. The paper also presents an X-filling technique that minimizes the spatial temperature variation within the circuit while preserving the overall circuit power consumption at low level. Experimental results show the effectiveness of the proposed method compared to the existing X-filling techniques.

keywords: *thermal-uniformity, test power, X-filling, at-speed test.*

1 Introduction

It is well known that switching activity in test-mode is several times higher than that in functional mode. In scan-based DFT architectures, each test pattern generates a significant amount of switching activities not only in the scan chains but also in logic cells during the scan-shift operation. The excessive switching activity increases overall circuit temperature, and at the same time, creates localized heating, so called *hot-spot*. Peak temperature on hot-spot may lead to high cooling cost, decrease in reliability or even permanent damage [1]. Furthermore, since a hot-spot, which occurs faster than circuit-wide heating, is a localized by nature, it can create temperature differences across the circuit. The spatial temperature non-uniformity causes a non-uniform effect on relative path delay within logic blocks. In [2], for every 20°C rise in temperature, approximately a 5-6% delay variation in timing was observed. Test-induced hot-spots can slow critical and/or non-critical paths, causing the circuit to fail (pass) in delay test even for a good (bad) part (this will be further discussed in Section 2).

For the above-mentioned power and thermal problems, a significant amount of works on power reduction have been proposed in literature [1] such as low power ATPG, X-filling, pattern ordering, scan chain modification and low power oriented DFT to reduce average and/or peak power consumption. Although minimizing or limiting the overall chip power consumption may reduce the temperature, it is not effective enough in reducing the peak temperature on hot-spots or in creating spatially uniform temperature distribution because of the non-uniform spatial power distribution across the circuit. Recently, several approaches have been proposed in order to directly reduce or limit the peak temperature on hot-spots [3, 4, 5, 6, 7]. Although the hot-spot temperature can be reduced with the above methods, the temperature differences within the circuit can be still as high as 40°C to 50°C and create non-uniform thermal maps [8].

In this paper, we discuss the importance of achieving spatial uniformity in temperature distribution that minimize temperature-induced delay variation and of increasing the quality and accuracy in at-speed testing. It is well known that temperature in a layout block depends on power density (*heat generation*) of the block as well as *heat transfer* or *heat exchange* between the adjacent blocks [9]. When the power consumption is uniformly distributed across the circuit, there will be no heat exchange between the blocks, which results in spatially uniform temperature distribution. Therefore, we introduce a power management framework based on X-filling technique that achieves spatially uniform power distribution for the thermal-uniformity. To the best of our knowledge, this is the first paper that addresses the spatial temperature uniformity with X-filling technique. The main contributions of this paper are as follows.

- We discuss the importance of achieving spatially uniform temperature distribution for accurate at-speed testing, and show how power management techniques are used to solve the thermal-uniformity problem.
- We present a low-power and thermal-uniformity-aware X-filling technique that minimizes the spatial power variation between layout blocks while preserving the overall power at low level. The proposed method uses a standard scan design and does not require any DFT technique. Therefore, it is easily embedded into the current design flow.
- We present simulation results for ITC'99 benchmark circuits to illustrate the effectiveness of the proposed X-filling technique compared to the other X-filling methods.

The rest of this paper is organized as follows. Section 2 describes the importance of spatially uniform temperature distribution during test-mode and motivates the need for a thermal-uniformity-aware testing. Section 3 discusses a low-power and thermal-uniformity-aware X-filling problem and presents a framework to solve the problem. Section 4 presents experimental results for several ITC'99 benchmark circuits. Finally, Section 5 concludes the paper.

2 Motivation

In order to show how power consumption and temperature are distributed within the circuit, We performed some preliminary experiments using an ITC'99 benchmark circuit (*b*17) and a 45nm library [10]. We divided the circuit into 4×4 square layout blocks with the same size according to the layout information, and the flow shown in Figure 1 was used to estimate the power and temperature distribution across the 16 blocks. For the thermal simulation, we used a thermal simulator called *HotSpot* [9]. Except that,

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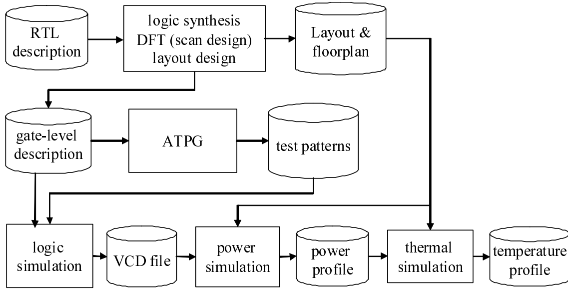
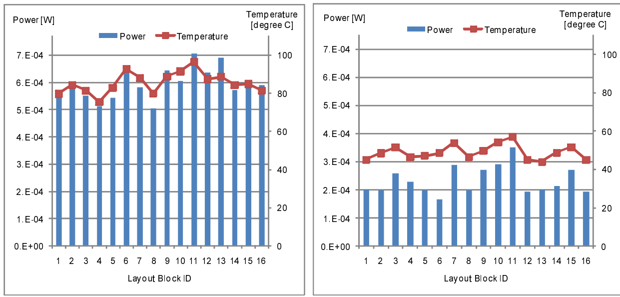


Figure 1. Flow to estimate power and temperature.



(a) Random fill (b) Minimum transition fill

Figure 2. Power and temperature distributions for $b17$.

the Synopsys tools were used in the experiments.

Figure 2 shows the spatial variations in power consumption and temperature when random or minimum transition fill method is used during ATPG process. Each bar in the figure denotes the average power consumption for a set of given test patterns in each block and each plot in the line graph denotes the corresponding temperature in the block. From Figures 2(a) and (b), we observe that the power consumption and temperature are not uniformly distributed within the circuit. The situation of the minimum transition fill still remains the same or worse than the random fill. Figure 3 shows the temperature-induced delay sensitivity of a ring oscillator (27 stages, 180nm process technology) [11]. For every 10°C rise in temperature, there is approximately a 170ps delay increase in timing. In Figure 2, the maximum temperature difference between layout blocks is around 20°C in both cases. This suggests that there may exist 340ps delay variation between the hottest and the coolest blocks, and it might lead to decrease in quality and accuracy of at-speed testing.

Finally, Figure 4 shows the result of temperature distribution when we use a hand-crafted spatially uniform power distribution (shown as the bar graph in the figure) for the thermal simulation. The result shows that the spatially uniform power distribution creates the spatial temperature uniformity since each block has the same power density and there exists no heat exchange between the blocks as we explained in Section 1.

These observations motivate the need for thermal-uniformity for a high quality and accurate at-speed testing, and show that a power management framework should be used to achieve the thermal-uniformity.

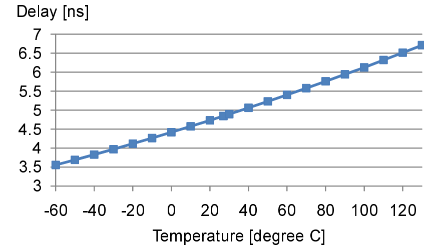


Figure 3. Temperature-induced delay sensitivity.

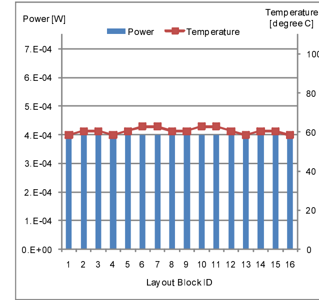


Figure 4. Temperature distribution by spatially uniform power.

3 Low-Power and Thermal-Uniformity Aware X-Filling

3.1 Problem Formulation

In this paper, we present a framework to manage the spatial power variation based on X-filling technique since it is known as one of the effective techniques to manage power consumption, and it has no impact on the fault coverage and the design flow. In scan-based designs, test application is carried out by simultaneous scan-out of the current test response and scan-in of the next test pattern, and this process is repeated until all the test patterns are applied. Switching activity as well as power consumption at each node of the circuit varies significantly at every clock cycle during test. However, it is well known that temperature does not change as rapidly as power consumption and it is enough to consider the average power in a time interval . In this paper, we consider the average power for each test pattern, not the cycle-by-cycle power since our preliminary experiments showed that a set of several thousand cycles is a proper unit of granularity for managing temperature. In the rest of this paper, we simply use the term ”power consumption for a test pattern t” to denote the average power consumption when t is completely shifted in and the previous response is simultaneously shifted out.

As we discussed in Section 2, the goal of this paper is to minimize the variation in power density between the given layout blocks. However, in order to simplify the discussion without loss of generality, we assume that all the sizes of the given layout blocks are the same and consider the variation in power consumption instead of power density in the rest of the paper. We use the variance σ^2 in power consumption for each test pattern t defined as follows to analyze the spatial variation.

$$\sigma^2(t) = \frac{1}{N}\sum_{i=1}^{N}(P_i(t) - P_{ave}(t))^2 \qquad (1)$$

1: **for** each test pattern $t \in T$ in the original order **do**
2: Set $t_{cur} = t$;
3: Do 0-fill for t_{cur};
4: Compute $\sigma^2(t_{cur})$ and Set $\sigma^2_{min} = \sigma^2(t_{cur})$;
5: **repeat**
6: **for** each scan chain $m \in M$ **do**
7: **for** $i = l_m$ to 1 **do**
8: **if** $t(m, i) = X$ **then**
9: Flip $t_{cur}(m, i)$ and Compute $\sigma^2(t_{cur})$;
10: **if** $\sigma^2_{min} > \sigma^2(t_{cur})$ **then**
11: Set $\sigma^2_{min} = \sigma^2(t_{cur})$;
12: **else**
13: Revert $t_{cur}(m, i)$;
14: **end if**
15: **end if**
16: **end for**
17: **end for**
18: **until** no more improvement on σ^2_{min}
19: Set $t = t_{cur}$ and Compute the response;
20: **end for**

Figure 5. The proposed framework to manage power variation.

where N is the number of layout blocks for temperature analysis, $P_i(t)$ is the power consumption in block b_i for t, and $P_{ave}(t)$ is the average power consumption among all the blocks for t. In addition to minimizing the variation between blocks, the overall power consumption should be minimized. Now, we formally define the low-power and thermal-uniformity-aware X-filling problem P_{PTXF} as follows.

Definition 1 P_{PTXF}: Given a netlist with M scan chains of length $l_1, l_2, ..., l_M$, ordered test set T with unspecified bits (Xs), physical information (xy-coordinates of each cells) and number of layout blocks N for temperature analysis, determine X-fill values for each test pattern such that (i) the variance in power consumption for the test pattern is minimized and (ii) the power consumption for the test pattern is minimized subject to (i).

3.2 Framework to Manage Power Variation

The outline of the proposed framework to solve P_{PTXF} is shown in Figure 5. For each test pattern t in the given ordered test set T, we first copy t to t_{cur} and fill all the Xs in t_{cur} with 0 for low power purpose (line 2-3). Then, we compute the variance for t_{cur}, $\sigma^2(t_{cur})$ and initialize the minimum variance σ^2_{min} by it (line 4). After that, we search through each scan chain $m \in M$ from its scan-out to scan-in (line 6-7). Whenever we find a FF which is originally unspecified in t (i.e., $t(m, i) = X$ where $t(m, i)$ denotes the value of ith FF in scan chain m for t), we flip the value to the opposite and compute the variance (line 8-9). If it is smaller than the current minimum variance σ^2_{min}, then we adopt the new value and update σ^2_{min} (line 11). Otherwise, we revert the change to the original (line 13). The above process is repeated until there is no more improvement on σ^2_{min} after exploring all the scan chains (line 5-18). Finally, we replace t by t_{cur} and compute the response for the next pattern (line 19).

In the proposed framework, we need to estimate power consumption in each block iteratively to compute the variance for each intermediate X assignment. For a pair of subsequent test vectors, we use the following flow, which is also shown in Figure 1, to estimate the power consumption in each block accurately.

Step1: We simulate the scan response-pattern pair using a logic simulator to capture the switching activity of all the cells in the circuit using VCD (Value Change Dump) format.

Step2: We use a power simulator to analyze the power consumption in each block of the circuit using the switching activity captured in Step1.

The power analysis using the above flow is able to get more accurate data than the analysis using switching activity alone, because the power simulator utilizes the characterized power information that includes dynamic and leakage power consumption, which is provided in the logic synthesis cell library. However, the flow is computationally very expensive. If we use this power estimation flow in our proposed X-filling scheme, we might not be able to search through a large number of candidate X-assignments within a reasonable computational time.

In [12], it was shown that the weighted transition count (WTC) in the scan chain during scan shifting has a high correlation with the total power consumption of the circuit. The WTC is easily calculated while it is not accurate enough to manage the spatial power distribution within the circuit (this will be shown in the next section). In [13, 14], the weighted switching activity (WSA) was presented to estimate power consumption. Even though the WSA is more accurate than the WTC, calculating the WSA is still a time consuming process. Therefore, in the next section, we present a fast and accurate power estimation method that is iteratively used in the proposed framework to manage spatial power distribution.

3.3 Fast and Accurate Power Estimation

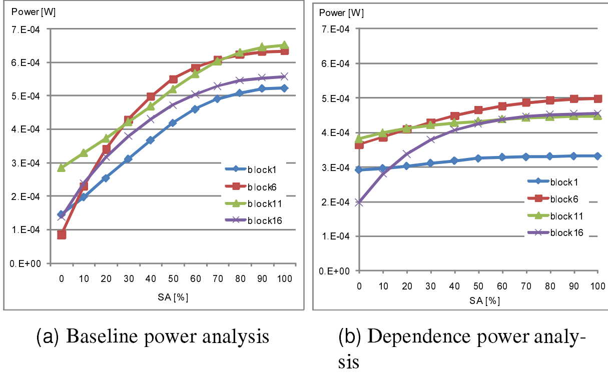
In this section, we present a new method to estimate the power consumption accurately only from the switching activities of FFs, not from the other logic cells in the circuit. Note that, in this paper, we use the term " switching activity (SA)" of FF to denote the ratio of the total transition counts at the FF (during scan shift mode) to the scan chain length.

The basic ideas of the proposed method are (1) to use the pattern-independent static power analysis for some reference SAs as a "Pre-Process" and (2) to use a linear interpolation to estimate the power consumption for other SAs from the known reference SAs computed in the pre-process, which is defined as follows.

A. Pattern-Independent Static Power Analysis

Power consumption depends on SAs of FFs and switching activities of other cells in the block. Since each cell activity in a block is influenced by FFs in the block and also by FFs in other blocks that are constitutionally connected to the cell, we estimate power consumption of the block using SAs of FFs in the block as well as those of the surrounding blocks. In order to take the two effects into account, we do the following two static power analyses using a power simulator as a pre-process step: (1) *baseline power analysis* to estimate the power caused by SAs of FFs in the block itself and (2) *dependence power analysis* to estimate what amount of the baseline power is affected by SAs of FFs in the surrounding blocks. We specify SA value of each FF for the power simulator and estimate the average power consumption including dynamic and leakage power in FFs as well as logic cells.

Baseline Power Analysis: We estimate the average power consumption of each block when SA of every FF in the circuit is as-



(a) Baseline power analysis

(b) Dependence power analysis

Figure 6. An example of the static power analysis.

sumed to be d%, where d is varied from 0% to 100% with 10% increment.

Dependence Power Analysis: We estimate the average power consumption in each block as follows. First, we fix SA value of a block to the average SA of the circuit for a given set of test patterns. Then, we vary SAs from 0% to 100% with 10% increment for FFs in other blocks.

Examples of the power analysis results obtained by the above pre-process are shown in Figure 6. The examples include the power analysis results of 4 among 16 blocks in the ITC'99 benchmark circuit $b17$ used in Section 2. In this example, the average SA for the given set of test patterns is 30%. Therefore, we see that the estimated power values for each block at 30% SA in Figure 6(a) are the same as those in Figure 6(b) because they are estimated when SAs of all the FFs in the circuit is 30%. For example, the estimated power consumption of block16 at 30% SA is 3.8×10^{-4} W in both Figures 6(a) and (b). However, even though SA of block16 is fixed to 30%, the power consumption of block16 is decreased to 2.8×10^{-4} W (26% decrease) when SAs of the surrounding blocks become 10% as shown in Figure 6(b). In Section 3.C, we use the ratio of the relative decrease (or increase) to the baseline power consumption as *dependence factor* to estimate the final power consumption.

From Figure 6, we observe that (1) power consumption in each block is not proportional to SA of the block, (2) power consumptions differ from one block to another even if they have the same SA and (3) power consumption in each block b_i is also affected by SAs of the other blocks even if the SA of b_i is fixed. This proves that the WTC in the scan chain is not accurate enough to manage the spatial power distribution. Note that the pattern-independent static power analysis is much faster than the flow explained in Section 3.2, and it is required only once for every circuit.

B. Linear Interpolation

Suppose that the two adjacent reference SAs for a block b_i collected in the baseline power analysis (shown in Figure 6(a)) or dependence power analysis (shown in Figure 6(b)) are given by the coordinates (x_a, y_a) and (x_b, y_b) where x and y represent the SA and the corresponding power consumption, respectively. For a SA_i in the interval (x_a, x_b), the corresponding power consumption

Table 1. Characteristics of benchmark circuits.

circuit	#FF	#gate	block	#sc	#pat	x ratio
b12	121	1847	3 × 3	9	102	0.789
b14	215	5579	3 × 3	9	497	0.910
b15	416	10093	3 × 3	9	451	0.949
b17	1317	32871	4 × 4	16	569	0.934
b20	430	10294	4 × 4	16	401	0.837
b21	430	10165	4 × 4	16	393	0.841
b22	613	15303	4 × 4	16	406	0.838

$P(i, SA_i)$ is linearly interpolated by the following equation.

$$P(i, SA_i) = y_a + (SA_i - x_a) \times \frac{y_b - y_a}{x_b - x_a} \quad (2)$$

We use $P_{base}(i, SA_i)$ and $P_{depend}(i, SA_i)$ for the linearly interpolated power consumption from the baseline power analysis and dependence power analysis, respectively.

C. Power Estimation Using Linear Interpolation

We present a way of estimating the power consumption in block b_i for a pair of subsequent test vectors. Suppose that SA_i and $SA_{i,adj}$ are the average SAs of FFs in b_i and the adjacent blocks to b_i, respectively. Then, for b_i, we estimate the power consumption P_i by the following equation

$$P_i = (1 + D(i, SA_{i,adj})) \times P_{base}(i, SA_i) \quad (3)$$

where $P_{base}(i, SA_i)$ is the baseline power consumption in b_i when SA is SA_i% computed using the linear interpolation and $D(i, SA_{i,adj})$ is the dependence factor of b_i on the adjacent blocks given by the following equation.

$$D(i, SA_{i,adj}) = \frac{P_{depend}(i, SA_{i,adj}) - P_{base}(i, SA_{ave})}{P_{base}(i, SA_{ave})} \quad (4)$$

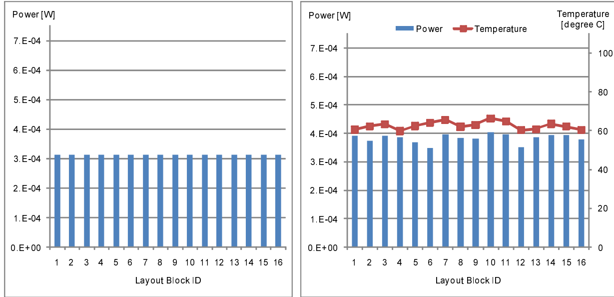
where SA_{ave} is the average SA of the circuit for a given set of test patterns.

The proposed method estimates the power consumption quickly and accurately since it uses only the switching activities of FFs and it is based on the static power analysis including dynamic and leakage power consumption in both FFs and logic cells. Therefore, it is used iteratively in a short time in the proposed framework to manage the spatial power distribution discussed in Section 3.2.

4 Experimental Results

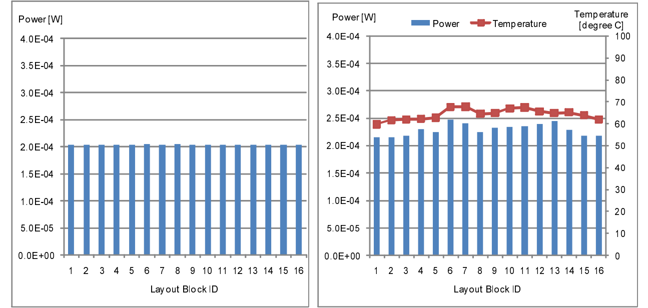
In this section, we present experimental results using several ITC'99 benchmark circuits. The X-filling technique uses the proposed power estimation method and tries to minimize the spatial power variation subject to minimizing overall power consumption, which leads to the thermal-uniformity at low temperature. Therefore, we present the following results.

- *Power Estimation Method*: we highlight the accuracy and effectiveness of the proposed power estimation method.
- *Power Consumption*: we highlight the relative differences in "power variance", "overall average power" and "maximum power" between the proposed and the existing X-filling techniques: minimum transition fill (min-fill), 0-fill, 1-fill, random fill (rand-fill) and maximum transition fill (max-fill). The relative difference in power variation is denoted by ΔV_{pwr} and it is computed as $\frac{V_{exist} - V_{pro}}{V_{exist}} \times 100$ where V_{pro} and



(a) Estimated power (b) Actual power and temperature

Figure 7. Power distributions for $b17$ by the proposed fill.



(a) Estimated power (b) Actual power and temperature

Figure 8. Power distributions for $b22$ by the proposed fill.

V_{exist} denote the power variance by the proposed and the existing X-filling techniques, respectively. The relative differences in overall average power and in maximum power are denoted by ΔP_{ave} and ΔP_{max}, respectively, which are computed in similar fashion to ΔV_{pwr}.

- *Temperature*: we highlight the relative differences in "temperature variance" and "peak temperature" between the proposed and the existing X-filling techniques. The relative differences in temperature variance and in maximum temperature are denoted by ΔV_{temp} and ΔT_{peak}, respectively, which are computed in similar fashion to ΔV_{pwr}.

We used the same flow as shown in Figure 1 to estimate power and temperature. In addition to that, the X-filling techniques are applied in between the steps of ATPG and logic simulation. We used the test sets with Xs generated by Synopsys TetraMAX with dynamic compaction as the initial test sets for X-filling. We also used a 45nm library [10] through the experiments. The characteristics of the circuits used in the experiments are listed in Table 1. In our experiments, we used $N \times N$ square layout blocks with the same size for the power and temperature analyses and assumed each block has one scan chain that consists of all of the FFs in the block. The 4th and 5th in Table 1 columns denote the number of layout blocks and scan chains in the circuit, respectively. The 6th and 7th columns denote the number of the initial test patterns with Xs and the corresponding X-ratio, respectively.

A. Power Estimation Method

The proposed method tries to minimize the power variation using the estimated power values presented in Section 3.3 instead of using the actual power. Figures 7(a) and 8(a) show the estimated power distributions used in the proposed X-filling method for $b17$ and $b22$, respectively. Figures 7(b) and 8(b) show the corresponding actual power and temperature distributions computed using the flow shown in Figure 1. Although the estimated power is slightly different from the actual power, it is accurate enough to manage spatial temperature variation. All experiments were performed on a 3.0 GHz AMD Opteron256 processor with 16 GB memory. The CPU times for the proposed X-filling was in the order of minutes.

B. Power Consumption

Table 2 shows the relative differences in spatial power variation ΔV_{pwr}, in overall average power consumption ΔP_{ave} and in maximum block power consumption ΔP_{max} between the proposed and the existing X-filling techniques. The results show that a significant reduction (72% on average) in spatial power variance was obtained using the proposed X-filling technique. In comparison with the low-power-oriented techniques such as minimum transition fill, 0-fill and 1-fill, we achieved up to 91% reduction and 70% reduction on average in power variance. On the other hand, the proposed method incurred around 35% increase in overall average power consumption compared to the low-power-oriented techniques. However, the overall average power consumptions of the proposed X-filling technique are still 20% lower than those of the random fill. Furthermore, the increase in maximum block power consumption is only around 2% compared to the low-power-oriented techniques. Since peak temperature is strongly correlated to the maximum block power consumption, and does not correlate to the average, the proposed X-filling technique can reduce the temperature variance significantly with a little increase in peak temperature (this will be shown in Section 4.C).

C. Temperature

Table 3 shows the relative differences in spatial temperature variation ΔV_{temp} and in peak temperature ΔT_{max} between the proposed and the existing X-filling techniques. The results show that a significant reduction in temperature variance was obtained using the proposed X-filling technique while preserving the peak temperature relatively at low level. In comparison with the random fill, we obtained not only 68% reduction in temperature variance but also 15% reduction in peak temperature. In comparison with the low-power-oriented X-filling techniques such as min-fill, 0-fill and 1-fill, we obtained around 68% reduction on average in temperature variance. Although the overall average power was increased by 35%, the increase in peak temperature was only less than 10% as we expected. The results also show that the power variation is strongly correlated to the temperature variation and the proposed power management framework based on X-filling effectively minimizes the variance with a little increase in peak temperature.

5 Conclusions

In this paper, we have shown the importance of achieving spatially uniform temperature distribution for accurate at-speed testing. We have presented an X-filling technique together with the fast and accurate power estimation method to manage the spatial variation both in power and temperature during manufactur-

Table 2. Reduction in power variance, average power and maximum power by the proposed X-filling technique.

circuit	min-fill			0-fill			1-fill			rand-fill			max-fill		
	ΔV_{pwr} (%)	ΔP_{ave} (%)	ΔP_{max} (%)	ΔV_{pwr} (%)	ΔP_{ave} (%)	ΔP_{max} (%)	ΔV_{pwr} (%)	ΔP_{ave} (%)	ΔP_{max} (%)	ΔV_{pwr} (%)	ΔP_{ave} (%)	ΔP_{max} (%)	ΔV_{pwr} (%)	ΔP_{ave} (%)	ΔP_{max} (%)
b12	88.1	-29.8	-0.6	91.3	-32.5	3.2	89.9	-28.2	2.4	85.7	9.7	15.5	89.6	29.4	24.3
b14	53.7	-39.2	5.7	55.9	-38.6	1.6	61.5	-28.4	7.8	57.9	18.2	17.3	79.6	34.7	35.7
b15	42.1	-58.9	-6.1	32.0	-67.6	-1.5	50.5	-51.9	0.5	71.3	21.4	10.5	85.4	42.5	33.1
b17	88.9	-64.1	-3.1	90.5	-56.1	-2.7	90.6	-59.1	-6.2	90.7	35.6	7.6	93.4	55.0	34.4
b20	66.5	-25.0	-3.6	71.1	-18.4	0.6	74.9	-19.6	2.3	67.4	18.4	14.5	75.4	34.1	29.7
b21	59.0	-26.3	-12.8	65.6	-24.9	-7.7	62.4	-18.2	-13.1	49.2	15.6	-0.4	75.4	32.1	20.0
b22	75.6	-26.5	-4.0	80.5	-20.0	0.6	81.6	-13.7	-1.3	61.7	19.5	7.0	66.2	35.6	19.3
average	67.7	-38.5	-3.5	69.6	-36.9	-0.8	73.1	-31.3	-1.1	69.1	19.8	10.3	80.7	37.6	28.1

Table 3. Reduction in temperature variance and peak temperature by the proposed X-filling technique.

circuit	min-fill		0-fill		1-fill		rand-fill		max-fill	
	ΔV_{temp} (%)	ΔT_{peak} (%)	ΔV_{temp} (%)	ΔT_{peak} (%)	ΔV_{temp} (%)	ΔT_{peak} (%)	ΔV_{temp} (%)	ΔT_{peak} (%)	ΔV_{temp} (%)	ΔT_{peak} (%)
b12	93.9	-2.3	95.6	-2.3	94.6	0.8	90.0	14.1	94.6	23.3
b14	61.0	-11.7	60.5	-8.9	66.5	-5.1	64.4	13.7	84.2	29.2
b15	48.6	-8.7	38.6	-17.5	58.0	-9.2	73.8	13.9	86.6	29.7
b17	75.5	-12.4	79.5	-8.9	79.2	-9.7	86.3	27.5	90.8	45.1
b20	52.4	-9.3	61.0	-1.7	67.2	-3.1	65.2	14.2	72.5	24.7
b21	56.3	-9.3	64.9	-6.7	59.7	-5.6	47.2	9.3	73.6	22.4
b22	63.9	-5.5	70.8	-0.4	73.7	2.0	57.9	15.1	65.2	25.7
average	64.5	-8.5	67.3	-6.6	71.3	-4.3	69.3	15.4	81.1	28.6

ing test. The experimental results show that the proposed method minimizes the variation in power and temperature while preserving them relatively at low level. Since the proposed method minimizes the delay variation caused by the temperature differences, it is effective to increase accuracy of at-speed delay testing.

One of the future works is to extend the proposed framework so that the power distribution in testing mode can be controlled to match with that in functional mode to reflect the actual delay variation in testing mode.

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