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Scan Cell Reordering to Minimize Peak Power during Test Cycle: A Graph Theoretic Approach

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SUMMARY

Scan circuit is widely practiced DFT technology. The scan testing procedure consist of state initialization, test application, response capture and observation process. During the state initialization process the scan vectors are shifted into the scan cells and simultaneously the responses captured in last cycle are shifted out. During this shift operation the transitions that arise in the scan cells are propagated to the combinational circuit, which inturn create many more toggling activities in the combinational block and hence increases the dynamic power consumption. The dynamic power consumed during scan shift operation is much more higher than that of normal mode operation.

Due to change in design characteristic the dynamic power dissipated during scan operation becomes an important issue. The average power and peak power are the standard metric to measure dynamic power. During scan test both average power and peak power are required to be within the specified power budget for safe testing of chip. Average power causes excessive heat dissipation where as peak power causes IR drop and cross talk problem. Particularly, the excessive peak power during *test-cycle* of at-speed testing is vulnerable. The excessive peak power causes high rate of current in the power and ground rails which decreases the supply voltage and causes ground bounce, this phenomenon is known as IR-drop. The larger IR-drop means the worse speed performance of circuit. This degradation in performance grows if circuit is operated at high frequency which is the case during at-speed testing. This degradation in performance leads to incorrect capture of responses and this results in to undesired yield loss.

Hence, to avoid yield loss the the peak power minimization is necessary especially in case of narrow *test-cycle*. More over the minimization of peak power is also advantageous for parallel testing of multiple core to reduce test time.

In this work we have focused on the problem of peak power consumption during *test-cycle* for at-speed testing. The methodology proposed in this work is based on scan cells reordering.

Many direction has been explored to reduce peak power during *test-cycle*. One of the methodology on scan reordering is proposed by Bonhomme et al. [1]. The methodology is formulated as a global optimization problem and solved using simulated annealing approach. Although the simulated annealing can provides near optimal solution - if it is allowed to run for suffcient number of iteration - the graph theoretic formulation will wider the solution space for scan reordering methodology. With this motivation we are proposing a graph theoretic formulation for scan reordering methodology to minimize peak power during *test-cycle*.

The overall approach consists of graph theoretic problem formulation and an algorithm to solve it. From given scan related informations viz. scan cells, possible scan path, and power consumption a complete *vector-weighted* graph is constructed. The *vector-weight* is a weight of an edge which keeps the information of peak power consumed by each test vector. On this graph a TSP (Travelling Sales Person) problem is formulated. The cost function in this formulation is peak power. The problem formulated is NP-complete. As the problem is NP-complete we have proposed a greedy based heuristic to solve it.

The proposed heuristic consists of two parts. Part 1 to find a Hamiltonian cycle which consume less peak power from the constructed complete graph and Part 2 to find a Hamiltonian path having lower peak power from Hamiltonian cycle. The Part 1 of algorithm runs in polynomial time and the Part 2 runs in linear time. The memory space required to execute these alorithms is also linear.

The experiment conducted on ITC99 and ISCAS89 benchmarks show that the proposed methodology is able to reduce appreciable percentage (around 55%) of peak power compared to [1].

Overall, this paper has proposed a novel way of formulating a graph theoretic problem for scan reordering to minimize *test-cycle* peak power. The scan reordering methodology may incur nominal area overhead in terms of routing and may alter the delay fault coverage for at-speed skewed-load testing. In this work we have not taken these parameters into account. However, the proposed methodology can be extended to consider these parameters. One limitation of the scan reordering methodology is it is pattern dependent. If some additional pattern has to be added on top of the existing patterns the methodology will not be able to reduce peak power effectively. This issue needs further examination.

REFERENCES

[1] N. Badereddine et al., "Scan cell reordering for peak power reduction during scan test cycles," IFIP Iinternational Federation for Information Processing, vol. 240, pp. 267-281, 2007

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