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Test Pattern Selection to Optimize Delay Test Quality with a Limited Size of Test Set

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***Abstract*—Timing-aware ATPGs are being developed to detect small delay faults for high defect coverage for current nanometer VLSI design. However, it results in a large test set compared with test generation targeting traditional fault models. This paper proposes a method to get a limited size of test set with high delay test quality based on statistical delay quality level (SDQL).**

I. Introduction

We address the problem to generate a small test set with high delay test quality. Unlike related works [1], [2], we adopt statistical delay quality level (SDQL)[3] as a delay test quality. The SDQL shows the amount of delay defects that should be detected but cannot be detected. It is defined as follow.

$$SDQL = \sum_{f \in N} \int_{T^f_{mgn}}^{T^f_{det}} F(s)ds \qquad (1)$$

In the definition, N is the total number of faults, $F(s)$ is a delay defect distribution function and T^f_{mgn} and T^f_{det} are the minimum delay defect sizes of a fault f that can affect system behavior and is detected by a given test set, respectively.

II. Test Set Selection Method

To generate a test set with the minimum SDQL under a constraint on test pattern count, 1) we first generate *a base test set* T_{base} according to some criteria, then 2) select the required number of test patterns from T_{base}. The proposed selection method first obtains, for each test pattern, an SDQL value and the minimum delay defect sizes detectable by the pattern for all the faults and select a test pattern with the minimum SDQL as the first pattern. From the second pattern, we efficiently select test patterns one by one based on the descrease of the sum of $T^f_{det} - T^f_{mgn}$ for all the faults.

Experiments. We evaluated the proposed selection method by comparison with two methods: 1) generate a limited number of test patterns by ATPG (ATPG order) and 2) select a test pattern from T_{base} based on transition fault coverage (coverage based). We used TetraMAX(Synopsys) and SunFireX4100 (3.0GHz CPU and 16GB memory, Sun Microsystems). Table I shows the results for ITC benchmark circuits. Figure 1 shows the improvement of SDQL value from the SDQL value for an empty test set, where T_{base} is generated by timing-aware ATPG. From these results, we can find that the proposed method efficiently improves SDQL. Next, we compared several ATPGs to find a suitable base test set. Figure 2 shows the SDQL improvement for b19. We can find that timing-aware ATPG is suitable to obtain high delay test quality.

TABLE I
Base test set generation and selection results.

circuit	#faults	#patterns	TGT(s)	selection time(s)	
				proposed	coverage
b14	22,904	1,325	2,429.06	195.89	28.15
b15	26,428	1,793	439.21	80.34	20.72
b17	80,612	5,745	2,193.66	602.93	198.74
b18	223,312	13,030	32,898.94	5,559.22	1,312.01
b19	433,410	24,058	103,917.61	26,556.51	5,342.22
b20	46,538	3,894	14,542.42	1,094.56	173.23

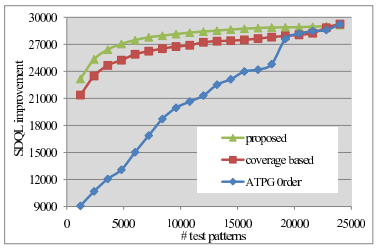

Fig. 1. SDQL and selection method for b19.

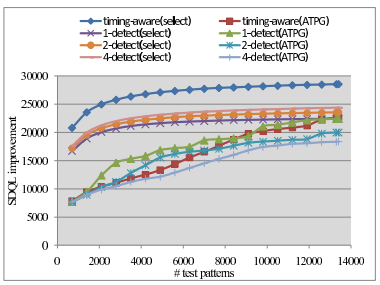

Fig. 2. SDQL and base test set for b19.

References

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