F-Scan Test Generation Model for Delay Fault Testing at RTL using Standard Full Scan ATPG

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Abstract—**We propose a new test generation method for F-scan delay fault testing that uses standard full scan delay fault automatic test pattern generation (ATPG). This method shows that it is possible to generate test patterns fast for F-scannable register-transfer level (RTL) circuits by using currently well-developed and high-performance commercial ATPG tools for gate-level scan circuits.**

I. Introduction

F-scan [1], [2] has been proposed as a new DFT technique that utilizes available functional nodes and paths in a register-transfer level (RTL) circuit for testing. It is proven to be better than full scan in terms of area overhead, test application time, and reduction of overtesting. Since we employ constrained ATPG [2], only valid patterns can be generated for F-scan. We have extended to a hybrid model for F-scan delay fault ATPG that achieves high fault coverage in [3]. The test patterns can be automatically applied to F-scannable circuits at-speed because of the RTL DFT mechanism, hence, there are no difficulties for the scan-enable timing. However, this method is incomplete because using the two-time frame model with constraints takes too much effort and time during test generation. In order for F-scan to be practically applicable to today's circuits, there is a need for it to be integrated to the available technology. Hence, we complete the F-scan delay fault test generation model in this work.

II. Delay Fault ATPG for F-Scan Design

The proposed F-scan test generation model (FTGM) for delay faults also uses the hybrid approach, which can produce both skewed-load and broadside test patterns. However, instead of using the two-time frame combinational stuck-at ATPG, the new method uses standard full scan delay fault ATPG.

In order to make the gate-level F-scannable circuits compatible with full scan delay fault ATPG, we add full scan chains "tentatively" during the test generation phase. The order of the flip-flops on full scan chains are determined according to the F-scan-paths. The full scan chains will be used during delay fault ATPG only. Application of tests will still be at RTL. The full scan chains are not needed during test application because the F-scannable circuits are already integrated with F-scan-paths to be used for scanning-in and -out test data. The only purpose of the full scan chains is to make ATPG faster, thus the flip-flops in a "physical" F-scannable circuit are not converted to scan flip-flops. The FTGM for delay fault testing proposed in this paper is shown in Fig. 1.

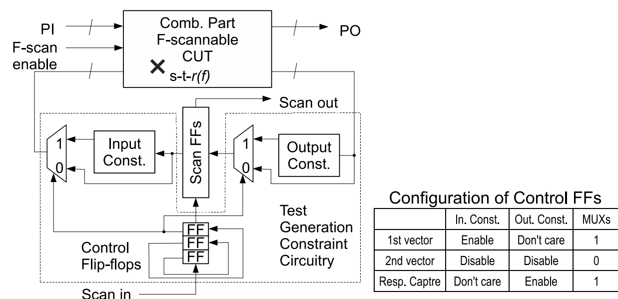

Fig. 1. F-scan test generation model for delay fault testing using standard full scan delay fault ATPG.

TABLE I
Number of Faults, Fault Coverage, and Test Generation Time.

Ckt	Hybrid Full Scan			Hybrid FTGM			New FTGM		
	#Faults	FC	TGT (CPU sec.)	#Faults	FC	TGT (Elapsed sec.)	#Faults	FC	TGT (CPU sec.)
b03	852	97.77%	0.10	1074	99.35%	95.18	978	99.69%	0.05
b04	2620	94.66%	155.71	3116	96.37%	2001.10	2954	96.21%	0.72
b06	402	97.51%	0.01	566	98.23%	45.70	562	98.75%	0.72
b07	1694	97.17%	3.24	2142	96.69%	57.50	2002	99.30%	1.59
b08	814	96.44%	0.06	1046	99.81%	115.30	702	99.95%	0.12
b09	784	99.62%	1.91	1080	98.52%	101.60	948	99.79%	0.31
b10	858	97.20%	0.07	1122	99.91%	140.80	1086	100%	0.03
b11	2072	95.22%	14.31	2464	99.03%	480.00	2378	99.20%	0.70
b13	1756	97.10%	0.30	2214	96.03%	531.00	2080	99.09%	0.31

III. Experiments

In the experiments, we compare test quality and test generation time required to the following: full scan with broadside and skewed-load ATPG (Hybrid Full Scan); the previous F-scan with FTGM using combinational stuck-at ATPG (Hybrid FTGM); and our proposed F-scan with FTGM using standard full scan delay fault ATPG (New FTGM) using ITC'99 RTL Benchmark Circuits.

IV. Conclusion

From the above results, it is shown that the proposed TG method dramatically improves test generation time compared to that of the previous method and that it is comparable with or faster than standard full scan delay fault test generation.

References

[1] M. E. J. Obien and H. Fujiwara, "F-Scan: An approach to functional RTL scan for assignment decision diagrams," Proc. IEEE 8th Int. Conf. on ASIC, pp. 589-562, Oct. 2009.
[2] M. E. J. Obien, S. Ohtake and H. Fujiwara, "Constrained ATPG for functional RTL circuits using f-scan," 2010 IEEE International Test Conference, Paper 21.1, pp.1-10, Nov. 2010.
[3] M. E. J. Obien, S. Ohtake and H. Fujiwara, "Delay fault ATPG for f-scannable RTL circuits," IEEE International Symposium on Communications and Information Technologies (ISCIT'10), pp. 717-722, Oct. 2010.

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