Temperature-Variation-Aware Test Pattern Optimization

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***Abstract*—For accurate failure prediction, it is important to eliminate the environmental delay variations from the measure delays for capturing the actual delay shift caused by aging. This paper presents a novel test pattern optimization method to reduces spatial and temporal temperature variations during delay test.**

I. Introduction

In nanometer technologies, the temperature-induced delay variations during test is as much as that is caused by on-chip process variations [1]. Temperature difference between different locations in a circuit can be as high as 40°C to 50°C, and typical time intervals for temperature changes over time are very short time of milliseconds. Besides, the execution of on-line self-test may last for a long time [2]. For example, the extremely thorough test patterns that specifically target aging [3] may take several seconds to run. This indicates that, for accurate failure prediction, we need to embed a lot of temperature sensors into several locations within a chip to collect spatially and temporally accurate temperature profile during test. However, this is not the cost effective solution since it incurs a lot of overhead. Even if we could accept the overhead, it requires (1) a lot of data to be stored in the memory and (2) a complex procedure to eliminate the temperature induced delay variations from the measured delay values for failure analysis. Therefore, we need a cost effective solution to eliminate the spatial and temporal temperature-induced delay variations for accurate failure prediction.

II. Test Pattern Optimization

The proposed method consists of the following two steps: (1) X-filling and (2) test pattern ordering. The proposed method starts with a test sequence including unspecified bits (X's) generated by a commercial ATPG. In Step1, the thermal-uniformity-aware X-filling technique [4] is performed so as to minimize the spatial temperature variance. Step2 determines an order of the test patterns so that the temporal temperature variance is minimized while preserving the spatial temperature variance achieved in the first step. The main idea is to adopt a sub-sequence-based ordering strategy, not pattern-by-pattern ordering, and minimize the number of sub-sequences used for the ordering. The spatial thermal-uniformity achieved in Step1 is valid only for the current response-pattern pair which are simultaneously shifted in the original test sequence. Therefore, the sub-sequence-based ordering itself can preserve the spatial thermal-uniformity without any consideration if the length of sub-sequences is long enough, and focus our efforts on minimizing the temporal temperature variance. This simplification reduces the computational cost of this step significantly.

TABLE I
Reduction in spatial and temporal temperature variance by the proposed method.

circuit	[4] ΔV_T^{spa} (%)	[4] ΔV_T^{temp} (%)	min-fill ΔV_T^{spa} (%)	min-fill ΔV_T^{temp} (%)	0-fill ΔV_T^{spa} (%)	0-fill ΔV_T^{temp} (%)	1-fill ΔV_T^{spa} (%)	1-fill ΔV_T^{temp} (%)
b12	17.5	80.6	94.6	92.5	96.0	94.0	93.9	93.2
b14	7.3	90.8	73.4	95.3	70.4	97.1	75.4	96.6
b15	6.3	97.5	56.0	97.7	63.2	98.1	62.3	98.3
b17	3.4	96.2	86.7	94.5	87.8	96.1	88.6	95.0
b20	2.2	86.6	60.5	95.4	67.4	95.5	68.3	95.5
b21	4.6	93.6	69.0	96.1	71.2	97.1	66.2	96.5
b22	3.1	94.3	74.7	96.4	77.2	96.8	79.6	96.6

III. Experimental Results and Conclusion

Table I shows the relative differences in "spatial temperature variance ΔV_T^{spa}", "temporal temperature variance ΔV_T^{temp}" and "peak temperature ΔT_{max}" between the proposed method and the existing X-filling techniques for several ITC'99 benchmark circuits. The results show that the proposed test pattern optimization method effectively reduces the spatial and temporal variations. Since the proposed method consists of the thermal-uniformity-aware X-filling and test pattern ordering for given test sequences with unspecified bits, it is easily embedded into the current design flow without any loss of fault coverage.

Acknowledgments

This work was supported in part by Japan Society for the Promotion of Science (JSPS) under Grants-in-Aid for Young Scientists(B)(No.21700059).

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