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The Past and Future of WRTLT

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Abstract—**The paper recalls the establishment, and development of the IEEE workshop on RTL and High Level Testing. This workshop has run for 12 years, and has brought researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL) and high level testing. However, since nano-scale ICs are confronting material and fabrication technology challenges, it might be hard for computer scientists to provide new ideas on this kind of ICs testing. In addition, many people pay attention to paper publication, which is not a major issue for a workshop. In order to re-activate the workshop, authors suggest some ideas for consideration.**

Keywords- RTL testing, high level testing, functional testing

I. HISTORICAL RETROSPECT

At the very beginning of this new century, 2000, the first IEEE Workshop on RTL ATPG & DFT was held in Hunan University, Changsha, China. It took place in a room with a Statue of Confucius in Yuelu Academy, what so called a one thousand year university, although we discussed modern IT technology in English over there.

In 2002, WRTLT changed its title to Workshop on RTL and High Level Testing, since we understood that RTL testing and even further high level testing were more important than before, as the IC complexity and technology has been largely advanced. Most of the workshops have been conjunction with ATS, and had a number of attendees.

In recently years, nanoscale IC industry requires more material and fabrication technologies. Computer scientists may feel they could not help much in these areas. And then the submitted papers for WRTLT are not as many as expected, and many of those submissions are not related to RTL or high level testing. We think it is time for us to re-activate the workshop, and to make it boisterous.

II. RE-CONSIDERING RTL AND HIGH LEVEL TESTING

In 1993, an ITC panel titled "Fault Coverage Numbers: What Do They Mean?" attracted about 400 people to discuss the use of fault models [1]. Fault model-based testing was proposed more than 40 years ago when ICs or PCBs were relatively small. Fault models are used for ATPG and test metrics. With the advance of IC density, complexity and technology, many defects cannot be reflected by stuck-at faults (SAF). Delay faults are one kind of the defects, which cannot be detected by stuck-at fault tests. People suggest path delay fault model, which is not practical due to its complexity, and then transition delay fault model was applied. However, even if 100% transition delay fault coverage does not mean free of delay faults, although it is easy to generate tests for transition delay faults by using some variant of SAF ATPG. This is to say SAF model is not sufficient for modern IC testing. But, on the other hand, it is interesting to note that industry experiments show that some 100% SAF fault coverage leads ICs under test to be overtested.

SAF testing is then extended to RTL and high level testing for design verification and product testing. In fact, a superscalar processor with superpipeline and reorder buffer cannot be tested as a combinational circuit, and even as a sequential circuit, whose sequential depth may reach to 1000, and even much high. In this case, we cannot be restricted ourselves to SAF model and have to consider timing, power, signal integrity and etc. Therefore, functional testing, and even system testing are necessary and feasible. A functional test uses a large test sequence or a test program designed to functionally verify operations at the design frequency. The problem is when the functional testing is sufficient to stop, similar to a problem of software testing. To test or verify a SystemC design, it is very difficult to count how many faults or bugs there are, but desirable to have more faults or bugs to be detected.

Companies have experience in system-level testing (SLT) [2]. For most companies, SLT is to avoid unnecessary cost. Nvidia reported how SLT can potentially save test cost by reducing fault yield loss, as correlation data suggests there is less overkill with SLT. Nevertheless, replacing Final Test on ATE with SLT may be a better option. Then, SLT test generation is an issue. Although very high coverage structural testing is applied at wafer sort and final test, still many faulty chips escape from testing, and later caught at SLT. Functional testing is then important to reduce DPPM (defect parts per million), but requires much longer test durations. However, test duration for functional testing is not as costly as structural tests applied to automatic test equipment (ATE). On the other hand, when a customer rejects a product, a true test escape should be identified, and avoided for the coming products. System-level testing techniques are then important. It not only activates functional testing, but also some parameter measurements involved.

There are a number of challenges for scan design [3]. The i.MX21 applications processor from Freescale includes an ARM926EJ-S core and a host of peripherals. The i.MX21 does not have boundary-scan capability [4]. But, some build-in functional testing facilities are available.

From the whole process of IC production point of view, adaptive test in the Model-View-Controller Paradigm [5] is an effective approach to stabling production process. The "model" is a means of abstracting data into standardized structures as a layer above low-level relational databases, which can be considered as high-level database abstractions, and allow the low-level databases to take care of database infrastructure. The assertion-based verification is a verification methodology based on instrumenting the design with assertions. These assertions are checked by simulation, emulation and formal verification.

Now, at RTL level, system Verilog assertions are still under the way for standardization [6], which allows some of the ATE functions to be embedded in circuits including built-in memory, logic, and I/O test engines; temperature and voltage monitors; debug instruments such as logic analyzers, scopes, and trace buffers. Those developments show that industry provides a broader perspective to consider the whole IC production process from design, manufacturing, testing and packaging to improve productivity, instead of only consider testing at gate level.

III. CHALLENGES IN WRTLT

This is the 13rd workshop on RTL and high level testing. We have had many attendees to discuss problems and present papers at the previous 12 workshops. It should be noted that workshop is not a good place for paper publication, but a good opportunity for discussions among our test community. A successful example is the IEEE semiconductor wafer test workshop (SWTW) in South California. It celebrates its 23rd year now. The workshop is the only IEEE Components, Packaging, Manufacturing Technology (CPMT) Society event that focuses on all the aspects associated with microelectronic wafer and die level testing. The conference has a mixture of manufacturer and vendor presentations. It is not a sales show, nor an academic or theoretical conference. It is a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas. It often gathers hundreds of attendees without proceedings, but a heated discussion. The success comes from two reasons. First, attendees have common interests in searching for new research directions, new industrial experiences, and new ideas. Second, it is attractive for manufacturers and vendors to attend due to interesting discussions.

Functional testing was proposed in 1980's, such as [7], which was based on functional fault models, as that at gate level. However, this approach is not successful, because functional faults are various, and very hard to model and to classify. What we need is to check functions to be implemented. That is function-oriented, rather than fault-oriented, as software testing does. The problem is how long we should take to test a product, which is just a big problem of software testing. We appreciate testing tools capable of detecting more faults than the others by tracing the testing process.

Software testing means not only testing software, but also testing hardware by using some specific software. This approach is especially suitable for testing complex superscalar processors, as long as high level descriptions are available.

System testing is a kind of high level testing technique. It tests hardware and software as a whole. Recent systems are highly integrated, such as SOCs. Testing at system level avoids unnecessary cost and being overtested, and also helps locating faults for rejected parts. It depends on high level description including model checking, a wide spread technique.

For high level testing, it is very important to have testing coverage metrics, which is always challenged. A common question is how high stuck-at fault coverage can be achieved. Unfortunately, SAF coverage is no longer a good metric for advanced nano-scale chips and systems testing. But what is the better one? Or to predicting testing quality by tracing the test process instead.

Delay testing is critical for high speed ICs. Functional delay testing can be a way of path selection. In addition, verification testing and secure testing are also in consideration.

All those and many other high level testing techniques are of wide concern, and in rapid development, and might be major themes of coming WRTLT.

IV. SUMMARY

In order to attract more manufacturers and vendors involved in the workshop, we suggest select a specific theme for each WRTLT. The theme may encourage people to focus on challenges and discussions around the theme. We can invite some industry people to give an opening presentation of the theme, so that a heated discussion will follow. During the call for papers stage, we should call for session proposals, such as panel session proposals or special session proposals. The proposer is invited, and all panelists and special session contributors are collected by the proposer, and named invited speakers.

Finally we would like to hope WRTLT becomes a more active event, and has its bright future.

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