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UNIVERSAL TEST SETS FOR PROGRAMMABLE LOGIC ARRAYS

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Abstract

In this paper, the problem of fault detection in easily testable programmable logic arrays (PLAs) is discussed. The easily testable PLAs will be designed by adding extra logic. These augmented PLAs have the following features: (a) for a PLA with n inputs, m columns (product terms) and ℓ outputs, there exists a "universal" test set such that the test patterns and responses do not depend on the function of the PLA but depend only on the size of the PLA (the values n, m, and ℓ); (b) the number of tests is of order n+m. For the augmented PLAs, universal test sets to detect faults in PLAs are presented. The types of faults considered here are single and multiple stuck faults and cross-point faults in PLAs. Fault location and repair of PLAs are also considered.

I. Introduction

With the increasing circuit density in a single large scale integrated (LSI) circuit chip, the difficulty of testing the circuits is becoming apparent. In order to overcome this problem, methods have been suggested in which test points and additional logic are used for the purpose of easing the test generation problem [1]-[3]. Designing easily testable circuits, one should pay attention to the following features: (a) the cost of generating test patterns is low, that is, the computation time for test generation is short; and (b) the cost of testing the circuits is low, that is, the length of test sequences is short.

This paper is concerned with the problem of fault detection and location in the easily testable programmable logic arrays (PLAs) which have the abovementioned features. The PLA, which is conceptually a two-level AND-OR, is attractive in LSI due to its memory-like array structure. A method is presented to augment PLAs by adding extra logic so that the augmented PLAs have the following easily testable features: (a) for a PLA with n inputs, m columns (product terms) and ℓ outputs, there exists a "universal" test set such that the test patterns and responses do not depend on the function of the PLA but depend only on the size of the PLA (the values n, m, and ℓ); (b) the number of tests is of order n+m. Since the augmented PLAs have the universal test set, the test genèration of PLAs is no more necessary, and the cost of test generation is considerably reduced to almost zero. The augmented PLAs introduced in this paper is similar to the PLA which was independently obtained by Hong and Ostapko [3]. However, since the augmented PLAs considered in this paper is somewhat different from [3] and also since no test sequence for multiple faults appears in [3], we will present universal test sequences for single and multiple faults in the PLAs. First, single stuck faults and single cross-point faults are considered, and the universal test sets to detect these faults in PLAs are presented. Then, the types of faults are extended to multiple faults. Fault location and repair of PLAs are also considered where the faults are assumed to be multiple cross-point faults.

II. Programmable Logic Arrays

A programmable logic array (PLA) consists of three main parts. These are the decoders, the AND array and the OR array. The decoders are usually implemented by single-bit decoders or double-bit decoders as shown in Figures 1 or 2. Both the AND array and the OR array are used to implement multi-output combinational logic with sum-of-products forms. Fig. 3 shows an example of a 4-input, 2-output PLA with single-bit decoders, which realizes two functions in the following:

$$f_1 = x_1 \vee x_4 \vee \bar{x}_2\bar{x}_3 \vee \bar{x}_1x_2x_3$$

$$f_2 = \bar{x}_2 \vee x_4 \vee x_1\bar{x}_3 \vee \bar{x}_1x_2x_3$$

Fig. 4 shows another realization using a PLA with double-bit decoders.

In the following sections III and IV, we present a method to augment PLAs with single-bit decoders or double-bit decoders by adding extra logic so that the augmented PLAs are easily testable PLAs with short "universal" test sequences. The types of faults considered in Sections III and IV are single faults in the PLA which are the stuck faults and the cross-point faults. A cross-point fault in a PLA is a fault such that the presence (absence) of a contact between a row and column of the PLA becomes the absence (presence) of the contact.

III. Augmented PLAs with Single-Bit Decoders

In order to design an easily testable PLA with single -bit decoders, we augment a given PLA by adding extra logic, that is, a shift register, two

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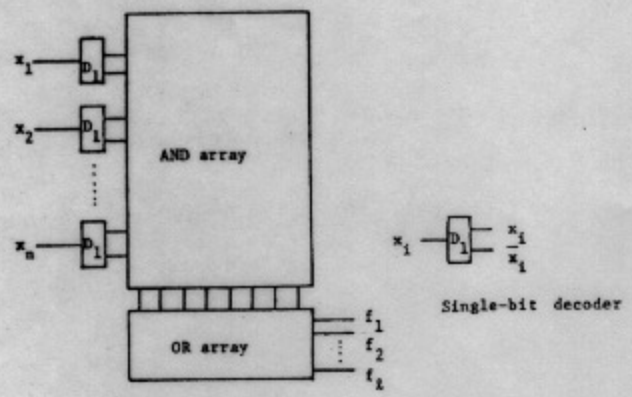

Fig. 1 PLA with single-bit decoders

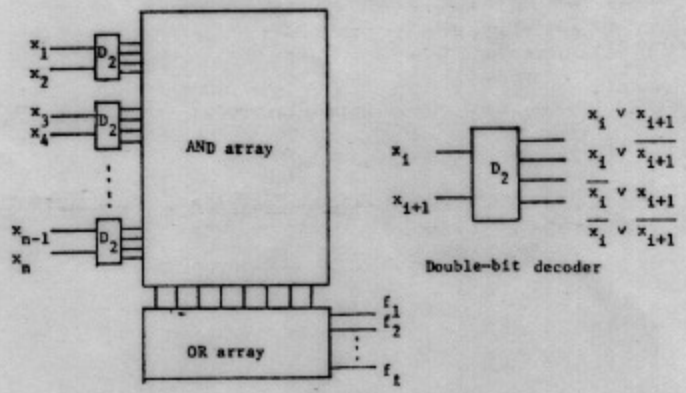

Fig. 2 PLA with double-bit decoders

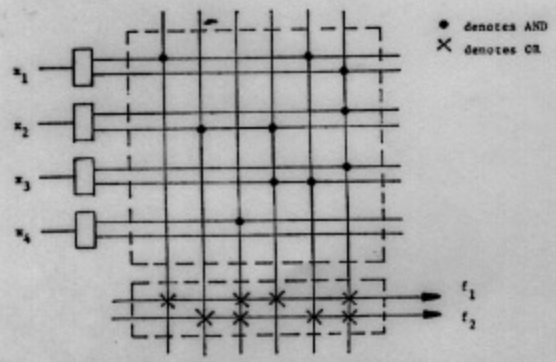

Fig. 3 Example of PLA with single-bit decoders

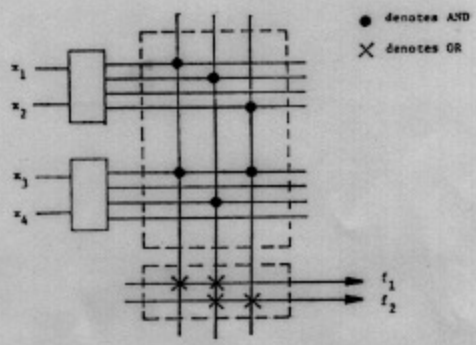

Fig. 4 Example of PLA with double-bit decoders

cascades of EORs (Exclusive ORs), and one column and one row to AND and OR arrays, respectively, as shown in Fig.5. The connections of the added column in the AND array is arranged so that each row of the AND array has an odd number of connections. Similarly, the connections of the added row in the OR array is arranged so that each column has an odd number of connections. In the augmented PLA, each column (product term) b_i is ANDed by each variable S_i of the shift register as follows:

$$b_i = p_i.S_i \quad \text{for } i=1,2,\ldots,m$$

where p_i is a product term generated by the ith column of the AND array without the shift register, and m is the number of columns. Fig.5 shows a PLA augmented from the PLA shown in Fig.3.

The augmented PLA has the following properties:

(1) The shift register can be used to select an arbitrary column of the AND array by setting 1 to the selected column and 0 to all other columns. (See Fig.6-a).

(2) The augmented decoders with control inputs y_1 and y_2 can be used to sensitize an arbitrary row of the AND array by setting 0 or 1 to the selected row and 1 to all other rows. (See Fig.6-b).

(3) The cascade of EORs under the OR array can be used as a parity checker to detect single errors in the sensitized row of the AND array. (See Fig.6-c).

(4) The cascade of EORs on the left of the OR array can be used as a parity checker to detect single errors in the sensitized column of the OR array. (See Fig.6-d).

Utilizing the above properties of the augmented PLA we can present a universal test set to detect single faults in the following:

(1) Stuck faults on the input or output lines or gates within the decoders, the AND array; and the OR array.

(2) Cross-point faults in the AND and OR arrays.

Table 1 shows the test set $A_{n,m,\ell}$ to detect the above types of faults, where n is the number of inputs, m is the number of columns in the AND array, ℓ is the number of rows in the OR array, and

$$\epsilon_m = \begin{cases} 0 & \text{if } m \text{ is even} \\ 1 & \text{if } m \text{ is odd} \end{cases}$$

and " - " represents don't care.

For this test set $A_{n,m,\ell}$, we have the following theorem.

Theorem 1: Let $M_{n,m,\ell}$ be an augmented PLA with single-bit decoders which has n inputs, m columns in the AND array and ℓ rows in the OR array. For any $M_{n,m,\ell}$, the test set $A_{n,m,\ell}$ can detect all single stuck and cross-point faults in the decoders, AND array and OR array.

Proof: When we apply test inputs I^0_{2j} and I^1_{2j} the jth column is set to 1 and other columns are all set to 0. Therefore, both I^0_{2j} and I^1_{2j} can detect any cross-point fault on the jth column of

the OR array and any stuck fault on the rows of the OR array by observing the output Z_2, and a stuck-at-0 fault on the jth column, stuck-at-1 faults on the other columns and stuck-at-0 faults on the rows of the AND array by observing the output Z_1.

By applying test I^0_{3i} (I^1_{3i}), the (2i-1)st (2ith) row of the AND array is set to 0 and other rows are all set to 1. Therefore, test I^0_{3i} (I^1_{3i}) can detect all cross-point faults and a stuck-at-1 fault on the 2i-1 st (2i th) row in the AND array by observing the output Z_1.

Tests I^0_{2j}, I^1_{2j} (j=1,2,...,m) and I^0_{3i}, I^1_{3i} (i=1, 2,...,n) can also detect all stuck faults in the decoders. The stuck-at-0 faults on the input lines of OR gates can be detected by I^0_{2j} and I^1_{2j} (j=1,2, ...,m). The stuck-at-1 faults on the input lines of OR gates can be detected by I^0_{3i} and I^1_{3i} (i=1,2, ...,n). The stuck-at-0 faults on the input lines x_i (i=1,2,...,n), y_1 and y_2 can be detected by I^0_{2j} and I^1_{2j} (j=1,2,....,m). The stuck-at-1 faults on the input lines x_i (i=1,2,...,n),y_1 and y_2 can be detected by I^0_{3i} and I^1_{3i} (i=1,2,...,n).

Q.E.D.

Next, we will show that the test set $A_{n,m,\ell}$ can also detect any multiple stuck fault in the Exclusive-OR cascades under the fault assumption that permits only stuck-type faults on the external input and output lines of EOR gates, that is, no fault within EOR gates is considered.

Lemma 1: For an Exclusive-OR cascade realization of a k-input linear function, all multiple stuck faults on the external lines of EOR gates can be detected by the following k+1 tests:

$$t_0 = (0,0,.....,0)$$
$$t_1 = (1,0,.....,0)$$
$$t_2 = (0,1,0,.....,0)$$
$$\vdots$$
$$t_k = (0,0,.....,0,1)$$

Lemma 2: If k input vectors are linearly independent, then these k vectors plus zero vector are sufficient to detect any multiple stuck fault on the external lines of EOR gates in a k-input Exclusive-OR cascade.

Let $M_{n,m,\ell}$ be an augmented PLA, and let C_1 and C_2 be the cascades of EORs having the output Z_1 and Z_2, respectively, in the augmented PLA shown in Fig.5. Let $M_{OR} = [a_{ij}]$ be a matrix of ℓ rows and m columns where

$$a_{ij} = \begin{cases} 1 & \text{if there exists a link at the (i,j)-th position of the OR array, and} \\ 0 & \text{otherwise} \end{cases}$$

By Lemmas 1 and 2, we have the following theorem for the multiple faults in two cascades of EORs, C_1 and C_2.

Theorem 2: The tests I_{11}, I^0_{2j} (j=1,2,...,m) in $A_{n,m,\ell}$ are sufficient to detect all multiple stuck faults in C_1. If the column rank of matrix M_{OR} is ℓ, then all the multiple stuck faults in C_2 can be detected by tests I_{11}, and I^0_{2j} (j=1,2,...,m) in $A_{n,m,\ell}$.

Using the test set $A_{n,m,\ell}$, we can construct a test sequence for the augmented PLAs as follows:

$$\alpha_{n,m,\ell} = I_{11}\, I^0_{21} I^0_{22} \cdots I^0_{2m} I^1_{21} I^1_{22} \cdots I^1_{2m}$$
$$U_1 U_2 \cdots U_{m-1} I^0_{31} I^0_{32} \cdots I^0_{3n} I^1_{31} I^1_{32} \cdots I^1_{3n}$$

where the test pattern U_i (i=1,2,...,m-1) is defined as

	$x_1 \cdots x_n$	$y_1 y_2$	$S_1 S_2 \cdots S_i S_{i+1} \cdots S_m$	Z_1	Z_2
$U_i =$	- ...-	1 1	1 1 ...1 0 ... 0	ε_i	-

The test sequence $\alpha_{n,m,\ell}$ can also detect the shift function of the shift register as well as all single stuck and cross-point faults in the PLA. The length of the test sequence is 2n+3m.

Now, we have presented the test set and the test sequence for the augmented PLAs. Both the test set $A_{n,m,\ell}$ and the test sequence $\alpha_{n,m,\ell}$ have the following advantages of easy testability. The test $A_{n,m,\ell}$ does not depend on the connection pattern of the PLA but depends only on the values n, m and ℓ, that is, the test patterns and responses are uniquely determined only by the size of the PLA. Therefore, the test set $A_{n,m,\ell}$ is " universal ". We can also see that the test sequence $\alpha_{n,m,\ell}$ is universal. Hence, the test generation of the augmented PLAs is no more necessary. Moreover, the universal test sequence is a very short test sequence whose length is 2n+3m. In this way, we can see that the augmented PLAs are very easily testable PLAs having a universal test sequence.

Table 1 Universal test set $A_{n,m,\ell}$

	$x_1 \cdots x_i \cdots x_n$	$y_1 y_2$	$S_1 \cdots S_j \cdots S_m$	Z_1	Z_2
I_{11}	- .... - .... -	- -	0 ..... 0 0	0	0
For j=1,2,...,m					
I^0_{2j}	0 ..... 0 0	1 0	0 ..... 0 1 0 0	1	1
I^1_{2j}	1 ..... 1 1	0 1	0 ..... 0 1 0 0	1	1
For i=1,2,...,n					
I^0_{3i}	1 ... 1 0 1..... 1	0 1	1 .....1.....1	$\bar{\varepsilon}_m$	-
I^1_{3i}	0 ... 0 1 0 0	1 0	1 ..... 1 1	$\bar{\varepsilon}_m$	-

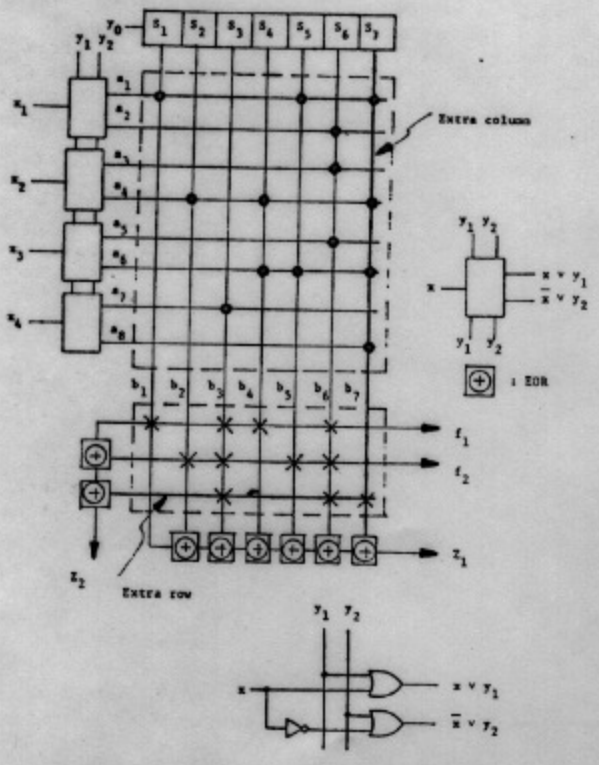

Fig. 5 Augmented PLA with single-bit decoders

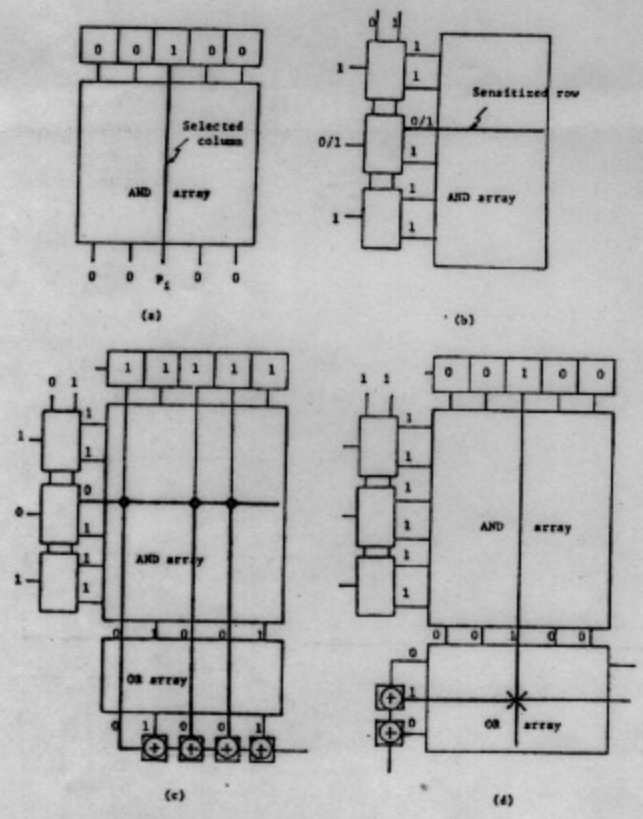

Fig. 6 Features of the augmented PLA

IV. Augmented PLAs with Double-Bit Decoders

The PLAs with double-bit decoders can be similarly augmented by adding extra logic, that is, a shift register, two cascades of EORs, and one column and one row to the AND and OR arrays, respectively, as shown in Fig.7. Fig.7 shows a PLA augmented from the PLA shown in Fig.4. The augmented double-bit decoders have four control inputs y_1, y_2, y_3 and y_4 as shown in Fig. 7.

For the augmented PLA with double-bit decoders, we can similarly construct a universal test set $B_{n,m,\ell}$ as shown in Table 2, and the following theorem holds.

Theorem 3: Let $N_{n,m,\ell}$ be an augmented PLA with double-bit decoders which has n inputs, m columns in the AND array and ℓ rows in the OR array. For any $N_{n,m,\ell}$, the test set $B_{n,m,\ell}$ can detect all single stuck and cross-point faults in the decoders, AND array and OR array.

Theorem 4: $B_{n,m,\ell}$ can detect all multiple stuck faults in the cascade C_1. If the column rank of M_{OR} is ℓ, then all multiple stuck faults in the cascade C_2 can be also detected by $B_{n,m,\ell}$.

Using the test set $B_{n,m,\ell}$, we can construct the universal test sequence $\beta_{n,m,\ell}$ for the augmented PLAs as follows:

$$\begin{aligned}\beta_{n,m,\ell} = {} & I_{11}\ I_{21}^0 I_{22}^0 \cdots I_{2m}^0 I_{21}^1 I_{22}^1 \cdots I_{2m}^1 \\ & I_{21}^2 I_{22}^2 \cdots I_{2m}^2 I_{21}^3 I_{22}^3 \cdots I_{2m}^3 \\ & U_1 U_2 \cdots U_{m-1}\ I_{31}^0 I_{32}^0 \cdots I_{3\frac{n}{2}}^0 \\ & I_{31}^1 I_{32}^1 \cdots I_{3\frac{n}{2}}^1\ I_{31}^2 I_{32}^2 \cdots I_{3\frac{n}{2}}^2 \\ & I_{31}^3 I_{32}^3 \cdots I_{3\frac{n}{2}}^3\end{aligned}$$

where the test pattern U_i (i=1,2,...,m-1) is defined as

$$U_i = \underbrace{-\ \cdots\ -}_{x_1 \cdots x_n}\ \underbrace{1\,1\,1\,1}_{y_1 y_2 y_3 y_4}\ \underbrace{1 \cdots 1\ 0 \cdots 0}_{S_1 \cdots S_i S_{i+1} \cdots S_m}\ \underbrace{\cdot}_{Z_1 Z_2}\ \varepsilon_i$$

The length of the test sequence is 2n+5m.

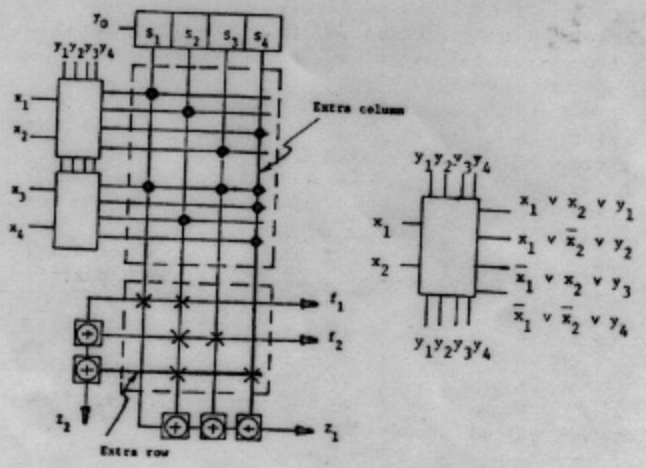

Fig. 7 Augmented PLA with double-bit decoders

V. Multiple Fault Detection

So far we have discussed the single fault detection problem for the augmented PLAs. Similarly, we can extend the single fault model to the types of multiple faults in the following. Note that no more than one of the following multiple faults occurs simultaneously.

1. Multiple stuck faults on the primary inputs x_i (i=1,2,...,n).
2. Multiple stuck faults on the control inputs y_i (i=1,2,3,4).
3. Multiple stuck faults on the rows in the AND array.
4. Multiple stuck faults on the columns in the AND and OR arrays.
5. Multiple stuck faults on the rows in the OR array.
6. Multiple stuck faults on the input and output lines of the EOR cascade C_1.
7. Multiple stuck faults on the input and output lines of the EOR cascade C_2 provided that the column rank of M_{OR} is equal to the number of rows in OR array.
8. Odd number of cross-point faults on the columns of the OR array.
9. Odd number of cross-point faults on the rows of the AND array.

For the class of the above mentioned multiple faults, we can show that the test sets $A_{n,m,\ell}$ and $B_{n,m,\ell}$ are also universal test sets for the augmented PLAs with single-bit decoders and double-bit decoders, respectively.

Now, the cascade of EORs in the PLA is used as a parity checker to detect odd number of errors on the rows and columns of the AND and OR arrays, respectively. In the same way, this approach can be extended to other multiple fault model by applying error detecting codes such as linear codes [7], where the augmented PLAs will be designed to have more than two cascades of EORs.

Table 2 Universal test set $B_{n,m,\ell}$

	$x_1\ x_2 \cdots x_{2i-1} x_{2i} \cdots x_{n-1} x_n\ y_1 y_2 y_3 y_4\ s_1 \cdots s_j \cdots s_m$	$z_1\ z_2$
t_{11}	- - ...- - ... - - - - - - 0 ....0 0	0 0

For j=1,2,...,m

t^0_{2j}	0 0 ... 0 0 .... 0 0 1 0 0 0 0 ... 1 0	1 1
t^1_{2j}	0 1 ... 0 1 .... 0 1 0 1 0 0 0 ... 1 0	1 1
t^2_{2j}	1 0 ... 1 0 .... 1 0 0 0 1 0 0 ... 1 ... 0	1 1
t^3_{2j}	1 1 ... 1 1 .... 1 1 0 0 0 1 0 ... 1 ... 0	1 1

For $i=1,2,\ldots,\frac{n}{2}$

t^0_{3i}	1 1 ... 0 0 ..... 1 1 0 1 1 1 1 ... 1 1	$\bar{c}_m$ -
t^1_{3i}	1 0 ... 0 1 .... 1 0 1 0 1 1 1 ... 1 1	$\bar{c}_m$ -
t^2_{3i}	0 1 .... 1 0 .... 0 1 1 1 0 1 1 ... 1 1	$\bar{c}_m$ -
t^3_{3i}	0 0 .... 1 1 .... 0 0 1 1 1 0 1 ... 1 1	$\bar{c}_m$ -

VI. Fault Location and Repair

In this section, we consider the fault detection and repair of the augmented PLAs. For the augmented PLAs there exists a universal test sequence of fault location. The types of faults considered here are the multiple cross-point faults in the AND and/or OR arrays.

Fault location test can be performed by identifying the configuration of the AND and OR arrays, that is, whether there exists a link between each row i and column j of the arrays. By applying the test pattern shown in Fig.8, we can identify whether there exists a link or contact between row i and column j of the AND array. If the value of output Z_1 is 0 (1), then there exists a link (correspondingly, no link) at the (i,j)-th position of the AND array.

For the OR array, the test pattern shown in Fig.9 can detect the presence or absence of a link between row i and column j of the OR array. If the value of output f_i is 1 (0), then there exists a link (no link) at the (i,j)-th position of the OR array. Note that the last row of the OR array does not have a direct output, however it is observable from the additional output Z_2.

Using these test patterns, we can completely determine the configuration of the AND and OR arrays. Therefore, all multiple cross-point faults can be found by observing the responses. The number of tests for the AND array is 2nm, and the number of tests for the OR array is m. Hence the total length of the fault location test sequence for the augmented PLAs is 2nm+m.

Now, after the fault location test the faulty PLA can be repaired as follows. For a field programmable logic array (FPLA), it is known that an arbitrary product term can be both logically and physically deleted and a new product term can be generated by using spare columns of the PLA, and thus the faulty PLA can be repaired using spare rows and/or columns [9]. If the PLA is a mask programmable logic array (MPLA), it is difficult to repair the PLA for itself. In this case, we can repair the faulty PLA by using the well known memory patch technique. This is a method to recover the fucntion of the faulty MPLA by switching it to a spare FPLA when some errors occur.

VIII. Conclusion

In this paper, we have introduced a design of easily testable PLAs by adding extra logic, and presented universal test sequences for them. These augmented PLAs have the very short universal test sequences such that the test patterns and responses are uniquely determined only by the size of the PLAs independently of the function of them. The length of the universal test sequences to detect single and multiple faults is of order n+m, and the length of the universal test sequences to locate multiple faults is of order nm,

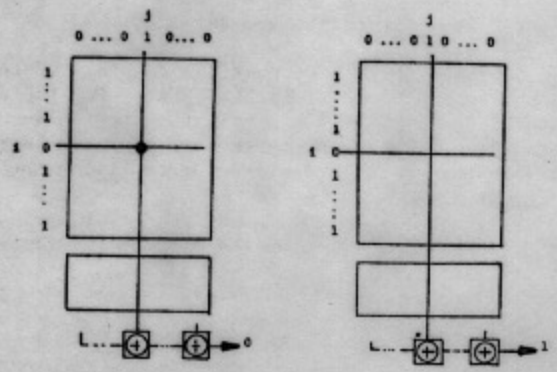

Fig. 8 Fault location test for AND array

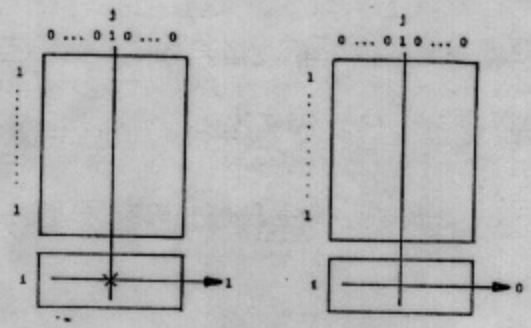

Fig. 9 Fault location test for OR array

where n is the number of inputs and m is the number of product terms in the PLAs.

Although we have not considered PLAs with flip-flops in this paper, we can augment them to have the universal test sets. This can be done by applying scan-in and scan-out technique [8].

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References

[1] R.G.Bennetts and R.V.Scott,"Recent developments in the theory and practice of testable logic design," IEEE Computer, pp.47-63, June 1976.

[2] S.M.Reddy,"Easily testable realizations for logic functions," IEEE Trans. Comput., C-21, pp.1183-1188, Nov. 1974.

[3] S.J.Hong and D.L.Ostapko, "Logic array with testing circuitry," United States Patent, 3958110, May 1976.

[4] H.Fleisher and L.I.Maissel, "An introduction to array logic," IBM Journal of Research and Development, Vol.19,No.2,pp.98-109,March 1975.

[5] D.L.Ostapko and S.J.Hong, "Fault analysis and test generation for programmable logic arrays (PLAs)," Proc. FTCS-8,France, pp.83-89,June 1978.

[6] V.K.Agarwal, "Multiple fault detection in programmable logic arrays," Proc. FTCS-9,pp. 227-234, June 1979.

[7] W.W.Peterson and E.J.Weldon, Jr., "Error-Correcting Codes," MIT Press, 1972.

[8] M.J.Williams and J.B.Angell, "Enhancing testability of large-scale integrated circuits via test points and additional logic," IEEE Trans. Comput.,C-22,pp.46-60, Jan. 1973.

[9] "Signetics Field Programmable Logic Arrays," Signetics, California, Oct. 1977.

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