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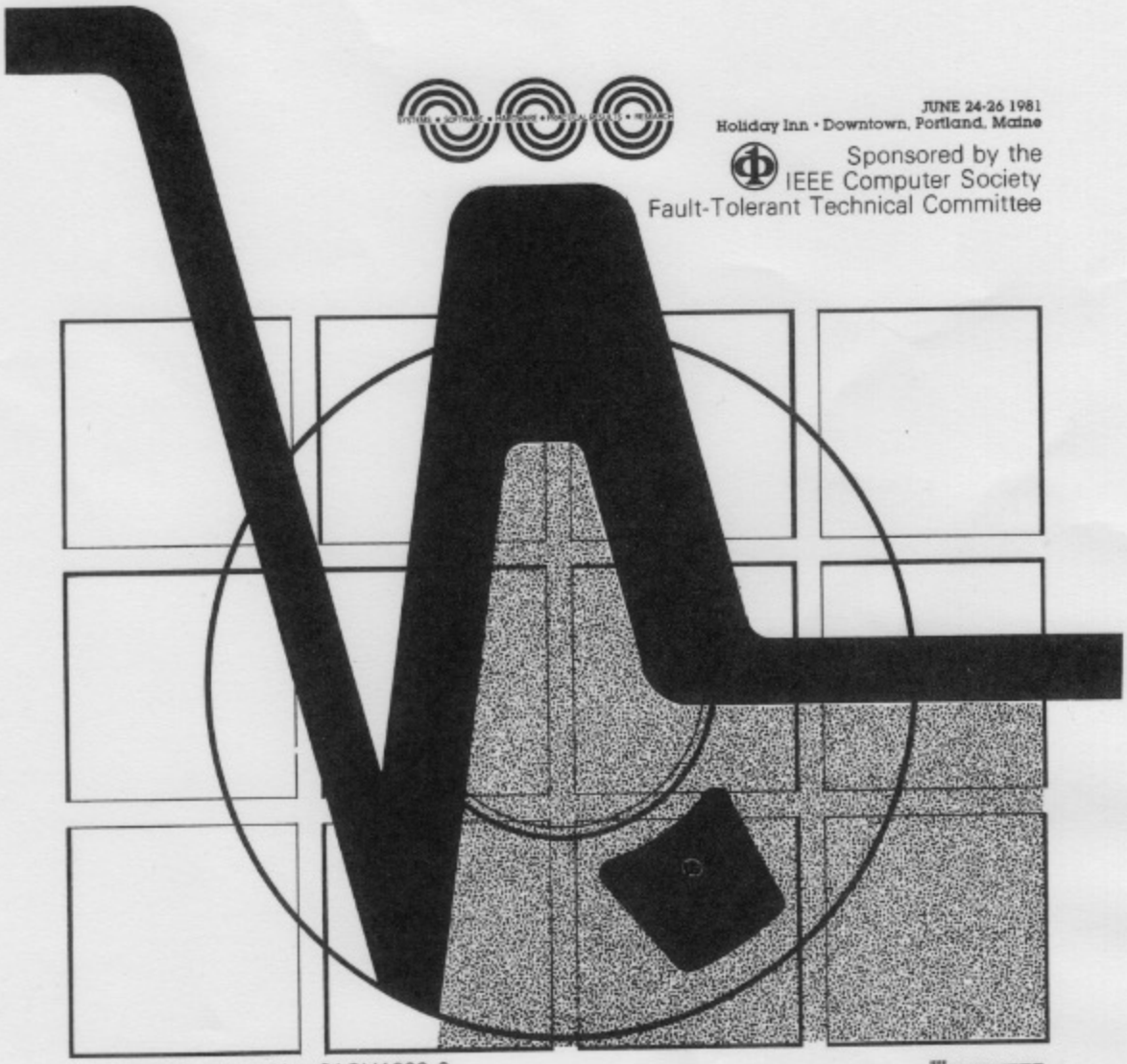

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A MULTIPLE FAULT TESTABLE DESIGN OF PROGRAMMABLE LOGIC ARRAYS

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ABSTRACT

In this paper, the problem of fault detection for multiple faults in easily testable Programmable Logic Arrays (PLAs) is discussed. The easily testable PLAs will be designed by adding extra logic. The augmented PLAs have the following properties: (1) for a PLA with n inputs and m product terms, there exists a test such that the test patterns do not depend on the function, but depend on n and m, though responses depend on the function ; (2) the number of test to detect multiple stuck and cross-point faults is $m(2n+1)+4n+5$; (3) the number of additional pins for the augmentation is 3.

1. INTRODUCTION

With the advent of VLSI, the circuit complexity of chips has been increasing exponentially. A considerable effort is being devoted to diagnosable designs. In addition to the use of extra inputs/outputs and additional logic it has been observed that regular structures help to reduce the complexity of the tests. Programmable Logic Arrays (PLAs) being one such regular structure have been studied in some detail for design and test generation [1-4].

Recently, Hong and Ostapko [5] and Fujiwara et al [6] have independently proposed designs of PLAs which can be tested easily by function independent test set. However, from application point of view these PLAs have the following limitations: (a) In general only single faults are detected, though most of the multiple faults are also detected. (b) Use of Exclusive-OR (EOR) cascades [6] introduces a large combinational delay in the test mode. (c) In [5] EOR cascade has been replaced by EOR tree to reduce the delay. However, it is well known that multiple fault detection properties of EOR cascades are superior than that of EOR trees [7,8].

One may advance the argument that in view of the fact methods to derive multiple fault detection test sets are known [2,4] and furthermore Agarwal [3] has shown that single fault detecting tests for PLAs also cover a large percentage of multiple faults of multiplicity of seven or less. However, it is important to detect all multiple faults, because (a) at fabrication level (or when first in use) a PLA must be tested for multiple faults and (b) introduction of additional logic increases the the possibility of multiple faults.

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2. MODIFICATION TO EXISTING DESIGNS

We shall describe our results using decoder-AND-OR array as shown in Figure 1. The Decoder D_1 shown in Figure 1 is a 1 bit decoder. Our results also apply to PLAs which use two or more bits decoders. A PLA consits of n inputs, m columns and ℓ outputs.

We shall call the PLA of [5] as HO-PLA and that of [6] as FKO-PLA. In HO-PLA the inputs required to the control decoder are $\lceil \log_2(x+1) \rceil$, where $x = n/i$, for i-bit decoders (normally i is small [1]). Introducing a shift register(SR) to decoder inputs we can reduce the number of additional inputs to the control decoder from $\lceil \log_2(x+1) \rceil$ to one. Similarly in FKO-PLA, the number of control inputs can be reduced by adding an SR. It appears from the above analysis the use of SR can be a very useful tool in testable design [9], also a realization of a shift register cell is very simple [10].

In the above two designs an additional column has been appended to the AND array for each of the decoder lines [5,6]. Thus these lines can be checked for parity violation, therefore any odd number of errors in a row or column can be detected. One could easily extend this concept and make use of error correcting codes [11]. A useful code can be Hamming code with an overall parity check. This will cause a detection up to three errors. Similar checks on the OR arrays can be used. It is interesting to note that for such cases the use of EOR cascade will be superior than the use of EOR tree as EOR cascades can be tested for arbitrary multiple faults with little or no additional effort [8].

3. NEW DESIGN

In this section we propose a new design of PLA which can be tested for any number of multiple faults. The fault model assumed is stuck faults and/or cross-point faults. Before proposing the final design we shall study a PLA like structure for its fault detection properties.

Consider a PLA like structure $M_{n,m}$, shown in Figure 2. It has 2n inputs to AND array, an SR and two outputs. Total number of columns in the AND array are m. The SR can be used to select an arbitrary column of AND array of $M_{n,m}$ by setting 1 to the selected column and 0's to all other columns.

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Let us define a set $A_{n,m,j}$ consisting of (2n+1) vectors in which each vector is a (2n+m)-tuple as shown in Table 1. We define a test set $A_{n,m}$ as follows:

$$A_{n,m} = \{ A_{n,m,j} \mid j=1,2,\ldots,m \}$$

We shall now show that the test set $A_{n,m}$ detects any number of stuck and cross-point faults in the PLA like structure, $M_{n,m}$.

LEMMA 1: Let $M_{n,m}$ be a PLA like structure with 2n inputs and m columns in the AND array. For any $M_{n,m}$ the test set $A_{n,m}$ can detect any number of stuck and cross-point faults in the AND array, provided no column is covered by all other columns.

Proof: Clearly any stuck type faults at the horizontal lines will be detected by the test set $A_{n,m}$ at the Z_1 output. Furthermore, the test set $A_{n,m,j}$ uniquely identifies all the cross point connections in the j-th column and also detects any stuck type faults in that column. Thus any number of stuck and cross-point faults will be detected at Z_2 output. Q.E.D.

In the above lemma we assumed SR to be fault free. However, SR can easily be tested while applying test $A_{n,m}$ by observing the SR output at S_m. We now consider the fault detection test set for the D_n circuit of Figure 3.

LEMMA 2: The D_n circuit of Figure 3 can be tested for all multiple stuck type faults by the test set T given in Table 2.

We are now ready to present our final design of a PLA. In this paper we will only study the case of PLAs with single-bit decoders, however the result can be easily extended to two-bit and three-bit decoders by modifying lemma 2. We augment a single bit decoder PLA by adding extra logic as follows (see Figure 4).

The following theorem gives a multiple fault detection test set for the augmented PLA.

THEOREM 1: The augmented PLA of Figure 4 can be tested for all multiple faults (stuck or cross-point type) by a test set of length m(2n+1)+4n+5.

Proof: We first set S-register to 0 and apply 4n+4 tests given in lemma 2 and observe Z_1 output. This way we will detect any faults in the horizontal lines and/or in the additional logic introduced in the docoder part of the array. We then set C=0, S_j=1 and all the remaining S_i's as zeros, and apply 2n+1 tests from V-register (given in lemma 1 as a_i inputs). Thus any faults in the AND array will be detected at Z_2 output. It only remains to be shown that the faults in the OR array will also be detected. Since only one column corresponding to S_j will be activated in the test of Table 1, by observserving $f_1, f_2, \ldots, f_\ell, z_2$ outputs any detectable faults will be detected at the f_i outputs.

We finally set S-register to all 0's and V-register to all 1's and observe output z_2.

Q.E.D.

Note that there are undetectable faults in arrays. An undetectable fault in an OR array can best be explained by the following example shown in Figure 5 (only the portion of interest has been shown). In this array following faults are undetectable; (a) stuck at 0 fault at α, (b) stuck at 0 fault at δ, (c) presence of a corss-point fault at β, and stuck at fault at γ.

None of these faults change the function f_1 and f_2. However, it is interesting to note that if in (c) only cross-point fault at β is present and γ is not stuck at 0, then this fault will be detected even though this fault does not change the functions

4. CONCLUSIONS

In this paper we have presented a new design of PLAs which can be tested for multiple faults by a test sequence of length m(2n+1)+4n+5. Furthermore, the test set is independent of the functions being realized by a PLA.

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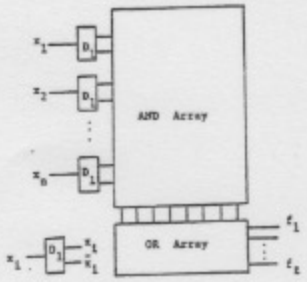

Fig. 1: A PLA structure

Table 1: The test set $A_{n,m,j}$

	s_1 s_2 ... s_{2n-1} s_{2n} s_1 s_2 ... s_j ... s_m
I_j	1 1 ... 1 1 0 0 ... 1 ... 0
$a_{1,j}$	0 1 ... 1 1 0 0 ... 1 ... 0
$a_{2,j}$	1 0 ... 1 1 0 0 ... 1 ... 0
	. . .
$a_{2n-1,j}$	1 1 ... 0 1 0 0 ... 1 ... 0
$a_{2n,j}$	1 1 ... 1 0 0 0 ... 1 ... 0

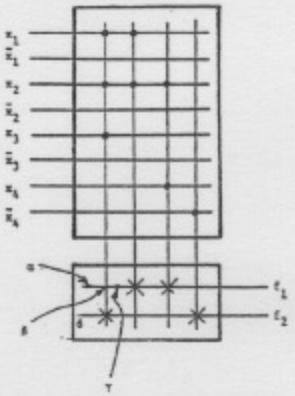

Fig. 5: Undetectable faults

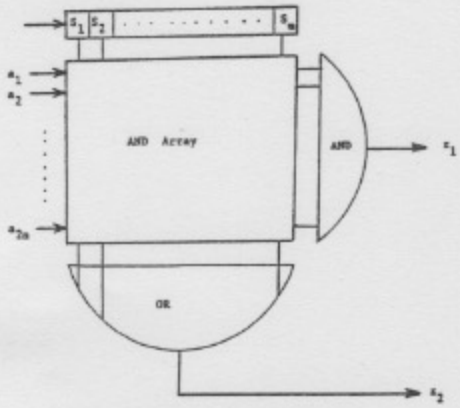

Fig. 2: A PLA like structure

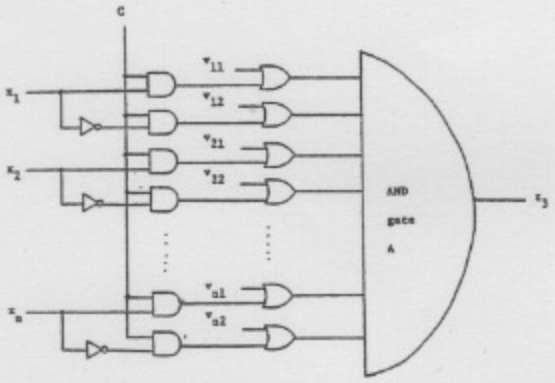

Fig. 3: A D_n circuit

Table 2: Test set T

	x_1 x_2 ... x_n	C	v_{11} v_{12} v_{21} v_{22} ... v_{n1} v_{n2}
$0_{0,1}$	0 0 ... 0	0	1 1 1 1 ... 1 1
$1_{0,1}$	1 1 ... 1	0	1 1 1 1 ... 1 1
$1_{0,a_1}$	1 1 ... 1	0	0 1 1 1 ... 1 1
$0_{0,a_2}$	0 0 ... 0	0	1 0 1 1 ... 1 1
$1_{0,a_3}$	1 1 ... 1	0	1 1 0 1 ... 1 1
⋮	⋮	⋮	⋮
$1_{0,a_{2n-1}}$	1 1 ... 1	0	1 1 1 1 ... 0 1
$0_{0,a_{2n}}$	0 0 ... 0	0	1 1 1 1 ... 1 0
$0_{1,a_1}$	0 0 ... 0	1	0 1 1 1 ... 1 1
$1_{1,a_2}$	1 1 ... 1	1	1 0 1 1 ... 1 1
⋮	⋮	⋮	⋮
$0_{1,a_{2n-1}}$	0 0 ... 0	1	1 1 1 1 ... 0 1
$1_{1,a_{2n}}$	1 1 ... 1	1	1 1 1 1 ... 1 0
$0_{1,\alpha}$	0 0 ... 0	1	1 0 1 0 ... 1 0
$1_{1,\bar{\alpha}}$	1 1 ... 1	1	1 0 1 0 ... 0 1

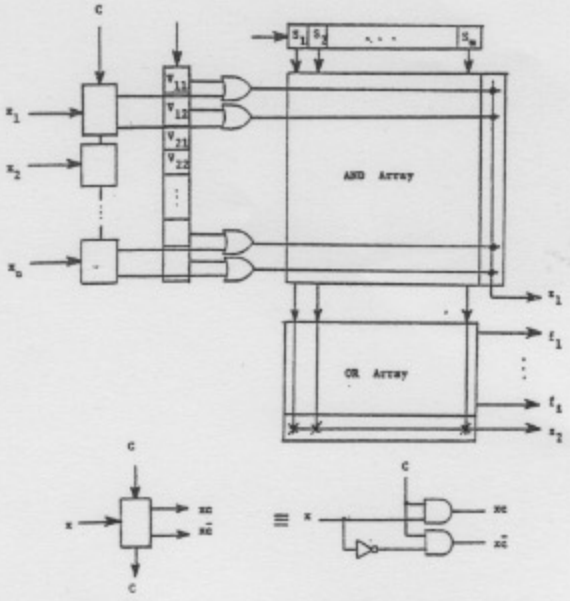

Fig. 4: Augmented PLA with single-bit decoders