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Test Generation for Acyclic Sequential Circuits with Hold Registers

1 Introduction

Test generation for sequential circuits is generally considered to be a hard problem. For such sequential circuits, *design for testability (DFT)* is an important approach to reducing the test generation cost [1, 2]. On the other hand, for combinational circuits, efficient test generation algorithms were proposed, and hence we can obtain a *complete (100% fault efficiency)* test set even if the circuit size is large. Therefore, it is significant to apply DFT to a sequential circuit so that the resultant circuit can be test-generated using only a combinational test generator.

Full scan design referring to chaining all of memory elements or flip-flops (FFs) into a shift register is such a traditional DFT technique. In the full scan design, the portion of the circuit excluding the scan path, which is called the *kernel*, is a combinational circuit, and consequently a combinational test generator can be used. However, the full scan design requires large overhead. Although *partial scan design* which makes a subset of FFs scannable can avoid such a penalty, the kernel circuit is still sequential one [3, 4], and hence it requires the use of sequential test generators in general.

In order to obtain *complete test sequences* for sequential circuits efficiently with low hardware overhead, several classes of sequential circuits for which test generation can be performed by using only a combinational test generator were identified [5]–[11]. In [11], we presented a method of test generation for acyclic sequential circuits using a *time-expansion model (TEM)*. One can obtain a *complete* test set for a given acyclic sequential circuit by applying combinational test generation to the TEM of the given circuit, provided that the combinational test generator can deal with multiple faults. Thus, for any sequential circuit, by selecting a sufficient set of scan FFs so that the resultant kernel is acyclic, a *complete test sequence* for the sequential circuit can be generated by using a combinational test generator in spite of partial scan. In [11], however, a *hold register* which is a collection of FFs with *hold mode* is regarded as a self-loop, and consequently it is always chosen as a scan register.

In this paper, we propose a *new* TEM (time-expansion model) for acyclic sequential circuits with *hold* registers. Even if an acyclic sequential circuit has hold registers, test generation for the circuit can be performed by applying combinational test generation to the new TEM. Hence, hold registers are not necessarily chosen as scan registers, and consequently the hardware overhead is smaller compared with that of the partial scan design in which kernels have no hold register [11].

For an acyclic sequential circuit, a TEM is obtained from a sequence of load/hold controls. Since there exist many sequences of load/hold controls, many TEMs are obtained from an acyclic sequential circuit. Hence, in order to obtain a complete test sequence for an acyclic sequential circuit, we may have to perform test generation for *all* TEMs of the circuit. However, that may not be acceptable. Therefore, in order to reduce the number of TEMs required for the test generation, we introduce a *cover relation* among TEMs for an acyclic sequential circuit, and show that test generation for all *maximal* (on the relation) TEMs is necessary and sufficient to obtain a *complete* test sequence. Furthermore, we present a class of acyclic sequential circuits for which the number of maximal TEMs is just one, i.e., the *maximum* TEM exists. For a circuit in the class, a test sequence for any testable fault can be generated by using only the maximum TEM of the circuit, and therefore a complete test sequence for the circuit can be obtained efficiently.

In the following discussion, all the proofs of propositions will be omitted due to limitations of space. The proofs can be displayed in the same way as [11].

2 Time-Expansion Model for Acyclic Sequential Circuits

In this section, we present a *time-expansion model (TEM)* for an acyclic sequential circuit, and show that test generation for an acyclic sequential circuit with hold registers can be performed by applying combinational test generation to its TEMs.

2.1 Circuit Model

In this paper, we consider synchronous sequential circuits. A sequential circuit consists of combinational logic blocks connected with each other directly or through registers. A register is a collection of D-type flip-flops (FFs) driven by the same clock signal. The clock signals of all registers are assumed to be directly controlled by primary inputs, and no clock signal feeds data input of either a combinational logic block or a register.

A combinational logic block (or logic block, for short) in a sequential circuit is a region of connected combinational logic, excluding registers. A logic block may include primary inputs and primary outputs.

Some registers may have a load enable control signals. A register with an explicit load enable control signal is called *H-register*. An H-register has two modes of operation: HOLD mode (in which it retains its value across consecutive clock cycles) and LOAD mode (in which it reads from the data input when a clock signal is applied). A register without a load enable control signal is called *L-register*, which always operates in the load mode during every clock cycle. The control signal for each H-register is assumed to be directly controlled by a primary input independent of that for the others.

An input-pattern for a sequential circuit consists of a data input-pattern and a control input-pattern, which are a collection of signals applied to combinational logics and that of signals applied to H-registers, respectively.

Under this constraint, the topology of a sequential circuit can be modeled by a *topology graph* defined as follows.

Definition 1 (Topology graph): A topology graph is a directed graph $G = (V, A, r)$, where a vertex $v \in V$ denotes a logic block and an arc $(u, v) \in A$ denotes a connection from u to v and each arc has a label $r : A \rightarrow Z^+$ (non-negative integers) $\cup \{h\}$. When two logic blocks u, v are connected directly or through one or more L-registers, the label $r(u, v)$ denotes the number of L-registers (i.e., $r(u, v) \in Z^+$). When two logic blocks u, v are connected through

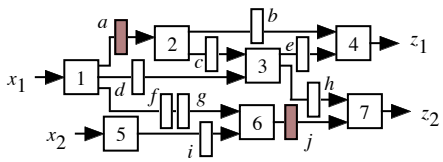


Figure 1. Acyclic sequential circuit S.

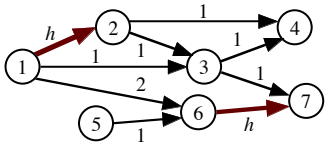


Figure 2. Topology graph of S: G.

one H-register [1], the label $r(u,v) = h$. □

Example 1: Consider a sequential circuit S illustrated in Fig. 1. In this figure, $1,2,\ldots,7$ are logic blocks, $b,c,\ldots,i$ are L-registers, and a and j, which are highlighted, are H-registers. The topology graph G of this circuit S is shown in Fig. 2. □

2.2 Time-Expansion Model (TEM)

A *time-expansion model* for an acyclic sequential circuit is defined based on the following *time-expansion graph*.

Definition 2 (Time-expansion graph (TEG)): Let S be an acyclic sequential circuit and let $G = (V,A,r)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$ be a directed graph, where V_E is a set of vertices, A_E is a set of arcs, t is a mapping from V_E to a set of integers, and l is a mapping from V_E to the set of vertices V in G. If graph E satisfies the following five conditions, graph E is said to be a *time-expansion graph (TEG)* of G.

C1(Logic preservation) The mapping l is a surjective, i.e.,
$$\forall v \in V, \exists u \in V_E \text{ s.t. } v = l(u).$$

C2(Input preservation) Let u be a vertex in E. For any direct predecessor v ($\in pre(l(u))$) of u in G, there exists a vertex u' in E such that $l(u') = v$ and $u' \in pre(u)$. Here, $pre(v)$ denotes the set of direct predecessors of v.

C3(Time consistency) For any arc (u,v) ($\in A_E$), there exists an arc $(l(u),l(v))$ such that $r(l(u),l(v)) = t(v) - t(u)$ or $r(l(u),l(v)) = h$.

C4(Time uniqueness) For any vertices u,v ($\in V_E$), if $t(u) = t(v)$ and if $l(u) = l(v)$, then the vertices u and v are identical, i.e., $u = v$.

C5(Hold consistency) For any pair of arcs (u_1,v_1), (u_2,v_2) ($\in A_E$) such that $(l(u_1),l(v_1)) = (l(u_2),l(v_2))$ and $r(l(u_1),l(v_1)) = r(l(u_2),l(v_2)) = h$, if $t(u_1) > t(u_2)$, then $t(u_1) \geq t(v_2)$.

□

This definition is written by adding the last condition C5 to that of the time-expansion graph for an acyclic sequential circuits *without* H-registers [11]. The condition C5 denotes that an H-register cannot read a new value while retaining a previous one.

[1]Even if there exist two H-registers or both of L and H-registers between two logic blocks, the topology graph can also represent such sequential circuits by supposing existence of a combinational logic block consisting only of lines or buffers between the two logic blocks.

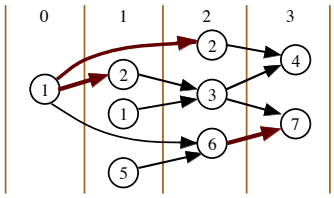


Figure 3. TEG of G: E_1.

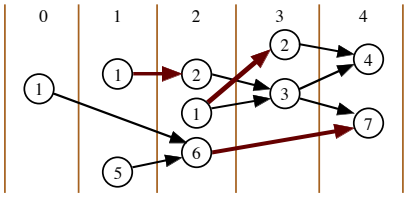


Figure 4. TEG of G: E_2.

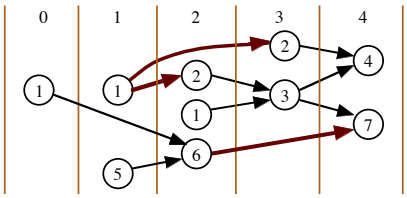


Figure 5. TEG of G: E_3.

Example 2: Figs. 3, 4 and 5 show TEGs of topology graph G. In these figures, the number denoted in a vertex u is the label $l(u)$, and the number located at the top of each column denotes the value of the labels $t(u)$ of the vertices u in the column. □

As shown in the above example, there exist different TEGs for a topology graph according to control input sequences.

Definition 3 (Time-expansion model (TEM)): Let S be an acyclic sequential circuit, let $G = (V,A,r)$ be the topology graph of S, and let $E = (V_E,A_E,t,l)$ be a TEG of G. The combinational circuit $C_E(S)$ obtained by the following procedure is said to be the *time-expansion model (TEM)* of S based on E.

(1) For each vertex $u \in V_E$, let logic block $l(u)$ ($\in V$) be the logic block corresponding to u.

(2) For each arc $(u,v) \in A_E$, connect the output of u to the input of v with a bus in the same way as $(l(u),l(v))$ ($\in A$). Note that the connection corresponding to (u,v) has no register even if the connection corresponding to $(l(u),l(v))$ has a register (i.e., $r(l(u),l(v)) \neq 0$).

(3) In each logic block, lines and logics that are reachable to neither other logic blocks nor primary outputs are removed.

□

Example 3: Fig. 6 shows the TEM of sequential circuit S (Fig. 1) based on TEG E_1 (Fig. 3). In this figure, a highlighted part in a logic block represents a portion of the lines and gates removed by Step (3) in Def. 3. □

2.3 Test Generation with TEM

Here we consider the relationship between input/output sequences of an acyclic sequential circuit and input/output patterns of its TEM. Let S be an acyclic sequential circuit, and let $G = (V,A,r)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$

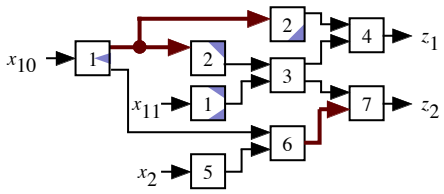


Figure 6. TEM of S based on E_1: $C_{E_1}(S)$.

Table 1. Input and output sequences for S obtained by transformation procedure τ_S.

Time		0	1	2	3
Data Input	x_1	I_{10}	I_{11}	X	X
	x_2	X	I_2	X	X
Control Input	Reg. a	L	H	X	X
	Reg. j	X	X	L	X
Output	z_1	X	X	X	O_1
	z_2	X	X	X	O_2

be a TEG of G, let $C_E(S)$ be the TEM of S based on E, and let $t_{\min}$ be the minimum of labels t in $C_E(S)$. An input pattern for $C_E(S)$ can be transformed into an input sequence for circuit S by the following procedure τ_S.

Definition 4 (Transformation procedure τ_S):

(1) Control input sequence I_H. Let $I_H(v',v,t)$ denote an input value which is applied to an H-register (v',v) $(\in A)$ at time t. For each arc $(u',u) \in A_E$ such that $r(l(u'),l(u)) = h$, let

$$I_H(l(u'),l(u),t-t_{\min}) = \begin{cases} L \text{ (LOAD mode)} & (t = t(u')) \\ H \text{ (HOLD mode)} & (t(u')+1 \le t \le t(u)-1) \end{cases}$$

Let the values $I_H(v',v,t)$ which are not defined by the above equation be X (don't care).

(2) Data input sequence I_S. For each logic block $u \in V_E$ in $C_E(S)$, let

$$I_S(l(u),t(u)-t_{\min}) = I_C(u),$$

where $I_S(v,t)$ denotes an input-pattern applied to logic block v in S at time t, and $I_C(u)$ denotes an input-pattern applied to logic block u in $C_E(S)$.

□

Note that in the above procedure, a control input sequence is obtained only from a TEG E independent of an input-pattern for TEM $C_E(S)$.

Lemma 1: Let I_C be an arbitrary input-pattern for TEM $C_E(S)$, and let I_S and I_H be a data input sequence and a control input sequence obtained by τ_S, respectively. The output pattern $O_C(u)$ obtained from a logic block $u \in V_E$ by applying input pattern I_C to $C_E(S)$ is equal to the output pattern $O_S(l(u),t(u)-t_{\min})$ obtained from the corresponding logic block $l(u)$ at time $t(u)-t_{\min}$ by applying data input sequence I_S with control input sequence I_H. □

Example 4: Consider a TEM $C_{E_1}(S)$ (Fig. 6) of a sequential circuit S shown in Fig. 1. Suppose an input-pattern $I_C = (x_{10},x_{11},x_2) = (I_{10},I_{11},I_2)$ applied to $C_{E_1}(S)$ and the corresponding output-pattern is $O_C = (z_1,z_2) = (O_1,O_2)$. According to the labels t in TEG E_1 (Fig. 3), the patterns I_C and O_C are transformed into the sequences shown in Table 1 by procedure τ_S. Here, X denotes a don't-care value. □

Note that the length of the sequence obtained from a pattern for TEM $C_E(S)$ by procedure τ_S becomes $\max_{u\in V_E}\{t(u)\} - \min_{u\in V_E}\{t(u)\}+1$.

Let I_S and I_H be a data input sequence and a control input sequence for acyclic sequential circuit S such that the sequences determine the output pattern $O_S(v,t)$ of a logic block v $(\in V)$ in S at time t, respectively. Here, a pattern that does not affect $O_S(v,t)$ in the input sequences I_S and I_H is considered as don't-care. Input sequences I_S and I_H for S can be transformed into a TEG E and an input-pattern I_C for the TEM $C_E(S)$ by the following procedure τ_C.

Definition 5 (Transformation procedure τ_C):

(1) TEG E. Construct a TEG $E = (V_E,A_E,t,l)$ in which there exists a vertex $u \in V_E$ that satisfies the following conditions.
(1) $l(u) = v \wedge t(u) = t$, and
(2) For the control input value $I_H(v_1,v_2,t')$ applied to an H-register (v_1,v_2) $(r(v_1,v_2) = h)$ at time t',
if $I_H(v_1,v_2,t') = L$, then there exists a vertex $u_1 \in Pre(u)$ such that $l(u_1) = v_1 \wedge t(u_1) = t'$,
if $I_H(v_1,v_2,t') = H$, then there exists an arc (u_1,u_2) $(\in A_E)$ such that $u_1,u_2 \in Pre(u) \wedge t(u_1) < t' \wedge t(u_2) > t'$. Here, $Pre(u)$ denotes the set of all predecessors of u.

(2) Input-pattern I_C. For every input pattern $I_S(v',t')$ applied to each logic block v' at time t', if $I_S(v',t')$ affects output $O_S(v,t)$, then for the logic block u' that satisfies $u' \in l^{-1}(v')$ and $t(u') = t'$, let $I_C(u') = I_S(v',t')$.

□

Lemma 2: Let v $(\in V)$ be an arbitrary logic block in acyclic sequential circuit S, and let I_S and I_H be a data input sequence and a control input sequence that are required to set the output of v to a pattern $O_S(v,t)$ at time t, respectively. Let E and I_C be a TEM and an input-pattern obtained from I_S and I_H by procedure τ_C, respectively. Let u $(\in V_E)$ be the logic block that corresponds to v by the first step (1) in procedure τ_C. The output pattern $O_C(u)$ obtained from the logic block u by applying the input pattern I_C to TEM $C_E(S)$ is equal to the output pattern $O_S(v,t)$. □

Note that as shown in the above procedure τ_C, a TEG (or TEM) is obtained from a control input sequence applied to H-registers in a sequential circuit, independent of data input sequences.

Next, let us consider the relationship between faults in an acyclic sequential circuit and those in its TEMs. Here we consider single stuck-at faults only in logic blocks as those in an original sequential circuit. The stuck-at faults on lines between logic blocks and in registers can be considered to be equivalent to those on input/output lines of logic blocks.

Definition 6 (Fault in TEM): Let S be an acyclic sequential circuit. Let $G = (V,A,r)$ be the topology graph of S, let $E = (V_E,A_E,t,l)$ be a TEG of G, and let $C_E(S)$ be the TEM of S based on E. Let F be the set of faults in S, and let F_E be the set of faults in $C_E(S)$. Suppose a fault $f \in F$ in a logic block u in circuit S. Let $f_e \in F_E$ be the fault corresponding to fault f. Fault f_e is a multiple fault that consists of all the faults existing on the same line in ev-

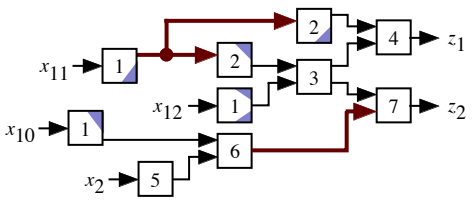


Figure 7. TEM of S based on E_3: $C_{E_3}(S)$.

ery logic block $u \in l^{-1}(v)$. That is, if the number of logic blocks u such that $l(u) = v$ is just one, then the fault f_e is a single fault, otherwise, f_e is a multiple fault. □

From the above discussion, we have the following theorem.

Theorem 1: Let S be an acyclic sequential circuit, and let F be the set of faults in S. Let $G = (V, A, r)$ be the topology graph of S.

(1) A fault $f \in F$ is testable (or irredundant) in S if and only if there exists a TEG E of G such that the fault f_e $(\in F_E)$ corresponding to f is testable in the TEM $C_E(S)$ based on E.

(2) A test pattern for a fault f_e $(\in F_E)$ obtained using a TEM $C_E(S)$ can be transformed into a test sequence for the fault f $(\in F)$ corresponding to fault f_e.

□

From this theorem, we can see that test generation for an acyclic sequential circuit can be performed by using several different TEMs. Furthermore, since TEMs are fully combinational, a combinational test generator can be used for the test generation provided that the test generator can deal with multiple faults.

3 Cover Relation

From Theorem 1, we can have the following corollary.

Corollary 1: Let S be an acyclic sequential circuit. Let F be a set of faults in S. A fault $f \in F$ is untestable (or redundant) in S if and only if the fault corresponding to f_e is untestable in every TEM for S. □

This corollary may imply that if a fault is untestable in an acyclic sequential circuit, in order to identify it, we must apply test generation to *all* the TEMs of the circuit, and identify the corresponding fault as untestable in every TEMs. However, as mentioned in the following discussion, all TEMs are not necessary for each identifying untestable fault.

Let us consider two TEMs $C_{E_1}(S)$ (Fig. 6) and $C_{E_3}(S)$ (Fig. 7) for sequential circuit S (Fig. 1). Suppose, in $C_{E_1}(S)$, an output-pattern O_2 obtained from primary output z_2 by applying an input-pattern (I_a, I_b, I_c) to primary inputs (x_{10}, x_{11}, x_2). This input/output relationship can be simulated by another TEM $C_{E_3}(S)$ (Fig. 7) with four primary inputs x_{10}, x_{11}, x_{12} and x_2: by applying an input-pattern (I_a, I_a, I_b, I_c) to $(x_{10}, x_{11}, x_{12}, x_2)$, the same output-pattern O_2 is obtained from z_2 in $C_{E_3}(S)$. For such a relationship between two TEMs, we say $C_{E_3}(S)$ *covers* $C_{E_1}(S)$, and define it as follows.

Definition 7 (Cover relation): Let S be an acyclic sequential circuit. Let $G = (V, A, r)$ be the topology graph of S, and let $E_1 = (V_1, A_1, t_1, l_1)$ and $E_2 = (V_2, A_2, t_2, l_2)$ be arbitrary TEGs of G. TEG E_1 is said to *cover* TEG E_2 if, for any vertex $v_2 \in V_2$, there exists a vertex $v_1 \in V_1$ which satisfies the following two conditions, and it is denoted by $E_1 \succeq E_2$.

(1) $l(v_1) = l(v_2)$, and

(2) for any pair of $u_1 \in Pre(v_1)$ and $u_2 \in Pre(v_2)$, if $l_1(u_1) = l_2(u_2)$ and $L_{E_1}(u_1, v_1) \cap L_{E_2}(u_2, v_2) \neq \phi$, then $L_{E_1}(u_1, v_1) \subseteq L_{E_2}(u_2, v_2)$.

Here $Pre(v)$ denotes the set of all predecessors of v and $L_E(u, v)$ denotes the set of paths $(l(u), ..., l(v))$ (in G) corresponding to paths $(u, ..., v)$ whose tail and head are u and v in E, respectively. □

Example 5: Consider TEGs E_1 (Fig. 3) and E_3 (Fig. 5). Here, let a_b denote a vertex v such that $l(v) = a$ and $t(v) = b$. Suppose a pair of vertices 1_0 and 7_3 in TEG E_1. There are two paths between 1_0 and 7_3: $L_{E_1}(1_0, 7_3) = \{(1,2,3,7), (1,6,7)\}$. In the other TEG E_3, vertex 7_4 corresponds to vertex 7_3 in E_1 uniquely, and there are two vertices u_3 that satisfy $l_{E_3}(u_3) = l_{E_1}(1_0)$ and $L_{E_3}(u_3, 7_4) \cap L_{E_1}(1_0, 7_3) \neq \phi$: vertices 1_0 and 1_1. $L_{E_3}(1_0, 7_4) = \{1,6,7\} \subseteq L_{E_1}(1_0, 7_3)$ and $L_{E_3}(1_1, 7_4) = \{1,2,3,7\} \subseteq L_{E_1}(1_0, 7_3)$. By checking such a relationship as mentioned above, we can see that E_3 covers E_1. Note that E_1 does not cover E_3. □

When a TEG E_1 covers a TEG E_2, we denote that $E_1 \succeq E_2$. Further, it is also said that TEM $C_{E_1}(S)$ covers TEM $C_{E_2}(S)$ $(C_{E_1}(S) \succeq C_{E_2}(S))$.

Let I_{E_2} be an input-pattern for TEM $C_{E_2}(S)$ (covered by TEM $C_{E_1}(S)$) such that the pattern determines the output-pattern $O_{E_2}(v_2)$ of a logic block v_2 $(\in V_2)$. Based on Def. 7, input-pattern I_{E_2} can be transformed into an input-pattern I_{E_1} for TEM $C_{E_1}(S)$ $(\succeq C_{E_2}(S))$ by the following procedure τ_R.

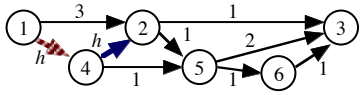
Definition 8 (Transformation procedure τ_R): Let v_1 $(\in V_1)$ be a logic block corresponding to v_2 that satisfies the conditions in Def. 7. Let $I_{E_2}(u_2)$ denote an input-pattern applied to a logic block u_2 $(\in Pre(v_2) \cup \{v_2\})$. For every logic block u_1 $(\in Pre(v_1) \cup \{v_1\})$ corresponding to u_2 $(l_1(u_1) = l_2(u_2)$ and $L_{E_1}(u_1, v_1) \cap L_{E_2}(u_2, v_2) \neq \phi)$, let $I_{E_1}(u_1) = I_{E_2}(u_2)$. Note that the number of logic blocks u_1 corresponding to one logic block u_2 is one or more. □

Lemma 3: Suppose two TEMs C_1 and C_2 of an acyclic sequential circuit such that $C_1 \succeq C_2$. Let v_2 be an arbitrary logic block in C_2. Let I_2 be an input-pattern required to set the output of v_2 to a pattern O_2. Let I_1 be an input-pattern obtained by procedure τ_R from I_2. The output-pattern O_1 obtained from v_1 corresponding to v_2 by applying the input-pattern I_1 to C_1 is equal to the output-pattern O_2. □

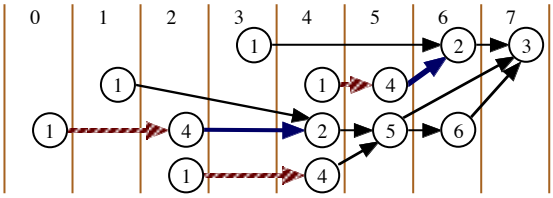
As mentioned above, if a TEM C_1 covers another TEM C_2, C_1 can *'simulate'* C_2. On the other hand, by definition Def. 6, for any fault in an acyclic sequential circuit, the corresponding fault is defined in either TEM of C_1 and C_2. Thus, we can form the following theorem.

Theorem 2: Let S be an acyclic sequential circuit. Let C_1 and C_2 be TEMs of S. Let F_1 and F_2 be the set of faults in C_1 and C_2, respectively (Def. 6). If TEM C_1 covers TEM C_2, the following holds: If a fault f_2 $(\in F_2)$ in C_2 is testable, fault f_1 $(\in F_1)$ in C_1 corresponding to f_2 is also testable. □

From the theorem, we can see that test generation for *all* the TEMs that are not covered by any other TEMs, i.e., *maximal* TEMs of an acyclic sequential circuit is necessary and sufficient



(a) Topology graph: G_m.



(b) Time-expansion model of G_m: E_m.

Figure 8. Example of max-testable circuit.

to obtain a complete test sequence for all testable faults in the circuit. For example, sequential circuit S has two maximal TEMs $C_{E_2}(S)$ and $C_{E_3}(S)$, i.e., any TEM is covered by either $C_{E_2}(S)$ or $C_{E_3}(S)$.

Thus, we can reduce the number of TEMs for complete test generation of sequential circuits, even though the number of control sequences for H-registers is unlimited.

4 Max-testable structure

In general, an acyclic sequential circuit has several maximal TEMs, e.g., the maximal TEMs of sequential circuit S (Fig. 1) are $C_{E_2}(S)$ and $C_{E_3}(S)$. However, if the number of maximal TEMs is just one for an acyclic sequential circuit i.e., the circuit has the *maximum* TEM, a complete test set for the circuit can be generated only by performing combinational test generation for the maximum TEM. If a sequential circuit has the maximum TEM, the sequential circuit is called *max-testable*.

4.1 Path-Adjustable Structure

Consider sequential circuit S (Fig. 1), again. Recall that TEG E_3 (Fig.5) covers another TEG E_1 (Fig. 3). Focus on an arc $(6,7)$ which corresponds to an H-register j (called *hold arc*, for short) in S, we can consider that TEG E_3 is obtained from E_1 by *adjusting* the length of the arc $(6,7)$ (i.e., the difference of $t(6)$ and $t(7)$) so that the tail 1 of a path $(1,6,7)$ is separated from that of another path $(1,2,3,7)$ that has the same head 7. In this way, if a common tail of different paths that have the common head can be divided into distinct vertices as respective tails of the paths under Condition C5 in Def. 2, another TEG covering the original TEG can be obtained.

Here, as a sufficient condition for the maximum TEM, we have the following lemma.

Lemma 4: Let $G=(V,A,r)$ be the topology graph of an acyclic sequential circuit S. Let $E=(V_E,A_E,t,l)$ be a TEG for G. A TEG is maximum if for any pair of vertices $u,v \in V_E$, the following holds.

$$\forall p,q \in P_E(u,v)[H_E(p)=H_E(q)],$$

where $P_E(u,v)$ denotes the set of paths whose head and tail are u and v in E, respectively, and $H_E(p)$ denotes the set of hold arcs (u',v'), such that the corresponding arc $(l(u'),l(v'))$ is an H-register (i.e., $(l(u'),l(v'))=h$). on path p. □

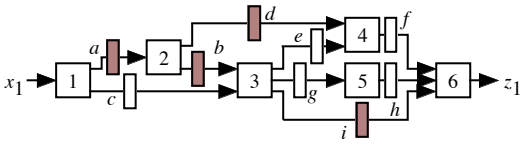


Figure 9. Sequential circuit S_2.

Example 6: Consider a TEG E_m for a topology graph G_m (Fig. 8). For any pair of paths p,q whose tail and head are severally the same in E_m, the set $H_{E_m}(p)$ of hold arcs is equal to that $H_{E_m}(q)$. Hence, TEG E_m is the maximum, and consequently the circuit represented by topology graph G_m is max-testable. □

Although TEG E_m shown in the above example is the maximum, it seems to be hard to derive the maximum TEG for G because *adjustability* of each hold arc depends on resultant adjustment of the other hold arc. From the practical point of view, An acyclic sequential circuit whose maximum TEG (TEM) can be derived easily is interesting and important. Here, recall that Condition C5 in Def. 2 is for more than one hold arcs that correspond to a certain H-register in an acyclic sequential circuit. Such arc duplication for an H-register is possible in a TEG when there exist more than one paths from the H-register to an primary output in the circuit. Hence, here we consider a sequential circuit whose maximum TEG can be derived by adjusting each hold arc independent of the others as follows.

Definition 9 (Path-adjustable structure): Let S be an acyclic sequential circuit. Let $G=(V,A,r)$ be the topology graph of S. Let $P(u,v)$ denote a set of paths from u to v $(u,v \in V)$. If G satisfies the following condition, sequential circuit S is said to be *path-adjustable*.

(CPA) Let V' $(\subseteq V)$ be a set of vertices which are reachable from some arc $a_h (\in A)$ such that $r(a_h)=h$ (H-register). Let u,v be any pair of vertices in V'. For any pair of paths $p,q \in P(u,v)$,

(1) if $H(p)=H(q)$, then $d(p)=d(q)$, else

(2) if $H(p) \neq H(q)$, then

$$H(p) \cap H(q) \neq \phi \Rightarrow H(p) \subset H(q) \vee H(p) \supset H(q).$$

Here $d(p)$ denotes the sum of labels $r(a)$ of arcs a $(\in A)$ such that $r(a) \in Z^+$ (L-register) in a path p, and $H(p)$ denotes the set of arcs a such that $r(a)=h$ (H-register) in a path p. □

Example 7: Consider a sequential circuit S_2 shown in Fig. 9. In this figure, a,b,d and i are H-registers, and the others are L-registers. For example, let us focus on an H-register a. There exist four paths to be considered for a: $p_1=(2,d,4,f,6)$, $p_2=(2,b,3,e,4,f,6)$, $p_3=(2,b,3,g,5,h,6)$ and $p_4=(2,b,3,i,6)$. Then, $H(p_1)=\{d\}, H(p_2)=\{b\}, H(p_3)=\{b\}$ and $H(p_4)=\{b,i\}$. For p_1 and p_2, $H(p_1) \cap H(p_2)=\phi$, this is in neither case. For p_2 and p_3, $H(p_2)=H(p_3)=\{b\}$ and $d(p_2)=d(p_3)$, i.e., case (1). For p_2 and p_4, $H(p_2) \subset H(p_4)$, i.e., case (2). Similarly, all the other pairs of paths in this circuit S_2 also satisfy Condition CPA, and hence S_2 is path-adjustable. Note that a sequential circuit S (Fig. 1) is not path-adjustable. As a result, we can obtain the maximum TEM for S_2 as shown in Fig. 10. The control input sequence obtained from the TEM (by procedure τ_S) is $I_H(a)=(L,L,L,H,X,X,X)$, $I_H(b)=(X,X,L,H,L,X,X)$, $I_H(d)=(X,L,H,H,H,X,X)$, $I_H(h)=(X,X,X,X,X,L,X)$. □

For a path-adjustable circuit, a TEG that satisfies the condition

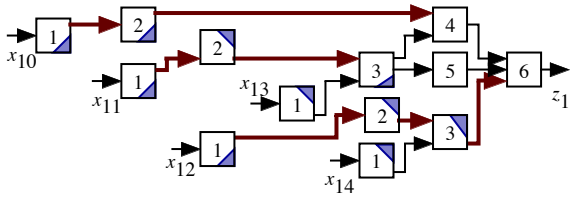


Figure 10. Maximum TEM for S_2.

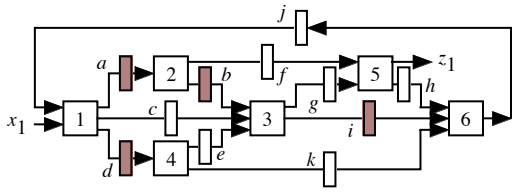


Figure 11. Sequential circuit S_3.

in Lemma 4. Therefore, we have the following theorem.

Theorem 3: A path-adjustable sequential circuit is max-testable. □

4.2 Application to Partial Scan Design

From Theorem 3, we can see that for any sequential circuit, by selecting a sufficient set of scan registers so that the resulting kernel is path-adjustable, a complete test sequence for the circuit can be obtained by using a combinational test generator for only the maximum TEM of the kernel (provided that the test generator can deal with multiple faults). On the other hand, from Def. 9, we have the following corollary.

Corollary 2: All the following sequential circuits are path-adjustable.
(1) balanced structures [5],
(2) internally-balanced structures [7], and
(3) acyclic sequential circuits without H-registers. □

Therefore, for a sequential circuit, the hardware overhead of the partial scan based on path-adjustable structure is smaller than that based on the structures mentioned in Corollary 2.

Example 8: Consider a sequential circuit S_3 shown in Fig. 11. In this figure, a,b,d and i are H-registers, and the others are L-registers. In the partial scan design based on path-adjustable structure, the minimum number of scan registers is two, e.g., by scanning L-registers j and k, the resulting kernel becomes path-adjustable. Note that there is an alternative DFT solution: if one L-register j is scanned and another L-register k is replaced with an H-register, then the resultant circuit is also path-adjustable.

On the other hand, in the partial scan design based on balanced structure, the minimum number of scan registers is five, e.g., the set of registers to be scanned is $\{b,c,e,f,k\}$. When the kernel is made an acyclic structure without H-registers, the minimum number of scan registers is also five, e.g., $\{a,b,d,h,i\}$. □

Therefore, it is seen that we can obtain complete test sequences for sequential circuits with low hardware overhead based on max-testable structure.

5 Conclusions and Future Works

In this paper, we presented a method of test generation for acyclic sequential circuits with *hold* registers. A *complete* test set for an acyclic sequential circuit can be obtained by applying a *combinational* test generator to all the *maximal time-expansion models (TEMs)* of the circuit. As a class of *max-testable* sequential circuits, referring to acyclic sequential circuits for which the number of maximal TEMs is one, i.e, the *maximum* TEM exists, we introduced *path-adjustable* structure. The class of path-adjustable sequential circuits properly includes several known classes of acyclic sequential circuits such as balanced structures and acyclic sequential circuits without hold registers for which test generation can be also performed by using a combinational test generator. Therefore, the hardware overhead for partial scan based on our path-adjustable structure is substantially smaller than that based on balanced or acyclic sequential structure without hold registers.

As future works, several issues are remaining.

- The condition in the definition of path-adjustable structure is a sufficient one for existence of the maximum TEM for acyclic sequential circuit. We believe that there exists a lager class of max-testable sequential circuits, and hence the hardware overhead of DFT for complete test sequences can be reduced further.
- We are now investigating an algorithm for finding an optimal partial scan / hold register insertion based on max-testable structure with minimum hardware overhead.
- The length of test sequences obtained from test generation using TEMs depends on the structure of the TEMs. Hence, it is also important to find optimal TEMs which minimize the length of resulting test sequences.

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