A Method of Test Generation for Path Delay Faults in Balanced Sequential Circuits

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Abstract

This paper shows that path delay fault test generation problem for sequential circuits with balanced structure can be reduced to segment delay fault test generation problem for their combinationally transformed circuits. We also propose a test generation method and a partially enhanced scan design method for path delay fault.

1. Introduction

For recent high performance VLSI circuits, delay testing is necessary to reach an acceptable quality level. Until now, many delay fault models are investigated[1]. Path delay fault model[2] is one of the most general models among them because distributed faults along paths can be tested and the delay size of detectable faults is scalable. However, the path delay fault model has disadvantages that the number of faults with respect to the number of gates in a circuit is exponential in worst case and test generation for faults is generally hard. In order to avoid the former disadvantage, a technique for selecting paths which are targets of testing[3] and techniques for re-synthesizing circuits such that the path count is reduced[4, 5] are proposed. The latter disadvantage can be avoided by synthesis-for-testability (SFT) techniques[1, 6] and design-for-testability (DFT) techniques[1, 7, 8].

In general, for sequential circuits, path delay fault coverage is low because there are many undetectable faults and time for generating delay tests is long because identification of undetectable faults is time consuming problem. Chakraborty et al.[8] classified undetected faults into three categories: (A) combinationally non-activated paths, (B) sequentially non-activated paths, and (C) unobservable fault effect. Path delay faults of the category (A) can only be made detectable by SFT or DFT and combinational logic can be designed for path delay testability[6]. Regarding the category (B), the fault effect propagation problem is almost the same as fault effect propagation problem of stuck-at fault model. Chakraborty et al.[8] showed that almost of sequentially undetectable faults are in the category (B). In order to ease complexity of test generation, sequentially undetectable faults must be decreased. The fully enhanced scan technique [7] and the partially enhanced scan technique [8] are proposed to achieve this claim.

Given a sequential circuit, the fully enhanced scan technique replaces each FF by an enhanced scan FF. An enhanced scan FF can store two bits to apply two consecutive vectors. For a sequential circuit designed by this technique, we can use a combinational path delay test generation algorithm to generate delay tests. Therefore high fault coverage can be achieved with short test generation time. However, this technique has disadvantage that hardware overhead which is caused by extra memory elements of enhanced scan FFs is very high. This disadvantage can be avoided using partial scan techniques. In the partially enhanced scan technique[8], for a sequential circuit, scan FFs are selected such that the feedback paths in the circuit are broken if these scan FFs are removed. For a sequential circuit designed by this partial scan technique, we can consider the circuit to be a feedback free circuit during test generation and test generation of the feedback free circuit is much easier than the original one. However, there is room for facilitating test generation because it still requires a sequential path delay test generation algorithm.

For stuck-at fault testability of sequential circuits, in order to select scan FF effectively, sequential circuits are classified by their structure as follows: {*sequential circuits of acyclic structure*} ⊃ {*sequential circuit of internally balanced structure*} ⊃ {*sequential circuits of balanced structure*} and that internally balanced structures allow *test gen-*

eration with combinational test generation complexity[9]. Although the number of scan FFs required to make a given sequential circuit acyclic is generally smaller than the number of scan FFs required to make the circuit internally balanced[10], in order to apply a combinational test generation algorithm to the acyclic sequential circuit, time frame expansion must be used[11] or multiple faults must be dealt with[10]. For a sequential circuit of balanced structure, the test generation problem of the circuit can be reduced to that of the combinationally equivalent circuit which can be obtained by replacing each FF in the original sequential circuit by a wire. In other words, instead of using a sequential test generation algorithm, tests of stuck-at faults in the sequential circuit can be obtained by generating tests for corresponding stuck-at faults in the combinationally transformed circuit using a combinational test generation algorithm. Therefore test generation time can be reduced significantly [12].

In this work, we introduce this concept into path delay test generation for sequential circuits and propose a method of path delay test generation for sequential circuits of balanced structure. To put it concretely, in our test generation method for path delay faults in a sequential circuit of balanced structure, we first make the sequential circuit into the combinationally transformed circuit. Next, we generate tests for segment delay faults[13] in the combinational circuit instead of generating tests for the path delay faults in the sequential circuit. And finally, we transform the generated tests for segment delay faults of the combinational circuit into tests for path delay faults of the original sequential circuit. We also show reducibility between the test generation problem for path delay faults of a balanced sequential circuit and that for corresponding segment delay faults of its combinationally equivalent circuit and propose a DFT method for making general sequential circuits path delay testable using enhanced scan FFs.

2. Preliminaries

2.1. Circuit Model

A sequential circuit is considered as an interconnection of combinational logic gates and FFs. The circuit is represented by a directed graph defined as follows.
Definition 1 A *circuit graph* for a sequential circuit S is a directed graph $G = (V, A, w)$.
- V is the set of vertices representing primary inputs, primary outputs and gates in S.
- $A \subset V \times V$ is the set of arcs representing FFs and wires in S.
- $w : A \mapsto \{0\} \cup N$ (natural numbers) defines the weights of the arcs where a weight is the number of FFs between the corresponding gates. □

In this work, we assume that FFs have no hold capability and FFs are of D-type. This assumption does not impose restriction on circuit representation because any FF which has hold capability or is the other type can be modeled by a D-type FF and some logic gates.

2.2. Delay Fault Model

In this work, we are targeting path delay faults in sequential circuits defined as follows.
Definition 2 In a sequential circuit, a path is defined as an order set of gates $\{g_1, g_2, \ldots, g_n\}$, where g_1 is a primary input or an FF and g_n is a primary output or an FF. Also, gate g_i is an input to gate $g_{i+1}(1 \le i \le n-1)$. A path has a delay fault if propagation time of rising or falling signal transition through the path exceeds a specified clock period. Such a delay fault on a path is said to be a *path delay fault (PDF)*[1, 2, 8]. □

PDFs can be classified as follows: *singly-testable* (ST), *multiply-testable* and *singly-testable dependent* [14]. For each ST PDF, there exists at least one delay test that is either robust, validatable non-robust, or non-robust. These tests are identified by the off-input values of the PDF. In order to simplify the discussion, we consider generating delay tests for ST PDFs in a combinational part of a sequential circuit and do not distinguish conditions of off-inputs, i.e., we consider generating non-robust delay tests for ST PDFs.
Definition 3 Let S and p be a sequential circuit and a path in S, respectively. Let f and S_f be a rising (falling) PDF on p and a faulty circuit of S produced by f, respectively. The fault f is *testable* if there exists an input sequence t for S and S_f such that the following conditions hold.
1. A rising (falling) signal transition is launched at the starting point (an FF or a primary input) of p of S by t.
2. The transition launched at the starting point of p is propagated to the ending point (an FF or a primary output) of p along p in S by t.
3. The captured or observed value induced by the transition at the ending point of p of S_f is different from that of S.
4. The output sequence of S and that of S_f are different.

Such an input sequence t is regarded as a *PDF test sequence*. □
Definition 4 In a combinational circuit, a segment is defined as an order set of gates $\{g_1, g_2, \ldots, g_n\}$, where n is the length of the segment. The length of the segment, n, can be anywhere from 1 to the number of gates in the longest path in the circuit. Also, gate g_i is an input to gate $g_{i+1}(1 \le i \le n-1)$. A segment has a delay fault if propagation time of rising or falling signal transition through the segment exceeds a specified limit. Such a delay fault on a segment is said to be a *segment delay fault (SDF)*[1, 13]. It is assumed that a segment delay fault is large enough to cause a delay fault on all paths that include the segment. □

Definition 5 Let C and s be a combinational circuit and a segment in C, respectively. Let f and C_f be a rising (falling) SDF on s and a faulty circuit of C produced by f, respectively. The fault f is *testable* if there exists an input vector pair (t_1, t_2) for C and C_f such that the following conditions hold.

1. A rising (falling) signal transition is launched at the starting point (a gate or a primary input) of s of C by (t_1, t_2).
2. The transition launched at the starting point of s is propagated to the ending point (a gate or a primary output) of s along s in C by (t_1, t_2).
3. The value induced by the transition at the ending point of s of C_f is different from that of C.
4. The second output vector of C and that of C_f are different.

Such an input vector pair (t_1, t_2) is regarded as an *SDF 2-pattern test*. □

Notice that, it is conceivable that conditions of off-inputs of an SDF are the same as that of a PDF.

2.3. Circuit Transformation

Definition 6 Given a sequential circuit S whose circuit graph is acyclic, we define its combinational equivalent $C(S)$ as the combinational circuit formed by replacing each FF in S by a buffer. Such a transformation is said the *combinational transformation (C-transformation)*. □

Notice that the original C-transformation [9] replaces FFs by wires. In order to clarify discussions about starting and ending points of SDFs, we use buffers instead of wires.

3. Balanced Structure

Our target circuit structure in our test generation method proposed in Section 4 is *balanced structure*. Balanced structure is defined as follows.

Definition 7 [15] A circuit graph G is defined to be a *balanced structure* if it satisfies the following conditions.

1. G is acyclic.
2. $\forall(v_i, v_j) \in G$ all directed paths (if any) between them have the same weight. □

Notice that the original definition of balanced structure [12] takes FFs which have hold capable into account. In this work, we need not consider such a FF because we assumed that such a FF was modeled by a FF of D-type with some logic gates.

Example 1 An example of a sequential circuit of balanced structure and its circuit graph are shown in Figure 1. In Figure 1 (a), from C_1 to C_6 are combinational logic blocks and from FF_1 to FF_7 are FFs.

In our test generation method, we generate delay tests for each output cone of a sequential circuit of balanced structure. The circuit structure of the output cone is *strongly*

balanced structure as Theorem 1 below. Strongly balanced structure is defined as follows.

Definition 8 A circuit graph is defined to be a *strongly balanced structure*[15] if we can assign integer values $t(v_i)$ to its vertices such that it satisfies the condition:
$$t(v_i) = t(v_j) + w(a) \quad \forall a(v_i, v_j). \qquad \square$$

Example 2 An example of a sequential circuit of strongly balanced structure and its circuit graph are shown in Figure 2. In Figure 2 (b), integer values (boldfaced numbers in the figure) can be assigned to all vertices without contradiction.

Theorem 1 [15] *A circuit graph is a balanced structure iff it is strongly balanced with respect to each input (or output) cone.*

For each output cone circuit of a sequential circuit of balanced structure, the following property is derived from Definition 1 and Theorem 1. Let $t_{\max}$ be the maximum value among values assigned to vertices of its circuit graph. Let I_i be a vertex, which corresponds to an input of the cone circuit, of the circuit graph. Let O be the vertex, which corresponds to the output of the cone circuit, of the circuit graph. An output value of O at $t_{\max}$ is only affected by an input value for I_i applied at $(t_{\max} - t(I_i))$.

4. Test Generation

In this section, we propose a new test generation method for PDFs of balanced sequential circuits.

4.1. Test Generation Method

Given a balanced sequential circuit S^B, the test generation method proceeds as follows.

For each output cone circuit S_c^B of S^B,

1. Make a PDF list F of S_c^B.
2. Transform S_c^B into the combinationally equivalent circuit $C(S_c^B)$ by C-transformation.
3. Transform F into a SDF list F^C of $C(S_c^B)$.
4. Generate a 2-pattern test set T^C for F^C of $C(S_c^B)$.
5. Transform T^C into a delay test set T for F of S_c^B.

Notice that, if S^B is of strongly balanced structure, we can apply the above procedure for the whole circuit S^B without considering cone circuits of S^B.

Here, we define the fault transformation from F into F^C in step 3 of the above procedure as follows.

Definition 9 Let p be a path in S^B. Let g_s and g_e be the starting point and the ending point of p, respectively. Let s be a segment in $C(S^B)$ such that the starting point is a primary input or a buffer corresponding to g_s and the ending point is a primary output or a buffer corresponding to g_e. Let f_p and f_s be a rising (resp. falling) PDF on p and a rising (resp. falling) SDF on s, respectively. A transformation φ from f_p of S^B into $f_s(=\varphi(f_p))$ of $C(S^B)$ is called the *fault transformation*. □
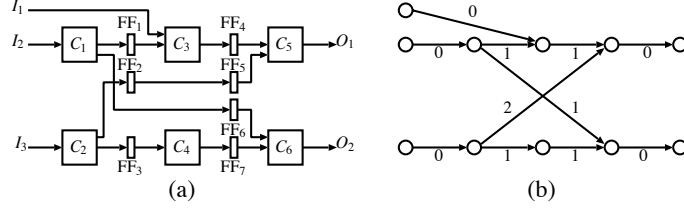
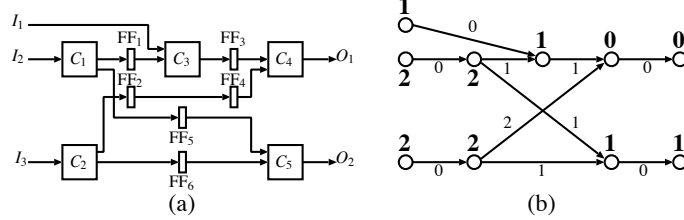**Figure 1. Balanced sequential circuit (a) and its circuit graph (b).**

Figure 2. Strongly balanced sequential circuit (a) and its circuit graph (b).

It is obvious that any PDF in S^B can be transformed into an SDF in $C(S^B)$ by the fault transformation. There exists a one-to-one mapping from a PDF in S^B to an SDF in $C(S^B)$.

The delay tests transformation in step 5 is defined as *sequence transformation* in the next subsection.

4.2. Reducibility of Test Generation Problems

Given an balanced sequential circuit S^B, our task of PDF test generation is to generate delay tests for all the testable PDFs. To prove the test generation method can generate delay tests for all the testable PDFs, we show that test generation problem[1] for a set of all the PDFs F^B in S^B can be reduced to that for a set of SDFs F^{CB} in $C(S^B)$ where an SDF is transformed from a PDF by the fault transformation.

We first consider strongly balanced sequential circuits.

Let G be a circuit graph of a strongly balanced sequential circuit S^{SB}. Let $t(q_i)$ be an integer value which can be assigned to a vertex q_i such that it satisfies the condition of Definition 8. Let t_{max} and t_{min} be the maximum value and the minimum value among values assigned to vertices of G, respectively. Let $I_j(j = 1, 2, \ldots, n)$ be a vertex, which corresponds to an input of S^{SB}, of G. A vector $T_I = (\alpha_1, \alpha_2, \ldots, \alpha_n)$ such that $\alpha_j = t_{max} - t(I_j) + 1$ is said to be an *input timing vector* of S^{SB}. For example, an input timing vector of the circuit of Figure 2 is $T_I = (2, 1, 1)$ whose coordinates correspond to the primary inputs (I_1, I_2, I_3).

Let L be $t_{max} - t_{min} + 2$. Let (v_1, v_2) be an n-bit vector pair where a vector v_l is $(v_1^l, v_2^l, \ldots, v_j^l, \ldots, v_n^l)$. A vector

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[1] A test generation problem for a fault set of a circuit consists of both generating tests for all the testable faults in the fault set and to identify untestable faults in the fault set.
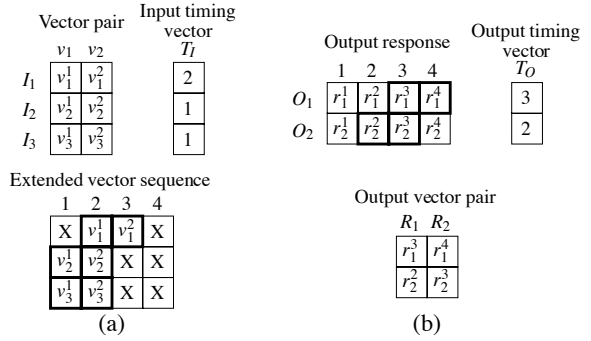

Figure 3. Extended vector sequence (a) and output vector pair (b)

sequence $[x_{ij}]$ of length L such that
$$
x_{ij} = \begin{cases} v_j^1 & \text{if } i = \alpha_j \\ v_j^2 & \text{if } i = \alpha_j + 1 \\ \text{don't care} & \text{otherwise} \end{cases}
$$
is said to be an *extended vector sequence of* (v_1, v_2) *with respect to* T_I. A transformation M which transforms from (v_1, v_2) into the extended vector sequence with respect to T_I is referred to as *sequence transformation with respect to* T_I. For example, in Figure 3(a), a vector pair for the circuit of Figure 2 is transformed into the extended vector sequence with respect to the input timing vector T_I.

Let $O_k(k = 1, 2, \ldots, m)$ be an vertex, which corresponds to an output of S^{SB}, of G. A vector $T_O = (\beta_1, \beta_2, \ldots, \beta_m)$ such that $\beta_k = t_{max} - t(O_k) + 1$ is said to be an *output timing vector* of S^{SB}. For example, an output timing vector of the circuit of Figure 2 is $T_O = (3, 2)$ whose coordinates cor-

respond to the primary outputs (O_1, O_2).

Let $R(C(S^{SB}))$ be an output vector pair of $C(S^{SB})$ when an n-bit vector pair (v_1, v_2) is applied to $C(S^{SB})$. Let $r(O_k, \beta_k)$ be an output response of a primary output corresponding to O_k at time β_k when the extended sequence of the vector pair (v_1, v_2) with respect to T_I is applied to S^{SB}. Let $R(S^{SB})$ be a vector pair such that $R(S^{SB}) = ((r(O_1, \beta_1), r(O_2, \beta_2), \ldots, r(O_m, \beta_m)), (r(O_1, \beta_1 + 1), r(O_2, \beta_2 + 1), \ldots, r(O_m, \beta_m + 1)))$. Such a vector pair $R(S^{SB})$ is referred to as an *output vector pair with respect to T_O* of S^{SB}. For example, consider again the circuit of Figure 2, an output vector pair with respect to the output timing vector T_O is obtained from an output sequence as shown in Figure 3(b).

For the relation between $R(C(S^{SB}))$ and $R(S^{SB})$, we can have the following lemma.

Lemma 1 *The response $R(C(S^{SB}))$ of $C(S^{SB})$ for any n-bit vector pair and the response $R(S^{SB})$ of S^{SB} for the extended sequence of the vector pair with respect to T_I of S^{SB} are identical.*

For testable PDF of S^{SB}, we can have the following lemma.

Lemma 2 *For any testable PDF of S^{SB}, there exists a test sequence formed as an extended sequence with respect to T_I.*

We call such a test sequence formed as an extended sequence a *2-pattern extended test sequence*.

The proofs of Lemma 1 and Lemma 2 are omitted here due to limitations of space. However, Lemma 1 can be easily proved from Definition 8 and Lemma 2 can be easily proved from Definition 8 and Definition 3.

Let F^{SB} be the set of all the PDFs of S^{SB}. Let F^{CSB} be a set of SDFs of $C(S^{SB})$, where an SDF is transformed from a PDF by the fault transformation φ.

Theorem 2 *The test generation problem for F^{SB} of S^{SB} can be reduced to the test generation problem for F^{CSB} of $C(S^{SB})$.*

Proof: There exists a one-to-one mapping φ from a PDF in S^B to an SDF in $C(S^B)$. We show that (*i*) a PDF $f_p \in F^{SB}$ of S^{SB} is testable iff $\varphi(f_p) \in F^{CSB}$ of $C(S^{SB})$ is testable and (*ii*) there exist a delay test transformation which transforms from a delay test for $\varphi(f_p)$ of $C(S^{SB})$ into a delay test for f_p of S^{SB}.

(*i*) <u>*Sufficiency*</u>: We show that if $f_p \in F^{SB}$ is testable, $f_s = \varphi(f_p) \in F^{CSB}$ is also testable. Let S_f^{SB} and $C(S_f^{SB})$ be faulty circuits of S^{SB} produced by f_p and of $C(S^{SB})$ produced by f_s, respectively. We divide S_f^{SB} and $C(S_f^{SB})$ into faulty parts and fault free parts and consider these faulty and fault free parts individually.

Faulty parts: Let C be a maximum region of connected combinational subcircuit in S_f^{SB} such that its inputs are either primary inputs or outputs of FFs, its outputs are either primary outputs or inputs of FFs, and it has the starting

point of f_p as an input and the ending point of f_p as an output. From Lemma 2, there exists a 2-pattern extended test sequence t_p if f_p is testable. From Definition 3, if f_p is testable, t_p must justify a 2-pattern test (v_1^C, v_2^C) for f_p of C to the inputs of C from primary inputs of S^{SB} and must propagate an error appeared at an output corresponding to the ending point of f_p of C to a primary output of S^{SB}. Let C' be a subcircuit corresponding to C in $C(S_f^{SB})$. Circuits C and C' are the same faulty circuits and f_p of C and f_s of C' can be considered as PDFs of combinational circuits C and C'. Therefore if f_p is testable by (v_1^C, v_2^C) in C, f_s is also testable by (v_1^C, v_2^C) in C'.

Fault free parts: Consider a circuit $S^{SB\prime}$ produced from S_f^{SB} by replacing C with primary inputs and primary outputs and a circuit $C(S^{SB\prime})$ produced from $C(S_f^{SB})$ by replacing C' with primary inputs and primary outputs. Let G' be the circuit graph of $S^{SB\prime}$ and its each vertex has the same integer value of the corresponding vertex of G. Let T_I' and T_O' be the input timing vector and the output timing vector of $S^{SB\prime}$, respectively. Let t_p' be an extended sequence of a vector pair with respect to T_I'. Let M' and M'^{-1} be an sequence transformation with respect to T_I' and its inverse transformation, respectively. Let $R(C(S^{SB\prime}))$ be the output vector pair when $M'^{-1}(t_p')$ is applied to $C(S^{SB\prime})$. Let $R(S^{SB\prime})$ be the output vector pair with respect to T_O' when t_p' is applied to $S^{SB\prime}$. From Lemma 1, $R(S^{SB\prime})$ and $R(C(S^{SB\prime}))$ are identical because $S^{SB\prime}$ and $C(S^{SB\prime})$ are a fault free strongly balanced circuit and its combinationally equivalent circuit, respectively. Therefore, if (v_1^C, v_2^C) can be justified to the inputs of C in S_f^{SB} when t_p is applied to the primary inputs of S^{SB}, (v_1^C, v_2^C) must be justified to the inputs C' in $C(S_f^{SB})$ by applying $M^{-1}(t_p)$ to the primary inputs of $C(S_f^{SB})$, where M^{-1} is the inverse transformation of M. Furthermore, if the error appeared at the output of C affects a primary output of S_f^{SB} when t_p is applied to S_f^{SB}, the error appeared at the output of C' must affects a primary output of $C(S_f^{SB})$ when $M^{-1}(t_p)$ is applied to $C(S_f^{SB})$. Thus, if the responses of S^{SB} and S_f^{SB} when t_p is applied are different, the responses of $C(S^{SB})$ and $C(S_f^{SB})$ when $M^{-1}(t_p)$ is applied are different.

Hence, if f_p is testable by t_p, f_s is also testable by $M^{-1}(t_p)$.

<u>*Necessity*</u>: We show that if $f_s \in F^{CSB}$ is testable, $f_p = \varphi^{-1}(f_s) \in F^{SB}$ is also testable as the same way as the proof of sufficiency.

Faulty parts: Consider again faulty subcircuit C' and C. From Definition 5, if f_s is testable in C', there exists a 2-pattern test $(v_1^{C'}, v_2^{C'})$ for f_s of C'. C' and C are the same faulty circuits and f_s and f_p are the same PDFs of these circuits. Therefore if f_s is testable by $(v_1^{C'}, v_2^{C'})$ in C', f_p is also testable by $(v_1^{C'}, v_2^{C'})$ in C.

Fault free parts: Consider again the circuits $C(S^{SB\prime})$

and $S^{SB\prime}$. Let t_s' be an input vector pair of $C(S^{SB\prime})$. Let $R'(C(S^{SB\prime}))$ be the output vector pair when t_s' is applied to $C(S^{SB\prime})$. Let $R'(S^{SB\prime})$ be the output vector pair with respect to T_O' when $M(t_s')$ is applied to $S^{SB\prime}$. From Lemma 1, $R'(C(S^{SB\prime}))$ and $R'(S^{SB\prime})$ are identical because $S^{SB\prime}$ and $C(S^{SB\prime})$ are a fault free strongly balanced circuit and its combinationally equivalent circuit, respectively. Therefore, if $(v_1^{C\prime}, v_2^{C\prime})$ can be justified to the inputs of $C\prime$ in $C(S_f^{SB})$ when a 2-pattern test t_s is applied to the primary inputs of $C(S^{SB})$, $(v_1^{C\prime}, v_2^{C\prime})$ must be justified to the inputs C in S_f^{SB} by applying $M(t_s)$ to the primary inputs of S_f^{SB}. Furthermore, if the error appeared at the output of C' affects a primary output of $C(S_f^{SB})$ when t_s is applied to $C(S_f^{SB})$, the error appeared at the output of C must affects a primary output of S_f^{SB} when $M(t_s)$ is applied to S_f^{SB}. Thus, if the responses of $C(S^{SB})$ and $C(S_f^{SB})$ when t_s is applied are different, the responses of S^{SB} and S_f^{SB} when $M(t_s)$ is applied are different.

Hence, if f_s is testable by t_s, f_p is also testable by $M(t_s)$.

(*ii*) From (*i*), any 2-pattern test t_s for $f_s = \varphi(f_p) \in F^{CSB}$ can be transformed into a delay test $M(t_s)$ for $f_p \in F^{SB}$. Therefore, there exists a delay test transformation M such that M transforms from a delay test for $\varphi(f_p)$ of $C(S^{SB})$ into a delay test for f_p of S^{SB}. □

Next, we expand Theorem 2 into balanced sequential circuits.

Theorem 3 *The test generation problem for F^B of S^B can be reduced to the test generation problem for F^{CB} of $C(S^B)$.*
Proof: From Theorem 1, the output cone circuit S_c^B of each primary output of S^B is strongly balanced. From Theorem 2 the test generation problem for PDFs of S_c^B can be reduced to the test generation problem for corresponding SDFs of $C(S_c^B)$. The generated delay tests of S_c^B can be applied to S^B because the primary inputs of S^B except for the primary inputs of S_c^B do not affect the primary output of S_c^B. Therefore the theorem holds. □

4.3. Complexity of Reduction

For stuck-at fault model, the class of balanced sequential circuits has *combinational test generation complexity*[9]. For PDF model, we reduce test generation problem for a PDF f_p of a balanced sequential circuit S to test generation problem for an SDF f_s of its combinationally equivalent circuit C. Here, we briefly discuss (*i*) the time complexities of sequential PDF test generation and combinational SDF test generation, (*ii*) the time complexity of C-transformation, (*iii*) the sizes of circuits S and C, and (*iv*) the sizes of faults f_p and f_s.
(*i*) It is conceivable that the time complexity of combinational SDF test generation is much smaller than that of sequential PDF test generation.
(*ii*) It is obvious that the time complexity of C-transformation is much smaller than the time complexity of
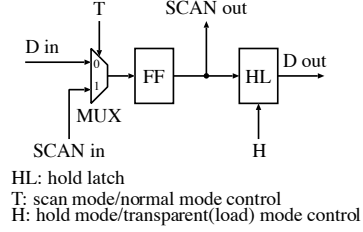

HL: hold latch
T: scan mode/normal mode control
H: hold mode/transparent(load) mode control

Figure 4. Enhanced scan FF.

combinational SDF test generation.
(*iii*) The numbers of gates of S and C are the same.
(*iv*) The numbers of gates on a path corresponding to f_p and on a segment corresponding to f_s are the same.
Therefore, we can say that the class of balanced sequential circuits has *combinational path delay test generation complexity*.

5. DFT for PDF testability

5.1. Partially Enhanced Scan Design

In order to apply the proposed test generation method to general sequential circuits, we use partial scan technique. For a PDF of a path in a sequential circuit, a transition must be launched at the starting point of the path by the system clock. Therefore each scan FF must store at least two bits. Such a scan FF is referred as an enhanced scan FF (ESFF) [7]. An example of such an ESFF is shown in Figure 4. The ESFF is composed of a standard scan FF and an extra hold latch (HL).

Our partially enhanced scan method for a given sequential circuit consists of the following two steps.
  1. Select FFs of the circuit such that the circuit becomes balanced structure if these FFs are removed.
  2. Replace each FF selected at the first step by an ESFF.

The first step is done by the Balancing Procedure of [12] or the Balancing Algorithm of [10]. The second step is just replacing FFs by ESFFs and making a scan chain. The number of scan FFs of this partially enhanced scan method for PDFs is the same as that of the methods of [12] and [10]. The extra hardware overhead of this partially enhanced scan method is $n \times Area(\mathrm{HL})$ compared with these methods where n is the number of ESFFs and $Area(\mathrm{HL})$ is the area of an extra hold latch. The area overhead of our partially enhanced scan method is smaller compared to fully enhanced scan method [7]. The test generation complexity of our partially enhanced scan method is smaller than the partially enhanced scan method based on acyclic structure [8] in return for paying larger hardware compared to the partially enhanced scan method [8].

5.2. Application of Delay Test

Given a circuit S designed by our partially enhanced scan method, the test plan for applying a 2-pattern extended test sequence t_p for a PDF f is as follows. N is the number of ESFFs in S, L is the length of t_p and t-th clock is operational speed clock to propagate transition through f. Each don't care value of t_p can be replaced by either 0 or 1.

For application of t_p, the t-th vector of t_p must be applied at operational speed after the $(t-1)$-th vector of t_p is applied. Therefore, the $(t-1)$-th vector and the t-th vector must be applied as follows. First, we scan in the $(t-1)$-th vector using scan mode for N scan clock cycles. Second, we transfer each value of the $(t-1)$-th vector to each HL by placing HLs in the load mode and then place HLs in the hold mode. Next, we scan in the t-th vector using scan mode for N scan clock cycles. Finally, we apply an operational speed clock for all the FFs using normal mode with placing HLs in the load mode. The other vectors of t_p can be applied as the above scheme or traditional scan scheme with placing HLs in the load mode. Notice that, in order to assume S is fault free circuits during application of vectors of t_p except for the t-th and the $(t-1)$-th vectors, low speed clocks must be applied to all the FFs in stead of system clock. During scan clocks are applied to ESFF, we must disable system clock for normal FFs (i.e., place normal FFs in the hold mode).

For observation of the response of t_p, it is sufficient that at least one error can be observed. If an error are propagated to a primary output, the error can be observe from the primary output. If an error are captured at an ESFF, the error can be scanned out and can be observed from the scan output of the circuit.

Consider reduction of test application time. Since each delay test for PDFs of S has many don't care values, it is conceivable that compaction techniques are useful for reducing test application time. The problem of test application time reduction is our future work.

6. Conclusion

In this paper, we proposed a method of path delay test generation for sequential circuits of balanced structure and showed the correctness of the method. We also proposed a DFT method for making general sequential circuits path delay testable using enhanced scan FFs. It is conceivable that the test generation time and fault coverage can be improved by the methods.

Future works are to evaluate effectiveness of the method by experiments using benchmark circuits and to reduce test application time.

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