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An Extended Class of Sequential Circuits with Combinational Test Generation Complexity*

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Abstract We introduce a class of sequential circuits with *internally switched balanced structure* which allows test generation with combinational test generation complexity. The proposed class includes any other known classes with this feature. This paper also considers faults in hold registers and switches regarded as macros, while any related work does not consider faults in such macros. Experimental results show the effectiveness of using combinational test generation for the circuits with internally switched balanced structure.

1 Introduction

Test generation for sequential circuits is, in general, a difficult and intractable task which may be unsolvable within a reasonable time for a large-scale circuit[1, 2]. When all the flip-flops of a circuit are replaced with scan flip-flops (*full scan design*), all the scan flip-flops are treated as equivalents to external I/O terminals and hence the test generation can be performed for the remaining circuit (called the "kernel circuit") with the exclusion of all flip-flops, i.e., for the combinational part of the sequential circuit. Therefore, the full scan design method can reduce the test generation problem for sequential circuits to the problem of test generation for combinational circuits.

To reduce area and delay overhead while preserving the above good feature of the full scan design, a class of sequential circuits that allow test generation with combinational test generation algorithms has been investigated[3, 4, 5, 6, 7]. Sequential circuits with *balanced structure* (B-structure)[6] are circuits with this feature. For a sequential circuit with B-structure, test generation problem can be reduced into the test generation problem for a combinational circuit obtained by replacing all flip-flops with wires.In [3], a sub-class of B-structure called *strongly balanced structure* is introduced to reduce test application time. In [5], B-structure is considered at register-transfer(RT) level. At this level, the functional behavior of the combinational logic such as "switch" can be considered, and *switched balanced structure*(SB-structure) is introduced as a larger class of B-structure. However, they consider only the functional behavior of switches and do not consider faults in switches.

For an acyclic structure, test generation methods using combinational test generation algorithm are proposed[7, 8, 9, 10]. Although these approaches allow test generation with combinational test generation algorithm, they use circuit models including multiple copies of the combinational blocks of the original sequential circuits. Therefore, the transformed circuit is much larger than the original circuit, and moreover, a single fault in the original circuit may correspond to a *multiple* fault in the transformed circuit. In general, the single stuck-at faults can be used to model other type of faults (see [1], pp.111–112), and hence multiple stuck-at faults can be modeled by single stuck-at faults. However, the approach requires additional circuitry for each fault to the circuit, and therefore, the size of the circuit under test generation is enlarged.

In [4], we introduced a structure called *internally balanced structure* (IB-structure) of sequential circuits that allow test generation with combinational test generation algorithm. Test generation problem for sequential circuits with IB-structure can be reduced into one for combinational circuits obtained by some transformation which preserves the size of circuits. In the definition in [4], only DFFs are considered, and other kinds of FFs are handled by replacing each FF with a circuit composed of a DFF and extra logic. The hold FF is handled by replacing it with a DFF and a multiplexor with feedback. However, IB-structure needs to be acyclic, and hence, it cannot have any hold FF in the definition in [4]. When considering only DFFs, the class of IB-structure is larger than the class of B-structures. Moreover, it is shown that $\{$FSMs which can be realized as a sequential circuit of acyclic structure$\}$ $=$ $\{$FSMs which can be realized as a sequential circuit of internally balanced structure$\}$ $\supset$ $\{$FSMs which can be realized as a sequential circuit of balanced structure$\}$.

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In this paper, we introduce a new structure called *internally switched balanced structure*(ISB-structure). This structure considers hold FFs as well as DFFs. We consider this structure at RT level, and incorporate the concept of SB-structure. The proposed structure derives larger class of circuits than B-structure, IB-structure and SB-structure. We show that circuits with ISB-structure allow test generation for combinational logic with *combinational test generation complexity*. Moreover, we give some sufficient conditions to detect faults in switches and hold registers (collections of hold FFs) that the related works did not consider when they are regarded as macros.

The rest of this paper is organized as follows. In Section 2, the internally switched balanced structure and some notations are provided. Section 3 considers necessary and/or sufficient conditions to generate tests for faults in several components of circuits. Experimental results show the effectiveness of test generation using combinational test generation algorithms for circuits with ISB-structure in Section 4. Finally, Section 5 concludes the paper.

2 Preliminaries

We define *internally switched balanced structure* (ISB-structure) for register-transfer level (RTL) circuits. An RTL circuit is composed of registers, switches, combinational logic and signal lines that connect these elements. The registers are classified into two types: load registers and hold registers. A hold register has an explicit LOAD ENABLE control signal controllable from the outside of the circuit and has two operation modes: LOAD and HOLD modes, while a load resister always operates in LOAD mode. A switch is a multiplexer or a bus whose control signals are controllable from the outside of the circuit. A combinational logic is partitioned into *clouds*, where each cloud is a maximal region of connected combinational logic excluding switches and fanout points at primary inputs. The inputs of clouds are either primary inputs, fanout branches of primary inputs, or outputs of registers, and the outputs are either primary outputs or inputs to registers.

The number of registers included in a path is called the sequential depth of the path. Suppose x is a primary input with fanout branches, and y_i and y_j are branches of x. If any pair of paths from y_i and y_j to the same primary output have different sequential depths or include a register which appears exactly one of these paths, then y_i and y_j are called *separable*.

Definition 1 (Extended Combinational Transformation) *A transformation based on the following two operations with a circuit S of acyclic structure is called the extended combinational transformation (C^*-transformation).*

1. **Separation of primary inputs:** *For each primary input x with fanout branches, separate it as follows. Let Y denote a set of the fanout branches of a primary input. Let us obtain the smallest partition Π of Y which satisfies the following statement: If branches y_a and y_b belong to different blocks $Y(i)$, $Y(j)$ of partition Π ($y_a \in Y(i)$, $y_b \in Y(j)$, $Y(i) \neq Y(j)$) then y_a and y_b are separable. Each partitioned block $Y(i)$ is provided with a new primary input x_i separated from the original primary input x (as shown in Fig.1(b)).*
2. **C-transformation:** *Replace each register by a data signal line.*

Note that we can uniquely obtain the smallest partition Π for each primary input. In this way, for a given acyclic circuit S, the resulting circuit from the separation of primary inputs and the resulting circuit from the C^*-transformation are uniquely determined. Let S^* and $C^*(S)$ denote these circuits, respectively. Figure1 shows an RTL circuits S, S^* and $C^*(S)$, where $C_1, C_1, C_2, \cdots C_5$ are clouds, SW is a switch, r_1 is a hold register and r_2, r_3 and r_4 are load registers. Among three fanout branches y_1, y_2, y_3 of x, pairs (y_1, y_2) and (y_1, y_3) are separable, and x is separated into two primary inputs x_1 and x_2 in S^*. These are also examples of circuits with *internally switched balanced structure* (ISB-structure) and with *switched balanced structure* (SB-structure) mentioned later.

Now we consider a class of sequential circuits with combinational test generation complexity. Let $T_\alpha(n)$ denote the complexity of the test generation problem for a class α of circuits, where n is a size of a given circuit. Let C denote the class of all combinational circuits. Though it has been known that the test generation problem for class C is NP-complete[2], the complexity for practically encountered instances of the problem was claimed to be only $O(n^3)$[11]. If the test generation problem for a class α of sequential circuits can be reduced to one for class C by some transformation to combinational circuits such that the complexity of the transformation is $O(n^3)$ and it preserves the size of a circuit, then we can say that the class α of sequential circuits has *combinational test generation complexity*. Actually, the complexity of the above extended combinational transformation is $O(n^3)$ and it preserves the size of a given circuit. Therefore, if the test generation problem for a class α can be reduced to one for class C by the extended combinational transformation, the class α has combinational test generation complexity.

To define a new structure called *switched balanced structure* (ISB-structure), we use a topology graph of an RTL circuit and *switched balanced structure* (SB-structure)[5]. A topology graph of an RTL circuit S is a directed graph $G_S = \{V, A\}$ where a set V of nodes consists of clouds, switches, primary inputs and primary outputs, and a set A

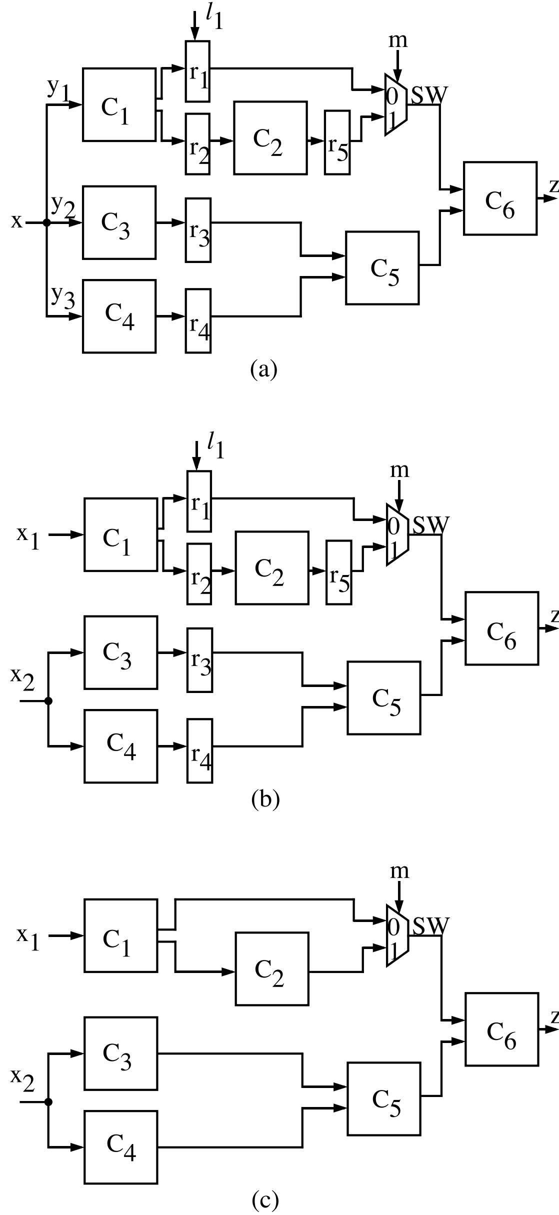

Figure 1. Example of RTL circuits: (a)S(ISB-structure), (b)S^*(SB-structure), (c)$C^*(S)$.

of arcs shows the relation between nodes connected directly or through registers or fanout points. Let $V_{SW} \subseteq V$ denote a set of switches. A set A of arcs are partitioned into three sets A_H of hold registers, A_L of load registers, and A_O of connections without registers. Figures 1(a) and (b) are examples of circuits with ISB-structure and SB-structure, respectively.

Definition 2 (Switched Balanced Structure[6]) *An RTL circuit with topology graph $G_S = \{V, A\}$ is said to be a switched balanced structure if*

1. *G is acyclic,*
2. *For any pair of $u, v \in V$, all directed paths from v to u are of equal depth(the number register arcs) or pass through the same switch node $v_s \in V_{SW}, v_s \neq v$, and*
3. *For any pair of $v, u \in V$, if any directed path from v to u passes through a hold register $h \in A_H$, then all such paths pass through h or all pass through the same switch node $v_s \in V_{SW}$, $v_s \neq v$.*

Definition 3 (Internally Switched Balanced Structure) *An acyclic circuit S is regarded as an internally switched balanced structure (ISB-structure) if a circuit $S^*(S)$ is SB-structure.*

3 Reducibility to Combinational Test Generation Problem

We consider the reducibility of test generation problem of circuits with ISB-structure into combinational test generation problem for each components of the circuits. We consider stuck-at faults at primary inputs and in clouds (combinational logic parts), switches, and registers. For a circuit S with an internally balanced structure, a single stuck-at fault f in S corresponds to the fault f_C in $C^*(S)$ at the same position except the following two cases.

1. A single fault f_S at a primary input x in S corresponds to a multiple fault f_C at primary inputs $x_1, x_2, \cdots$ in $C^*(S)$ if x is separated into $x_1, x_2, \cdots$.
2. Single faults at control inputs of hold registers have no corresponding faults because these lines disappear in $C^*(S)$. We consider this case later.

A multiple stuck-at-fault $\{f_C^1, f_C^2, f_C^3, \cdots\}$ in S corresponds to a multiple stuck-at-fault $\{f_S^1, f_S^2, f_S^3, \cdots\}$ in $C^*(S)$.

First we show a necessary condition to detect faults in a circuit S with ISB-structure.

Example 1 *Consider the circuits in Fig.1. We show an example that a test sequence T for f in S is transformed into a test pattern T_C for f_C in $C^*(S)$. Assume f is in C_5 and a test sequence $T = (x = 010, l_1 = 101, m = 000)$ propagates an error to a primary output z at time 3 in S. All the paths from x_2 to z in S^* have equal sequential depth 1, and hence the value of x at time 2 affects to the value of z at time 3 via C_3 and C_4. Therefore, we assign 1 to x_1 in T_C. Paths from x_1 to z have different sequential depths. However, a switch SW selects an input from a hold register*

r_1, and therefore, we assign the value of m at time 3 to m in T_C. We trace the path with r_1. Since the output value of r_3 at time 3 is loaded at time 1, we assign the value of x at time 1 to x_1 in T_C. We can find $T_C = (x_1 = 0, x_2 = 1, m = 0)$ can obtain the same output of z as T at time 3.

Lemma 1 *Let S be a circuit with ISB-structure. If a fault f at primary inputs, at data inputs/outputs of registers and switches, and in clouds in S is detectable, the corresponding f_C in $C^*(S)$ is detectable.*

Proof sketch: We show that a test sequence T for f in S can be transformed into a test pattern T_C for f_C in $C^*(S)$.

Assume that T propagates an error in S to some primary output z at time t_z. We trace the S^* from z and find when the values affecting the value of z at t_z are applied to each x of primary inputs and control inputs. If an unique time is obtained for x in S^*, we can assign the corresponding value in T to the value of x in T_C.

Because S^* is SB-structure, reconvergent paths in S^* without switch at the reconvergent point have no hold register, and their sequential depths are equal. Starting from z, we find when the values affecting the value of z at t_z are applied to each line as follows. For each cloud, the output value is affected by its input values at the same time. For each switch, the output value is affected by the control value at the same time and the selected input value at that time, since we do not consider faults in switches here and hence it is enough to consider the selected input. For each load register, the output value is affected by its input value at 1 clock cycle before. For each hold register, the output value is affected by its input value loaded lastly. If we encounter a reconvergent point of some paths such that the convergent point is not a switch, we should trace all the paths. In this case, these paths has no hold register and their sequential depths are equal. Therefore, we can find an unique time when the value of their fanout point affects the output value of the reconvergent point. From the above rules, we can find an unique time for each x of primary inputs and control inputs in S^*. ∎

Next, we show an sufficient condition to detect faults in a circuit S with ISB-structure.

Example 2 *We again consider Fig.1, and show an example that a test pattern T_C for f_C in $C^*(S)$ is transformed into a test sequence T for f in S. Assume f_C is in C_5 and a test pattern $T_C = (x_1 = 0, x_2 = 1, m = 0)$ propagates an error to a primary output z. The primary input x in S are separated into two primary inputs x_1 and x_2 in $C^*(S)$. Therefore, we should apply the values of x_1 and x_2 at different times in S. The sequential depth from x_2 to z is fixed in S^* since there is no hold registers between them. Though there are paths with different sequential depths from x_1, they reconverge at a switch and only the value from r_1 is used. In this case, we can adjust the hold register r_1 to hold values for some clock cycles so that the values of x_1 and x_2 are applied to x at different times in S. We can find that a test sequence $T = (x = 01-, l_1 = 10-, m = 000)$ for S can obtain the same output of z at time 3 as T_C.*

Lemma 2 *Let S be a circuit with ISB-structure. If a fault f_C at primary inputs, at data inputs/outputs of registers, and in clouds and switches in $C^*(S)$ is detectable, the corresponding f in S is detectable.*

Proof sketch: We show that a test pattern T_C for f_C in $C^*(S)$ can be transformed into a test sequence T for f in S. Assume that T_C propagates an error to a primary output z. For each x of control inputs and primary inputs that are not separated in S, we can assign the value of x in T_C to the value of x all through the T. We consider the case where a primary input x in S in separated into primary inputs $x_1, x_2, \cdots$ in $C^*(S)$. If there is no hold registers from a primary input x_i to z, all the paths from x_i to z have the equal sequential depths, and hence the time when the value for x_i is applied to x can be determined. Since paths from the separable primary inputs has distinct sequential depths, there are no conflict among these primary inputs. If some path from x_j to z has a hold register, only this path is selected by switches or the path is not selected. If the path is selected, we can adjust the hold register by holding values for any clock cycles so that the value for x_j can be applied to x at different time from other separated primary inputs. ∎

Lemmas 1 and 2 imply the following theorem.

Theorem 3 *A class of sequential circuits with ISB-structure has combinational test generation complexity for faults at primary inputs, at data input/outputs of registers and switches, and in clouds.*

Among faults mentioned in Theorem3, only single faults at primary inputs correspond to multiple faults if the primary inputs are separated. However, our previous work[12] showed that the test generation problem for a multiple fault at some of primary inputs in a combinational circuit can be reduced to the test generation problem for single faults at these primary inputs. Therefore, the test generation problem for single faults mentioned in Theorem3 can be reduced into the test generation problem for single faults in combinational circuits.

Now we consider the other components. For switches, Lemma2 shows a sufficient condition to detect faults in switches, and Lemma1 shows that this condition is also a necessary condition to detect faults at data inputs/outputs of switches. Therefore, we obtained a necessary and sufficient condition to detect faults at data inputs/outputs of switches, and hence for faults equivalent to these faults. However, there are some negative cases for identification of undetectable faults in S as follows.

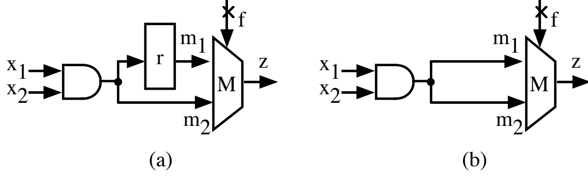

Figure 2. Faults in a switch:(a)S, (b)$C^*(S)$.

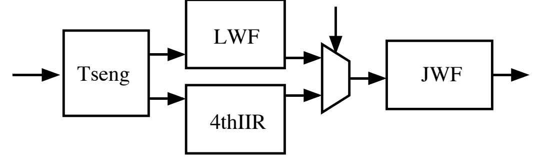

Figure 3. DP4.

Theorem 4 *Let S be a circuit with ISB-structure. Even if some fault f_C in switches is undetectable in $C^*(S)$, this does not always imply the corresponding fault f is undetectable in S.*

Proof: We show a counter-example. Figure2 shows a circuit with ISB-structure. To detect a stuck-at fault at control input of a multiplexor M, different values are needed for both inputs of M. However, we cannot justify the different values at both inputs in $C^*(S)$ while we can justify such values in S. ■

For control inputs of hold registers, we show a sufficient condition to detect the faults.

Theorem 5 *Let r be a hold register in a circuit S with ISB-structure, and let i be a line with some bit width replaced with h in $C^*(S)$. If both stuck-at-0 and stuck-at-1 faults are detectable for some bit b in i, faults at a LOAD ENABLE control input l_r of r are detectable in S.*

Proof sketch: Faults at b in $C^*(S)$ correspond to faults at the corresponding bits b_{in} and b_{out} in the input and the output of h in S. There are test sequences T_0 and T_1 for stuck-at-0 fault and stuck-at-1 fault at b_{in} in S, respectively. The sequences T_0 and T_1 are also a test sequence for stuck-at-0 fault and stuck-at-1 fault at b_{out}, respectively.

1. Stuck-at-0 fault at l_r
   The hold register r always operates in HOLD mode, and therefore, the value of r is always its initial value. This can be considered stuck-at faults at the output of r. Therefore, we can detect the faults by T_0 and T_1.

2. Stuck-at-1 fault at l_r
   First, we apply T_0. A test sequence T_0 can activates a stuck-at-0 fault at b_{in} and loads the error in r at some time t and holds the error for c (≥ 0) clock cycles in r. The error is propagated at b_{out} at time $t + 1 + c$. The value at b_{in} at time t should be 1 to activate a stuck-at-0 fault. When considering the stuck-at-1 fault at l_r, if the value at b_{in} at time $t+c$ is 0, an error $\bar{D}$ appears at b_{out} at time $t + c + 1$. T_0 can propagates this error to some primary output.

   If the value at b_{in} at time $t+c$ is 1, we apply T_1 and T_0 in this order but holding the value of r when T_1 activates a stuck-at-1 fault at b_{in} until when T_0 propagates an error to b_{out} (the $t + c + 1$th clock in T_0). Let t_1 be the length of T_1. In a correct circuit, the value of b_{out} is 0 at $t_1 + t + c + 1$, while this value is 1 in a faulty circuit. That is, an error D is propagated to b_{out} and T_0 can propagate this error to some primary output. ■

Table 1. Circuit characteristics

circuit	|bit|	#PI	#PO	#hold	#load	#gate
DP4	16	320	304	15	12	24381
ISB-RISC	32	1088	1152	7	12	70248

Table 3. Faults in hold registers

circuits	#faults	#detected($C^*(S)$)	#redundant(S)
DP4	30	28	2
ISB-RISC	14	14	–

4 Experiments

We made experiments to evaluate (1)the effectiveness of using combinational ATPG to generate tests for circuits with ISB-structure, and (2)fault coverage for faults in switches and registers where we only show sufficient conditions to detect faults. We used two circuits $DP4$ and ISB-$RISC$ where $DP4$ is obtained by connecting 4 benchmark circuits Tseng, 4thIIR, LWF and JWF like Fig.3, and ISB-$RISC$ is obtained from a RISC circuit. We replaced some FFs with scan FFs to make them ISB-structure. Table 1 shows the characteristics of these circuits. The columns |bit|, #PI, #PO, #hold, #load and #gate show the bit width, the numbers of primary inputs, primary outputs, hold registers, load registers and gates, respectively. We used TestGen (Synopsys) as both combinational and sequential ATPG on Sun Blade 1000.

Table 2 shows the results on test generation for sequential circuits S using sequential ATPG and for combinational circuits $C^*(S)$ using combinational ATPG. We show the test generation time (CPU), the numbers of faults

Table 2. Test generation results

circuit		CPU(s)	#faults	#detected		#redundant			#abort
				$C^*(S)$	S	$C^*(S)$	S		
							#redundant*	#abort*	
DP4	S	18476.9	30590		27404		361		2825
	$C^*(S)$	1.6	28640	25517	27461	3123	3115	14	0
ISB-RISC	S	38251.2	120140		118984		272		884
	$C^*(S)$	1952.4	119358	119037	119789	235	137	128	86

Table 4. Faults in switches

circuits		#faults	#detected	#redundant	#abort
DP4	S	9214	9178	36	0
	$C^*(S)$	9214	9178	36	0
ISB-RISC	S	38976	38756	207	13
	$C^*(S)$	38976	38756	220	0

(#fault), detected faults(#detected), identified redundant faults(#redundant), and aborted faults (#abort). For $C^*(S)$, we also show the numbers of faults in S obtained from the results on $C^*(S)$. In this case, #redundant* means the number of redundant faults identified by Lemma1 and their equivalent faults, and #abort* means the number of faults that we cannot identify to be detectable or not by Lemma1 or Lemma2. We obtained higher fault coverage and fault efficiency for both $DP4$ and $ISB\text{-}RISC$ using $C^*(S)$ with smaller test generation time than when we apply sequential ATPG to S.

Table 3 shows the results on faults at control inputs of hold registers. The columns #faults, #detected($C^*(S)$), #redundant(S) denote the number of faults, the number of detected faults from the results on $C^*(S)$ by Theorem5, and the number of redundant faults identified in S. In these two cases, test sequences are generated for all detectable faults by test generation using $C^*(S)$. Table 4 shows the results on faults in switches. We counted detectable faults in $C^*(S)$ by Lemma 2 and identified redundant faults in $C^*(S)$ by Lemma 1 for data inputs/outputs and their equivalent faults. We found that all the faults in switches are identified to be detectable or not by test generation using $C^*(S)$ while sequential ATPG aborted to generate test for some faults in S for $ISB\text{-}RISC$.

5 Conclusion

We proposed a new structure *internally switched balanced structure* (ISB-structure) as structure of sequential circuits with combinational test generation complexity. The proposed structure properly includes *balanced structure*, *internally balanced structure*, *switched balanced structure* proposed previously. As a result, we can generate tests efficiently using combinational ATPG for larger class of sequential circuits. Moreover, we consider the faults in switches and hold registers where we treat them as macros, while other related works ignored faults inside these macros. Experimental results showed that we can generate tests more efficiently using the transformed combinational circuits than using the original sequential circuits.

In this work, we assumed that control signals to switches and hold registers are derived from the outside of the circuits. One of future works to consider circuits where such control signals are generated inside the circuits.

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