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A Path Delay Test Generation Method for Sequential Circuits Based on Reducibility to Combinational Test Generation

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Abstract *In this paper, we present a new structure, called* discontinuous reconvergence structure (DR-structure), *of sequential circuits. We show that the path delay fault test generation problem for sequential circuits with DR-structure can be reduced to the segment delay fault test generation problem for their time-expansion models, which are combinational circuits. We propose a test generation method for path delay faults in sequential circuits with DR-structure based on the reducibility, and show the effectiveness of the method by a case study.*

Keywords *path delay fault, test generation, discontinuous reconvergence structure, time-expansion model, partially enhanced scan design*

1 Introduction

With the increasing speed and complexity of VLSI circuits, tests targeted only for stuck-at faults are insufficient to guarantee the proper circuit operation. Delay testing is necessary to reach the acceptable quality level. Until now, several delay fault models have been investigated [9]. The path delay fault model [11] is one of the most general models among them because distributed faults along paths can be tested and the delay size of detectable faults is scalable.

In general, test generation for sequential circuits under simple fault models such as the single stuck-at fault model is itself a hard task. Path delay test generation for sequential circuits is an even more challenging problem even if a small number of paths to be tested is selected by several path selection techniques [9]. For such sequential circuits, *design for testability (DFT)* is an important approach to reduce the test generation effort. Given a sequential circuit, a fully enhanced scan technique [4] replaces each flip-flop (FF) by an *enhanced scan FF (ESFF)*. An ESFF can store two bits to apply two consecutive vectors. For a sequential circuit designed by this technique, we can use a combinational path delay fault test generation algorithm (*ATPG*) to generate test sequences. Therefore, high fault coverage can be achieved with short test generation time. However, this technique has disadvantage that hardware overhead caused by extra memory elements of ESFFs is very high. This disadvantage can be alleviated by using partial scan techniques [1, 10]. In a partially enhanced scan technique [1], for a sequential circuit, ESFFs are selected such that feedback paths in the circuit are broken if these ESFFs are removed. For a sequential circuit designed by this partial scan technique, we can consider the circuit to be a feedback free circuit during test generation, and test generation of the feedback free circuit is easier than that of the original one. However, there is room for facilitating test generation because it still requires a sequential path delay fault ATPG. We have proposed a partially enhanced scan design method [10]. The method is based on *balanced structure* [5]. The class of acyclic sequential circuits properly includes that of balanced sequential circuits. We showed that test sequences for path delay faults in balanced sequential circuits can be generated by applying a combinational segment delay fault ATPG to their combinationally equivalent circuits. Our previous method can ease path delay test generation complexity at the cost of a large number of ESFFs compared with the method [1]. In this paper, we discuss an extended class of sequential circuits for which test sequences can be generated by a combinational delay fault ATPG.

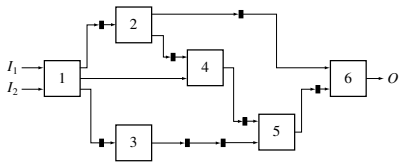
This paper presents a new structure of sequential circuits called *discontinuous reconvergence structure (DR-structure)*. The relation among three classes of sequential circuits are as follows: {the class of acyclic sequential circuits} $\supset$ {the class of sequential circuit with DR-structure} $\supset$ {the class of balanced sequential circuits}. The DR-structure has a property of easy testability for path delay faults: test sequences for path delay faults in sequential circuits with DR-structure can be generated by applying a combinational segment delay fault ATPG to their *time-expansion models* [7]. We propose a method of path delay test generation for sequential circuits with DR-structure, and show reducibility of test generation for path delay faults in a sequential circuit with DR-structure to that for the corresponding segment delay faults in its time-expansion model. It is confirmed the following by a case study: for sequential circuits with DR-structure, we can reduce the test generation time and can enhance the fault efficiency by using our method instead of an ordinary method using a sequential path delay fault ATPG. In order to apply the proposed method to general sequential circuits, we use a partially enhanced scan design technique to extract DR-structure from the circuits. Theoretically, DR-structure can be extracted from the circuits with low hardware overhead compared to balanced structure. In this paper, we also confirm it by the study.

2 Preliminaries

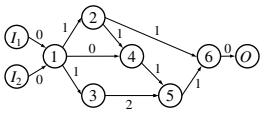
A sequential circuit consists of combinational logic blocks (CLBs) connected with each other directly or through FFs. A CLB in the circuit is a region of connected combinational logic. The circuit can be modeled by a weighted directed graph defined as follows.

Definition 1 A *topology graph* for a sequential circuit S is a weighted directed graph $G = (V, A, w)$.

- V is the set of vertices representing primary inputs, primary outputs and CLBs in S.



(a) Sequential circuit S.



(b) Topology graph of S: G.

Figure 1. Sequential circuit and its topology graph.

- $A \subset V \times V$ is the set of arcs representing FFs and wires in S.
- $w : A \mapsto \{0\} \cup N$ defines the weights of the arcs, and $w(u,v)$ $(u,v \in V)$ denotes the number of FFs on a connection $(u,v) \in A$, where N is the set of natural numbers. □

Example 1 An example of a sequential circuit and its topology graph are shown in Figure 1. In Figure 1(a), $1,2,\ldots,6$ are CLBs, and black blocks are FFs. □

In this paper, we assume that FFs have no hold capability, and those are of D-type. This assumption does not impose restriction on circuit representation because any FF with hold capability or the other types of FFs can be modeled by a D-type FF and some logic gates.

2.1 Delay Fault Model

Path Delay Fault Model In a sequential circuit, a path is defined as an ordered set of gates $(g_0, g_1, \ldots, g_n)$, where g_0 is a primary input or an FF and g_n is a primary output or an FF, and gate g_i is an input to gate g_{i+1} $(1 \leq i \leq n-1)$. A path has a delay fault if propagation time of rising or falling transition through the path exceeds a specified clock period. Such a delay fault on a path is said to be a *path delay fault (PDF)* [11]. PDFs can be classified into four categories by the off-input conditions: (1) *robust testable*, (2) *non-robust testable*, (3) *functional sensitizable* and (4) *functional unsensitizable* [3, 9]. The robust, non-robust and functional sensitizable PDFs can affect the performance of the circuit, and they are together called *functional irredundant faults*. Functional unsensitizable PDFs, also called *functional redundant faults*, never independently determine the performance, and they do not have to be tested. In this paper, in order to simplify the discussion, we do not distinguish (1), (2) and (3).

Definition 2 Let S and p be a sequential circuit and a path in S, respectively. Let f and S_f be the PDF on p and the faulty circuit of S with f, respectively. Let C be the combinational circuit composed of all the CLBs on p, and let t be a specified clock period of S. In a *slow-fast-slow testing*[1] [9], f is *testable* if there exists an input sequence T for S and S_f such that the following conditions hold.

1. By applying an input vector pair (v_1, v_2) to each input of C, the desired transition is launched at the starting point of p, and the transition is propagated to the ending point of p along p. Then, the value induced by v_2 at the ending point in S_f is different from that in S at time t.
2. By applying T to S_f, (v_1, v_2) is justified to each input of C, and the fault effect of f at the ending point is propagated to a primary output.

Such an input sequence T is regarded as a *test sequence* for f. □

Segment Delay Fault Model In a combinational circuit, a segment is defined as an ordered set of gates $(g_1, g_2, \ldots, g_L)$, where L is the length of the segment, and gate g_i is an input to gate g_{i+1} $(1 \leq i \leq L-1)$. The length of the segment L can be anywhere from one to the number of gates in the longest path in the circuit. A segment has a delay fault if propagation time of rising or falling transition through the segment exceeds a specified limit. Such a delay fault on a segment is said to be a *segment delay fault (SDF)* [6]. It is assumed that a segment delay fault is large enough to cause a delay fault on all paths that include the segment.

Definition 3 Let C and s be a combinational circuit and a segment in C, respectively. Let f and C_f be the SDF on s and the faulty circuit of C with f, respectively. Let t be a specified limit time. The fault f is *testable* if there exists an input vector pair (v_1, v_2) for C and C_f such that the following conditions hold.

1. By applying (v_1, v_2) to the circuits, the desired transition at the starting point of s is launched, and the transition is propagated to the ending point of s along s. Then, the value induced by v_2 at the ending point in C_f is different from that in C at time t.
2. The fault effect of f at the ending point is propagated to a primary output by applying (v_1, v_2) to C_f.

Such an input vector pair (v_1, v_2) is regarded as an *two-pattern test* for f. □

Notice that it is conceivable that categories of SDFs are the same as those of PDFs.

2.2 Circuit Transformation

In our test generation method, test sequences for path delay faults in sequential circuits with DR-structure are generated by applying a combinational ATPG to their *time-expansion models* [7]. A time-expansion model for an acyclic sequential circuit is defined based on the following *time-expansion graph* [7].

Definition 4 Let S be an acyclic sequential circuit, and let $G = (V, A, w)$ be the topology graph of S. Let $E = (V_E, A_E, t, l)$ be a directed graph, where V_E is the set of vertices, A_E is the set of arcs, t is a mapping from V_E to the set of integers, and l is a mapping from V_E to V. If E satisfies the following four conditions, E is said to be a *time-expansion graph (TEG)* of G [7].

C1 (CLB preservation) The mapping l is surjective, i.e., $\forall v \in V, \exists u \in V_E$ s.t. $v = l(u)$.

[1] In this paper, we assume a slow-fast-slow testing strategy in test application because a sequential circuit can be considered delay fault-free in both the fault initialization and the fault effect propagation phases.

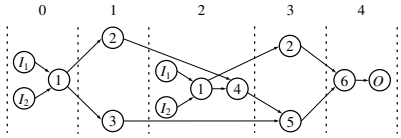


Figure 2. Time-expansion graph of G: E.

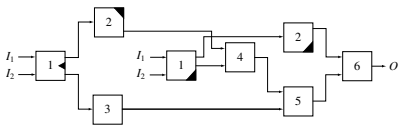


Figure 3. Time-expansion model of S based on E: $C_E(S)$.

C2 (Input preservation) Let u be a vertex in E. For any direct predecessor of u in G, $v \in pre(l(u))$, there exists a vertex u' in E such that $u' \in pre(u)$ and $l(u') = v$, where $pre(x)$ is the set of direct predecessors of a vertex x.

C3 (Time consistency) For any arc $(u,v) \in A_E$, there exists an arc $(l(u),l(v)) \in A$ such that $t(v) - t(u) = w(l(u),l(v))$.

C4 (Time uniqueness) For any vertices $u,v \in V_E$, if $t(u) = t(v)$ and $l(u) = l(v)$, then the vertices u and v are identical, i.e., $u = v$. □

Example 2 Figure 2 shows the TEG of S (Figure 1(a)). In Figure 2, the character denoted in a vertex is that of the corresponding vertex in G, and the number located at the top of each column denotes the value of the label of vertices in the column. The graph E satisfies all the conditions in Definition 4. □

Note that a TEG of an acyclic sequential circuit is unique if the circuit is a single-output acyclic sequential circuit [7].

Definition 5 Let S be an acyclic sequential circuit, and let $G = (V,A,w)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$ be a TEG of G. The combinational circuit $C_E(S)$ obtained by the following procedure is said to be the *time-expansion model (TEM)* of S based on E [7].

1. For each vertex $u \in V_E$, let $l(u) \in V$ be the CLB corresponding to u.
2. For each arc $(u,v) \in A_E$, connect the output of u to the input of v with a wire in the same way as $(l(u),l(v)) \in A$. Note that the connection corresponding to (u,v) has no FF even if the connection corresponding to $(l(u),l(v))$ has some FFs (i.e., $w(l(u),l(v)) \neq 0$).
3. In each CLB, lines and logic gates that are reachable to neither other CLBs nor primary outputs are removed.□

Example 3 Figure 3 shows the TEM of S (Figure 1(a)) based on E (Figure 2). In Figure 3, a highlighted part in a CLB represents a portion of the lines and gates removed by Step 3 in Definition 5. □

3 Discontinuous Reconvergence Structure

Our test generation method proposed in Section 4 generate a test set for path delay faults in sequential circuits with *discontinuous reconvergence structure*. We define the structure as follows.

Definition 6 Let $G = (V,A,w)$ be the topology graph of an acyclic sequential circuit S, and let $P(u,v)$ be the set of paths from u to v ($u,v \in V$). Let $n(p)$ ($p \in P(u,v)$) be the number of FFs on the path p. The circuit S is said to be a *discontinuous reconvergence structure (DR-structure)* if it satisfies the following condition.

$$|n(p_i) - n(p_j)| \neq 1 \quad (\forall u,v \in V, \forall p_i,p_j \in P(u,v)) \quad \square$$

Example 4 An acyclic sequential circuit S (Figure 1(a)) satisfies Definition 6. Therefore, S is a sequential circuit with DR-structure. □

Notice that, from Definition 6, the class of sequential circuits with DR-structure properly includes that of balanced sequential circuits [5, 10].

4 Test Generation

4.1 Test Generation Method

Given a sequential circuit with DR-structure, S, our test generation method proceeds as follows.

For each output cone circuit S_c of S,

1. Make a PDF list F of S_c.
2. Construct the topology graph G of S_c.
3. Create the TEG E of G.
4. Construct the TEM $C_E(S_c)$ of S_c based on E.
   For each PDF $f \in F$,
   (a) For $C_E(S_c)$, obtain the set of SDFs corresponding to f, and generate a two-pattern test t_e for an SDF f_e in the set by using a combinational ATPG[2].
   (b) Transform t_e into a test sequence T for f in S_c.
   (c) Transform T into a test sequence T' for f in S.

Note that this test generation scheme can be applied to the other delay fault models, e.g., the transition fault model, etc.

Here, we define the *fault transformation* in Step 4 (a) of the above procedure as follows.

Definition 7 Let S be an acyclic sequential circuit, and let $G = (V,A,w)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$ be a TEG of G, and let $C_E(S)$ be the TEM of S based on E. Let f be the PDF on a path p in S, and let C be the combinational circuit composed of all the CLBs on p in S. Let B be the set of the combinational circuits corresponding to C in $C_E(S)$, and let B' the subset of B whose the input (output) corresponding to the starting (ending) point of p in $C_E(S)$ does not removed. A transformation such that $B' = \mu(C)$ is said to be the *sub-circuit transformation*[3]. Let s in each $b' \in B'$ be the segment corresponding to p, and let F_E be the set of SDFs composed of all the s. A transformation such that $F_E = \sigma(f)$ is said to be the *fault transformation*[4]. □

Example 5 Figure 4 illustrates the fault transformation. In general, a path delay fault in S corresponds to one or more segment delay faults in $C_E(S)$. Notice that, from Definition 4, there exists at least one segment delay fault corresponding to a path delay fault even though lines or logic gates in $C_E(S)$ are removed by Step 3 in Definition 5. □

Next, we define the *sequence transformation* in Step 4 (b) of the above procedure as follows.

Definition 8 Let S be an acyclic sequential circuit, and let $G = (V,A,w)$ be the topology graph of S. Let $E = (V_E,A_E,t,l)$ be a TEG of G, and let $C_E(S)$ be the TEM of S based on E. Let $t_{\min}$ be the minimum value of labels assigned to vertices in E, and let d be the sequential depth of

[2] If all the SDFs corresponding to f are identified as redundant faults by a combinational ATPG, f is also a redundant fault.

[3] Transforming $b' \in B'$ into C is denoted as μ^{-1}.

[4] Transforming $f_e \in F_E$ into f is denoted as σ^{-1}.

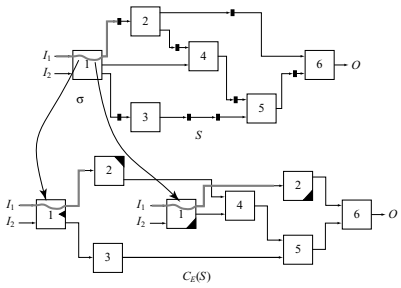


Figure 4. Fault transformation σ.

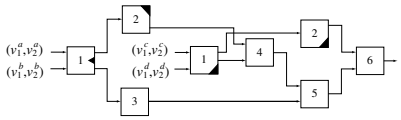


Figure 5. Input vector pairs.

S. Let $I_u = (v_1, v_2)$ be an input vector pair to each primary input $u \in V_E$ in $C_E(S)$. A procedure transforming I_u into the input pattern to the primary input $l(u) \in V$ of S at time k $(0 \leq k \leq d+1)$ is said to be the *sequence transformation* τ. That is, for each u,

$$I_{l(u)}(k) = \begin{cases} v_1 & \text{if } k = t(u) - t_{\min} \\ v_2 & \text{if } k = t(u) - t_{\min} + 1 \\ \textit{don't care} & \text{otherwise.} \end{cases}$$

Such an input sequence with the length $d+2$ is regarded as a *two-pattern sequence*. □

Example 6 Input vector pairs in Figure 5 are transformed into the two-pattern sequences in Table 1 by the sequence transformation τ. In Table 1, X denotes *don't care* value. □

In Step 4 (c) of the test generation procedure, T is transformed into T' by applying T to the primary inputs of S corresponding to the primary inputs of S_c. Note that the other primary inputs of S are assigned *don't care* values, i.e., each *don't care* value of T' is placed by 0 or 1.

4.2 Proof of Correctness

In this subsection, we discuss the correctness of our test generation method. In the following discussion, all the proofs of lemmas are omitted due to limitations of space. However, Lemma 1, 2 and 3 can be easily proved from Definition 4 and 6, Definition 2 and 4, and Definition 4 and Lemma 1, respectively.

Lemma 1 Let S be a single-output acyclic sequential circuit, and let $G = (V, A, w)$ be the topology graph of S. Let $E = (V_E, A_E, t, l)$ be the TEG of G. If S is a sequential circuit with DR-structure, S satisfies the following condition.

$$|t(u) - t(v)| \neq 1 \quad (\forall u, v \in V_E \text{ s.t. } l(u) = l(v)) \qquad \square$$

Lemma 1 guarantees that a two-pattern test t_e is transformed into a test sequence T without conflict of patterns in Step 4 (b) of our test generation method. Notice that, from Lemma 1, if a structure of a sequential circuit is not DR-structure but acyclic structure, conflict of patterns must occur in the sequence transformation. Hence, test generation for such a sequential circuit must be performed by using a sequential path delay ATPG.

Lemma 2 Let S^{DR} be a sequential circuit with DR-structure, and let f be any PDF in S^{DR}. If f is testable, there exists a test sequence formed as a two-pattern sequence. □

Table 1. Two-pattern sequences.

Primary input	Time					
	0	1	2	3	4	5
I_1	v_1^a	v_2^a	v_1^c	v_2^c	X	X
I_2	v_1^b	v_2^b	v_1^d	v_2^d	X	X

Lemma 3 Let S^{DR} be a single-output sequential circuit with DR-structure, and let $G = (V, A, w)$ be the topology graph of S^{DR}. Let $E = (V_E, A_E, t, l)$ be the TEG of G, and let $C_E(S^{DR})$ be the TEM of S based on E. Let $t_{\min}$ be the minimum value of labels assigned to vertices in E, and let d be the sequential depth of S^{DR}. Let $I_C = (v_1, v_2)$ be an arbitrary input vector pair to S^{DR}, and let $\tau(I_C)$ be the two-pattern sequence. Then, the value O_u observed from a primary output $u \in V_E$ by applying v_2 to $C_E(S^{DR})$ is equal to the value $O_{l(u)}(t(u) - t_{\min} + 1)$ observed from the primary output $l(u) \in V$ at time $t(u) - t_{\min} + 1$ by applying $\tau(I_C)$ to S^{DR}. □

From Lemma 1–3, we can have the following theorem.

Theorem 1 Let S^{DR} be a single-output sequential circuit with DR-structure, and let $G = (V, A, w)$ be the topology graph of S^{DR}. Let $E = (V_E, A_E, t, l)$ be the TEG of G, and let $C_E(S^{DR})$ be the TEM of S^{DR} based on E. Let F be the set of all PDFs in S^{DR}. Then,

1. a PDF $f \in F$ is testable if and only if at least one SDF $f_e \in \sigma(f)$ is testable, and
2. a two-pattern test for the SDF $f_e \in \sigma(f)$ can be transformed into a test sequence for the PDF $f = \sigma^{-1}(f_e)$.

(Proof) Let S_f^{DR} be the faulty circuit with $f \in F$ on a path p of S^{DR}, and let $C_{E_{f_e}}(S^{DR})$ be the faulty circuit with $f_e \in \sigma(f)$ of $C_E(S^{DR})$. Let C be the combinational circuit composed of all the CLBs on p, and let $t_{\min}$ be the minimum value of labels assigned to vertices in E. Let d be the sequential depth of S^{DR}, and let τ^{-1} be the inverse transformation of τ.

First, we show that if f is testable, at least one $f_e \in \sigma(f)$ is also testable. From Lemma 2, there exists a two-pattern sequence T_f if f is testable. From Definition 2, if f is testable, a vector pair (v_1, v_2) is justified to C at time i and $i+1$ by applying T_f, respectively. Let C' be the combinational circuit composed of CLBs such that $t(c) = i + t_{\min}$ in $\mu(C)$, where c is a CLB in $\mu(C)$. From Definition 4 and Lemma 3, when we apply $\tau^{-1}(T_f)$ to $C_{E_{f_e}}(S^{DR})$, (v_1, v_2) is justified to C'. From Definition 4, since a logic function of the combinational circuit on p with f and that on s with f_e are identical, the value appeared from the ending point of s by applying the 2nd vector of $\tau^{-1}(T_f)$ to $C_{E_{f_e}}(S^{DR})$ is equal to the value appeared from the ending point of p at time $i+1$ by applying T_f to S_f^{DR}. From the above discussion and Lemma 3, in a slow-fast-slow testing, the value observed from a primary output $u \in V_E$ by applying the 2nd vector of $\tau^{-1}(T_f)$ to $C_{E_{f_e}}(S^{DR})$ is equal to the value observed from the primary output $l(u) \in V$ at time $t(u) - t_{\min} + 1$ by applying T_f to S_f^{DR}. $C_{E_{f_e}}(S^{DR})$ and the TEM $C_E(S_f^{DR})$ of S_f^{DR} based on E are isomorphic because f_e is an SDF on s corresponding to p. Therefore, the output response of $C_E(S_f^{DR})$

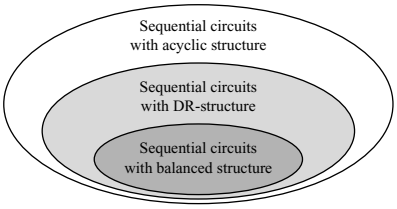


Figure 6. Classification of sequential circuits by structure.

by applying the 2nd vector of $\tau^{-1}(T_f)$ are different from that of $C_E(S^{DR})$ by applying the 2nd vector of $\tau^{-1}(T_f)$. Hence, if f is testable, at least one $f_e \in \sigma(f)$ is also testable.

Next, we show that if f_e is testable, $f = \sigma^{-1}(f_e)$ is also testable. If f_e is testable, there exists a two-pattern test t_{f_e}. Let s' and $C_{s'}$ be the segment with f_e and the combinational circuit composed of all the CLBs on s', respectively. Let $t_{s'}$ be the label of CLBs in $C_{s'}$, and let (v'_1, v'_2) be a vector pair to $C_{s'}$. From Definition 4 and Lemma 3, we can justify (v'_1, v'_2) to $\mu^{-1}(C_{s'})$ in S_f^{DR}. From Definition 4, since a logic function of the combinational circuit on s' and that on the path p' corresponding to s' are identical, the value appeared from the ending point of s' by applying the 2nd vector of t_{f_e} to $C_{E_{f_e}}(S^{DR})$ is equal to the value appeared from that of p' by applying $\tau(t_{f_e})$ to S_f^{DR} at time $t_{s'} - t_{\min} + 1$. From the above discussion and Lemma 3, the value observed from a primary output $u' \in V_E$ by applying the 2nd vector of t_{f_e} to $C_{E_{f_e}}(S^{DR})$ is equal to the value observed from the primary output $l(u') \in V$ at time $t(u') - t_{\min} + 1$ by applying $\tau(t_{f_e})$ to S_f^{DR} in a slow-fast-slow testing. By the same reason as previously, $C_{E_{f_e}}(S^{DR})$ and the TEM $C_E(S_f^{DR})$ of S_f^{DR} based on E are isomorphic. Therefore, when $\tau(t_{f_e})$ is applied, the output response of S^{DR} and the output response of S_f^{DR} are different. Hence, if f_e is testable, $f = \sigma^{-1}(f_e)$ is also testable.

Finally, from Lemma 1, any two-pattern test for f_e can be transformed into a test sequence for $f = \sigma^{-1}(f_e)$ by the sequence transformation τ. Thus, the theorem is proved. □

From this theorem, we see that our test generation method can not only generate test sequences for all the testable PDFs in sequential circuits with DR-structure, but also identify all the untestable PDFs in the circuits.

5 Advantage of the Test Generation Method

5.1 Characteristics of This Work and Previous Works

From Definition 6, we can see the relation among acyclic structure, balanced structure and DR-structure shown in Figure 6. In general, a sequential circuit is classified as none of these circuit structures. Therefore, if we generate test sequences for path delay faults in the sequential circuit by using the method [1], [10] or our method , we need to extract respective circuit structures by using DFT techniques, e.g., partially enhanced scan techniques. In the following discussion, we suppose that partially enhanced scan techniques are used to extract respective circuit structures.

Table 2. Comparison of the number of ESFFs.

Circuit name	#FF	Acyclic structure		DR-structure		Balanced structure	
		#ESFF	Scan (%)	#ESFF	Scan (%)	#ESFF	Scan (%)
s5378	179	30	16.8	92	51.4	106	59.2

Here, we discuss the test generation complexity for each class of sequential circuits and the hardware overhead (the number of ESFFs) required for extracting each structure by partially enhanced scan techniques.

Acyclic structure: The hardware overhead for making a general sequential circuit acyclic is lowest among these three structures. However, given an acyclic sequential circuit, the test generation is more complex than the others because a sequential path delay fault ATPG is required for generating test sequences.

Balanced structure: In the test generation method [10], given a balanced sequential circuit, test sequences for path delay faults in the circuit are generated by applying a combinational segment delay fault ATPG to its combinationally equivalent circuit. The combinationally equivalent circuit is obtained by just replacing each FF with a wire, and the sizes of the original circuit and the transformed circuit are equal except for FFs. Therefore, the test generation is much easier than the ordinary test generation using a sequential path delay fault ATPG. However, the hardware overhead is highest among these three structures.

DR-structure: The hardware overhead is lower than that of balanced structure. Furthermore, we can also generate test sequences for path delay faults in a sequential circuit with DR-structure by applying a combinational segment delay fault ATPG to its time-expansion model. Therefore, the test generation can be much easier than the ordinary test generation using a sequential path delay fault ATPG. However, when the circuit is transformed into a time-expansion model, some combinational logic blocks may be duplicated. In worst case, the size of the time-expansion model can be $\lceil d/2 \rceil$ times as large as that of the original circuit, where d is the sequential depth of the original circuit. In the next subsection, we examine the increase rate between the size of a sequential circuit with DR-structure and that of its time-expansion model, and evaluate the effectiveness of our test generation method.

5.2 Case Study

In this case study, we evaluate the effectiveness of the proposed method in the hardware overhead required for extracting DR-structure, the test generation time and the fault efficiency. The following experiment was performed on a Sun Blade 1000 workstation, and we used a combinational/sequential delay test generation tool TestGen (Synopsys) on the workstation. Note that we considered a fault model in test generation as the transition fault model because a combinational ATPG for segment delay faults was not available. However, our test generation method can be applied to fault models which can be tested by two-pattern tests. Therefore, the transition fault model can be also dealt with.

First, we compare the hardware overheads required for extracting acyclic structure, balanced structure and DR-structure from a sequential circuit. We used a circuit, s5378, of the ISCAS '89 benchmark set. Table 2 shows the hardware overheads required for extracting respective structures.

Table 3. Test generation result for s5378: Acyclic structure vs. DR-structure.

Sequential ATPG (acyclic structure)		Combinational ATPG (DR-structure)	
TGT (sec)	FE (%)	TGT (sec)	FE (%)
3721.58	99.07	352.78	100.00

Column "#FF" denotes the number of FFs in the original circuit. Columns "#ESFF" and "Scan (%)" in each column of circuit structure denote the number of ESFFs and the percentage of ESFFs in each structure, respectively. Note that we obtained s5378 with acyclic structure, S^A, by the exact algorithm [2], and s5378 with DR-structure, S^{DR}, and s5378 with balanced structure, S^B, were extracted by applying a greedy algorithm to S^A. Here, let us explain the greedy algorithm for S^{DR} briefly. The greedy algorithm traverse S^A from the primary inputs of S^A to the primary outputs of S^A by a depth-first fashion. In traversing S^A, if paths of S^A do not satisfy the condition of Definition 6, an FF on the paths is replaced by an ESFF in order for the paths to satisfy the condition. Thus, we obtained S^{DR} from S^A. S^B was obtained in a similar way. The time for extracting each structure was negligibly short. In Table 2, "Scan" of S^{DR} was larger than that of S^A. However, "Scan" of S^{DR} was the value of -7.8% compared to that of S^B. Thus, DR-structure can be obtained from a sequential circuit by paying low hardware overhead compared to balanced structure.

Next, we evaluate test generation time and fault efficiency for S^A and S^{DR}. In our method, test generation was performed for each output cone of S^{DR}, and when a fault was shared by some output cones, we only generated a test sequence for the fault in an output cone, i.e., when the fault was detected in an output cone, we removed the fault from the fault list of S^{DR}. In Table 3, column "Sequential ATPG" denotes the test generation result using a sequential ATPG for S^A, and column "Combinational ATPG" denotes the result using a combinational ATPG for the time-expansion model of S^{DR}. Columns "TGT (sec)" and "FE(%)" denote test generation time and fault efficiency under the non-robust criteria for transition faults, respectively. In the output cones of S^{DR}, the maximum percentage of increase between each output cone and its time-expansion model was about $+9.1\%$[5]. Despite increasing the circuit size, our method achieved 100% fault efficiency with very short test generation time compared to the conventional method using a sequential ATPG. Thus, our method can significantly improve the test generation time and the fault efficiency by paying large hardware overhead compared to acyclic structure.

We cannot show more results for the other benchmark circuits because part of procedures in the method is still not automated. However, from the above study, we can see that our method is effective in the hardware overhead, the test generation time and the fault efficiency.

6 Conclusions

This paper presented a new structure, called discontinuous reconvergence structure (DR-structure), of sequential circuits with easy testability for path delay faults. We proposed a path delay test generation method for sequential circuits with the structure. In our method, instead of a sequential path delay fault test generation algorithm, a combinational segment delay fault test generation algorithm is used to generate test sequences for path delay faults. We theoretically proved the correctness of the proposed method. Our method can be used not only path delay faults, but also the other delay fault models which can be detected by two-pattern tests, e.g., segment delay faults, transition faults, and so on. We confirmed that our test generation method can reduce test generation time and can enhance fault efficiency compared to the ordinary test generation method using a sequential delay fault test generation algorithm. To apply our method to general sequential circuits, we used a partially enhanced scan design to extract DR-structure from the circuits. Theoretically, the class of sequential circuits with DR-structure properly includes that of balanced sequential circuits. Therefore, it is conceivable that the number of enhanced scan FFs required for extracting DR-structure from a sequential circuit is smaller than that required for extracting balanced structure (our previous work [10]). By the case study, we confirmed that the hardware overhead for our method can be reduced compared with that for our previous method.

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[5] The sequential depth of S^{DR} was four.

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