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*Scott Davidson;*
*scott.davidson@eng.sun.com*

# Needed: Third-generation ATPG benchmarks

In 1983 I published the FAN algorithm, and by using actual combinational circuits, showed its superiority over both the D-algorithm (by J.P. Roth) and the PODEM algorithm (by P. Goel). In 1984 I discussed ATPG (automatic test pattern generation) benchmarking with Franc Brglez (then with Bell Northern Research and now with North Carolina State University) while I was on sabbatical visiting Vinod Agarwal at McGill University.

Before this, we had no benchmarks for ATPG algorithms. Brglez and I agreed that benchmark circuits helped advance ATPG algorithm research and development. We organized a special session on combinational ATPG benchmarking at ISCAS 85 (the 1985 International Symposium on Circuits and Systems) in Kyoto, Japan. With the cooperation of many people from industry and universities in the USA, Canada, Europe, and Japan, we collected excellent benchmarks with various and useful characteristics.

Later, others reported many better, more-efficient ATPG algorithms for combinational circuits. The widespread availability of these benchmarks drove the development of new algorithms, as researchers strove to generate the best-known results in terms of runtime, vector length, and fault coverage.

Many people involved with ATPG research and development wanted another set of benchmarks for sequential ATPG algorithms, which were at this point fairly primitive. In fact, many people did not believe in the feasibility of sequential ATPG. A special session on sequential ATPG benchmarking at ISCAS 89 in Portland, Oregon, presented two algorithms. Both algorithms achieved good results on the benchmark sequential circuits without DFT, which validated the utility of research in this area. Thanks to the ISCAS 89 benchmarks, we experienced a great acceleration in sequential ATPG research. This success in industry and academia led to the founding of companies selling sequential ATPGs. This segment of the CAD industry expanded from just one company before ISCAS 89 to over half a dozen today.

**Hideo Fujiwara,** our author, is a professor at the Graduate School of Information Science, Nara Institute of Science and Technology, in Japan; fujiwara@is.aist-nara.ac.jp.

Today, new benchmarks are required again. The existing ISCAS 85/89 benchmarks are no longer close to the size of industrial designs. We need much larger circuits (perhaps several million gates) to realistically study ATPG efficiency. We need circuits with features found in modern designs and not found in the current benchmarks. We encourage the development of advanced ATPG algorithms that can achieve almost 100% fault efficiency for very large, realistic circuits within practical computation time.

What should a new set of benchmarks include? There should be embedded blocks including memories (RAMs, ROMs, CAMs) and increasingly common cores such as microprocessors and DSPs. They should include complex multiple-clock domains, common I/O structures (bidirectional pins, boundary scan), and internal tristate buses. The designs should be hierarchical to reflect modern design practices.

The current benchmarks are described in a simple netlist format. Future benchmarks should be available at the behavioral, register-transfer, and gate levels. They should be described in a high-level language such as VHDL to facilitate research on high-level ATPG.

Learning from our experience with the ISCAS 85/89 benchmarks, we believe these new benchmarks would be very useful. They would not only help in appraising the effectiveness of proposed ATPG algorithms but also act as goals and challenges to stimulate interest in advancing ATPG algorithms that would handle the designs of today and tomorrow. They will also help in driving the development of new DFT techniques for circuits, just as the ISCAS 89 benchmarks helped in the development of partial scan.

The ISCAS 85 benchmarks were first-generation benchmarks for ATPG algorithms, and the ISCAS 89 benchmarks were the second generation. We now need a third generation to tackle urgent current issues and continue to stimulate research on solutions for future issues. Perhaps the solutions to the impossible challenges of today, when represented in third-generation benchmarks, will become the new products of tomorrow.


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