# ISCAS'85 Benchmarks:

## Special Session on ATPG and Fault Simulation, 1985 IEEE International Symposium on Circuits and Systems

Hideo Fujiwara

In 1983, I published the FAN algorithm, and by using actual combinational circuits, showed its superiority over both the D-algorithm and the PODEM algorithm. In 1984, I discussed ATPG benchmarking with Franc Brglez (then with Bell Northern Research) while I was on sabbatical visiting Vinod Agarwal at McGill University.

Before that, we had no benchmarks for ATPG algorithms. Brglez and I agreed that benchmark circuits helped advance ATPG algorithm research and development. We organized a special session on combinational ATPG benchmarking at ISCAS 85 (the 1985 International Symposium on Circuits and Systems) in Kyoto, Japan. With the cooperation of many people from industries and universities in the USA, Canada, Europe, and Japan, we collected excellent benchmarks with various and useful characteristics.

Later, others reported many better, more-efficient ATPG algorithms for combinational circuits. The wide-spread availability of these benchmarks drove the development of new algorithms, as researchers strove to generate the best-known results in terms of runtime, vector length, and fault coverage.

F. Brglez and H. Fujiwara, “A neutral netlist of 10 combinational benchmark circuits and a targeted translator in FORTRAN,” Special Session on ATPG and Fault Simulation, Proc. 1985 IEEE Int. Symp. on Circuits and Systems (ISCAS’85), June 5-7, 1985.

This is not a technical paper, but a reference to the magnetic tape containing “ISCAS’85 combinational benchmark circuits”. The tape was distributed to the authors who contributed to the special session of ISCAS’85.
It was requested to refer the tape in any publication (see my letter dated July 3, 1985, attached below).

Currently, those files can be obtained from the following website.

http://www.cbl.ncsu.edu:16080/benchmarks/ISCAS85/

Hideo Fujiwara
Department of Electronics and
Communication
Meiji University
1-1-1 Higashi-mita, Tama-ku
Kawasaki 214, Japan

July 3, 1985

Dear Colleague,

Below please find information on how to read on the tape containing "ISCAS'85 combinational benchmark circuits." If you are to publish your experiences with these circuits, please reference this tape in any publications as follows:

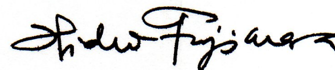
F. Brglez and H. Fujiwara, "A neutral netlist of 10 combinational benchmark circuits and a target translator in FORTRAN," Special Session on ATPG and Fault Simulation, Proc. 1985 IEEE Int. Symp. Circuits and Systems, Kyoto, Japan, June 5-7, 1985.

and send a pre-print to us.

Feel free to distribute the tape further, however please send us a note so that we can keep an up-to-date list of all recipients.

The magnetic tape contains a short FORISCAS FORTRAN program and a set of combinational logic descriptions written in an inefficient but easily convertable "neutral file format". From the attached documentation of a simple example you will discover that the FORISCAS FORTRAN program translates the neutral file into the format of your choice: FUNSIM, TEGAS, OSAKA, CADAT. Should e.g. your TEGAS format be somewhat different, small changes within a subroutine of FORISCAS FORTRAN will give you what you want. The exception is the CADAT format that will require insertion of more code, but the code will be quite similar to the one supported for the test example.

Very truly yours,



Hideo Fujiwara

```
Tape density              = 1600 BPI

Label processing          = no labels

Character format          = EBCDIC

Physical block length     = 800 bytes

Logical record length     = 80 bytes

     ==>  10 logical records per physical block on tape

File order on tape:

     FORISCAS FORTRAN
     FORISCAS EXEC
     C17      ISCAS
     C432     ISCAS
     C499     ISCAS
     C880     ISCAS
     C1355    ISCAS
     C1908    ISCAS
     C2670    ISCAS
     C3540    ISCAS
     C5315    ISCAS
     C6288    ISCAS
     C7552    ISCAS

Tape terminated with 5 write marks
```

# ISCAS'85

## 1985 International Symposium on Circuits and Systems

June 5-7, 1985 Kyoto Hotel, Kyoto, Japan

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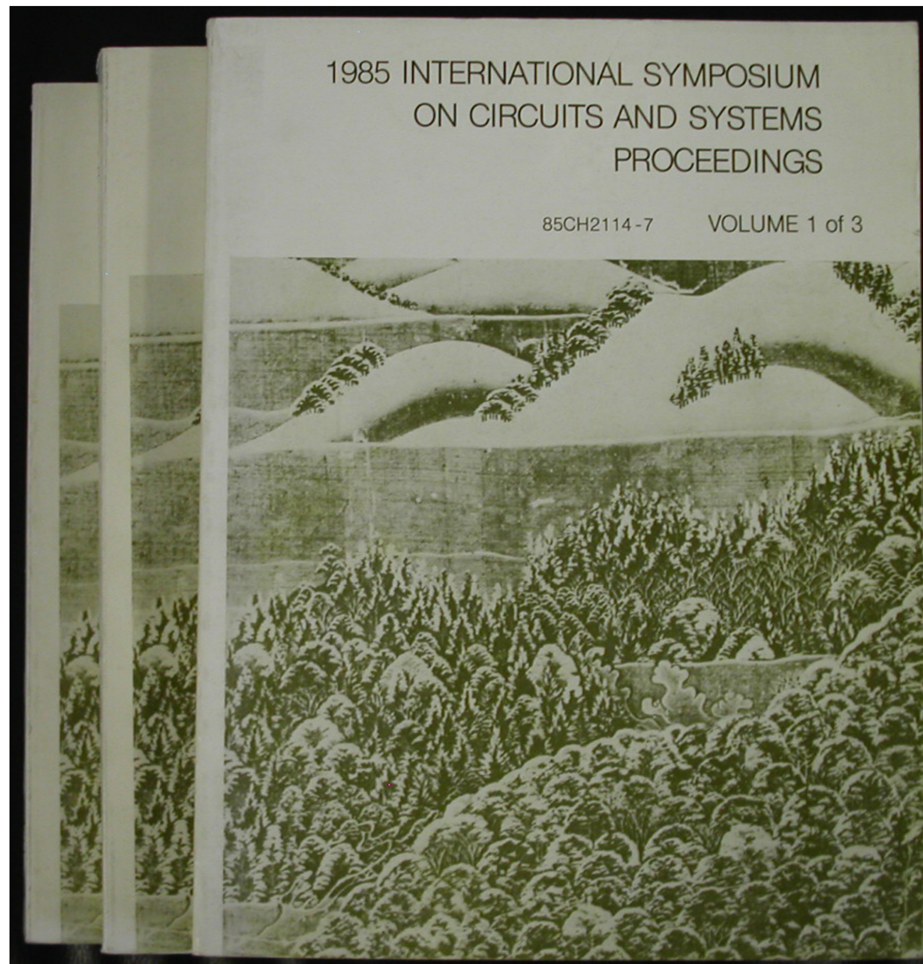


Special Session

**Recent Algorithms for Gate-Level ATPG with Fault Simulation and Their Performance Assessment**

***Organizer/Chairman:*** F. Brglez, *Bell Northern Research, Ottawa, ONT, Canada*
***Co-Organizer/Co-Chairman:*** H. Fujiwara, *Meiji University, Kawasaki, Japan*


S6AB. 1: **Automatic Test Pattern Generator for Large Combinational Circuits** — 663
M. Kawai, K. Oozeki, M. Takahashi, M. Ono, Y. Ishizaka, T. Masui, *NEC Corporation, Fuchu, Japan*

S6AB. 2: **Results from Applications of a Commercial ATG System to Large-Scale Combinational Circuits** — 667
B.C. Rosales, P. Goel, *Gateway Design Automation Corporation, Littleton, MA, USA*

S6AB. 3: **FAN: A Fanout-Oriented Test Pattern Generation Algorithm** — 671
H. Fujiwara, *Meiji University, Kawasaki, Japan*

S6AB. 4: **Test Generation for LSI Circuits Using Extended Nine-Valued Method** — 675
M. Murakami, H. Kikuchihara, *Oki Electric Industry Co. Ltd., Hachioji, Japan*

S6AB. 5: **An Efficient Test Generation Method by 10-V Algorithm** — 679
Y. Takamatsu, *Saga University, Saga, Japan*, K. Kinoshita, *Hiroshima University, Hiroshima, Japan*

S6AB. 6: **ATPG via Random Pattern Simulation** — 683
J.L. Carter, S. Dennis, V.S. Iyenger, B.K. Rosen, *IBM Corporation, Yorktown Heights, NY, USA*

S6AB. 7: **Probabilistically Guided Test Generation** — 687
V.D. Agrawal, *AT&T Bell Laboratories, Murray Hill, NJ, USA*, S.C. Seth, C.C. Chuang, *University of Nebraska, Lincoln, NE, USA*

S6AB. 8: **Applications of Testability Analysis to ATG** — 691
E. Trischler, *Siemens AG, Munich, F.R. Germany*, M. Schulz, *Technical University of München, Munich, F.R. Germany*

S6AB. 9: **Accelerated ATPG and Fault Grading via Testability Analysis** — 695
F. Brglez, P. Pownall, R. Hum, *Bell Northern Research, Ottawa, ONT, Canada*

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