テスト生成アルゴリズムとベンチマークの歴史
～ 半世紀の歩み ～

藤原 秀雄

奈良先端科学技術大学院大学 情報科学研究科　〒630-0192 生駒市高山町 8916-5

あらまし R.D.Eldred がテスト生成に関する世界で最初の論文を 1959 年の Journal of ACM に発表してからちょうど半世紀が過ぎました。 その間、数多くの優れたテスト生成アルゴリズムが研究開発され、今日の半導体産業を支える多くの優れた ATPG ツールに至っています。 本講演では、テスト生成アルゴリズムの歴史を振り返り、個性豊かなアルゴリズムが次々と研究開発されて来た半世紀の歩みを紹介します。 また、それらの活発な研究の起爆剤となった ISCAS85, ISCAS89, ITC99 のベンチマークがどのように作られ、多くの研究者に役立って来たか、その歴史についても紹介します。

History of Test Generation Algorithms and Benchmarks
– Half a Century of the Progress –

Hideo FUJIWARA

Graduate School of Information Science, Nara Institute of Science and Technology
8916-5 Takayama, Ikoma, Nara, 630-0192 Japan

Abstract Half a century has passed since R. D. Eldred published the first paper on test generation in Journal of ACM in 1959. Until now, many excellent algorithms for test generation have been reported and they have come to many excellent ATPG tools supporting today's semiconductor industries. In this talk, looking back on the long history of test generation algorithms, we introduce those excellent and unique ATPG algorithms that appeared and contributed in the progress of half a century. We also introduce the history of benchmarks of ISCAS85, ISCAS89, and ITC99 that became the trigger of those active and animated research and development.

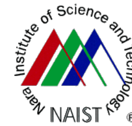
January 20-22, 2011
64th FTC Workshop

History of Test Generation Algorithms and Benchmarks:

Half a Century of the Progress

Hideo Fujiwara

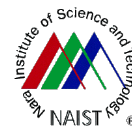
Nara Institute of Science and Technology



1

Outline

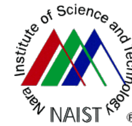
- My Personal History
- History of Test Generation Algorithms
- Digression: FAN and Non-Scan
- History of Benchmarks



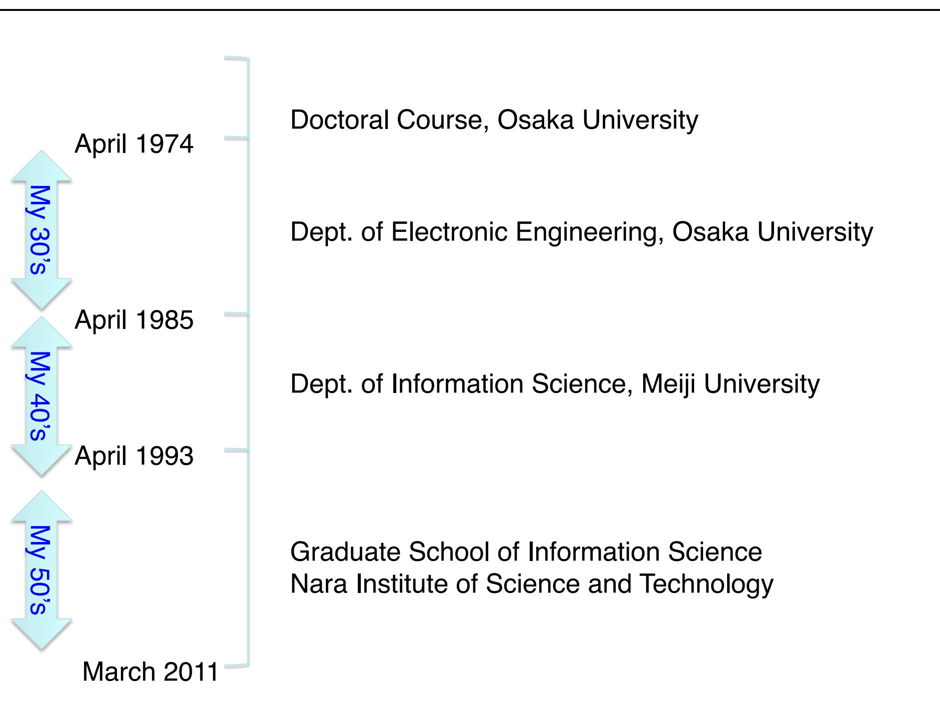
2

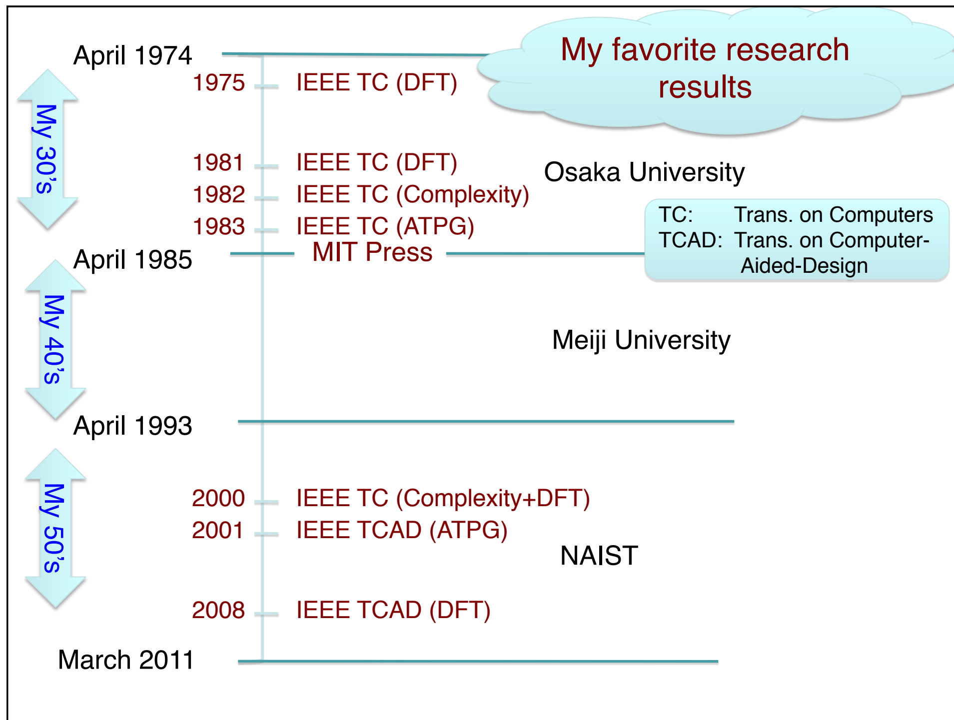
Outline

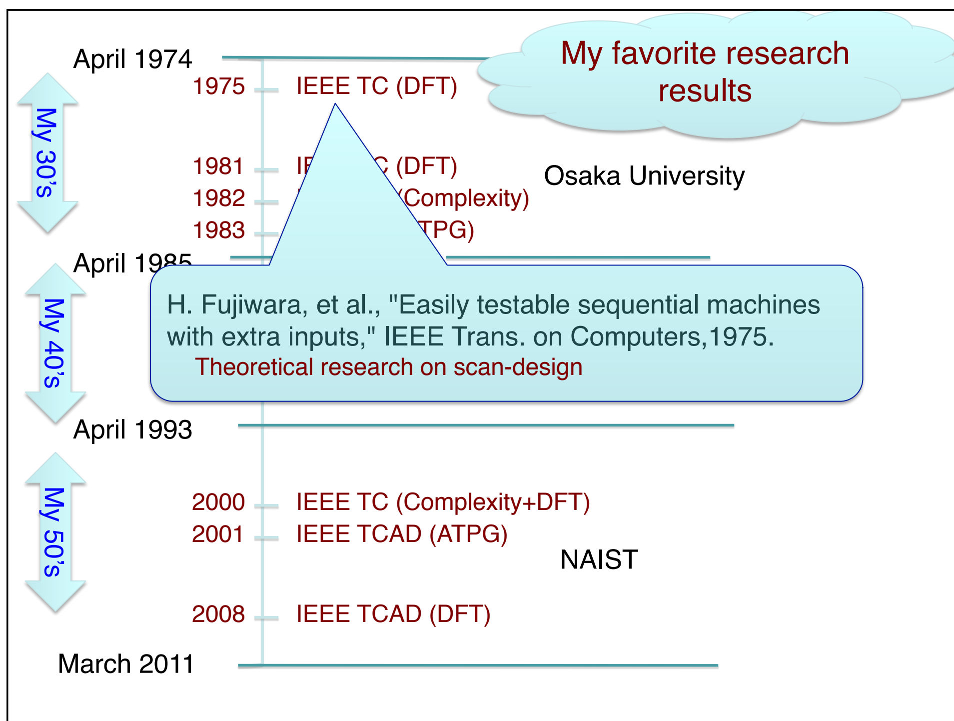
- My Personal History
- History of Test Generation Algorithms
- Digression: FAN and Non-Scan
- History of Benchmarks

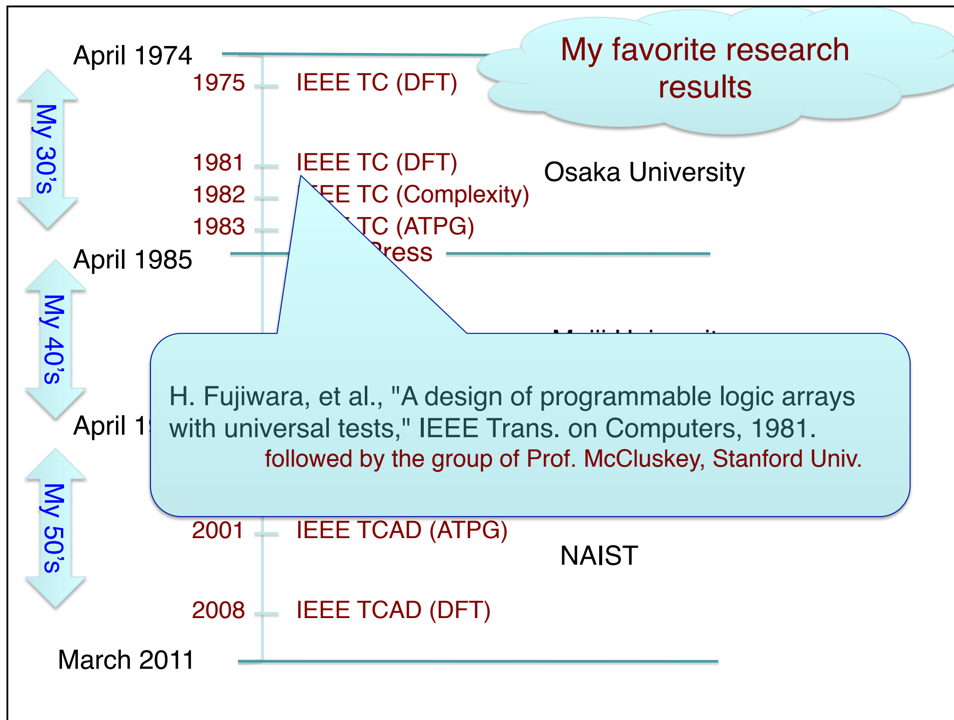


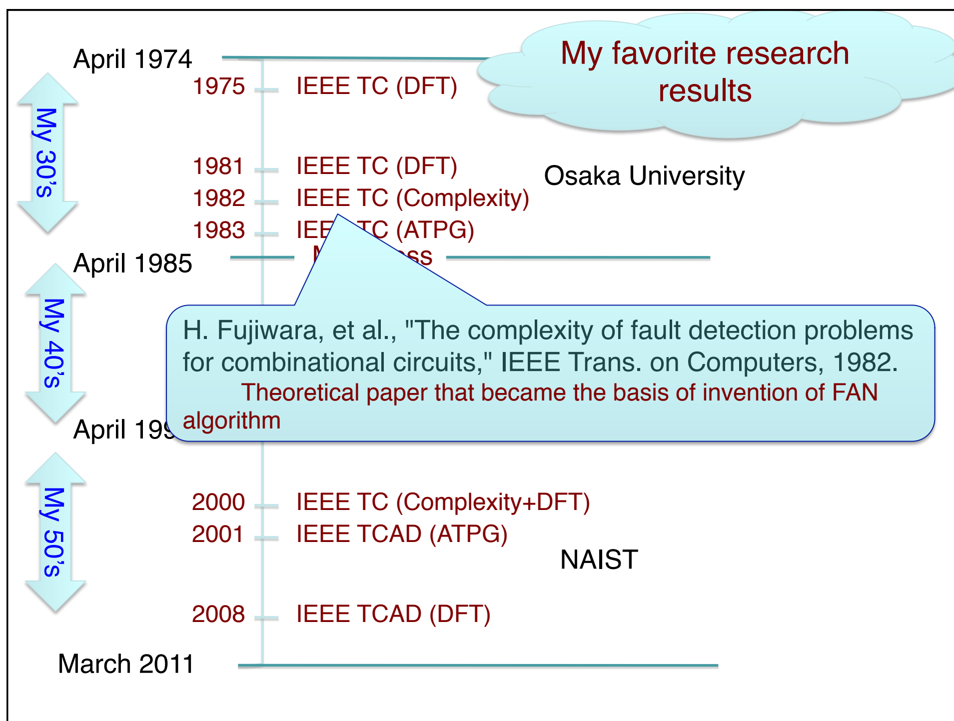
3

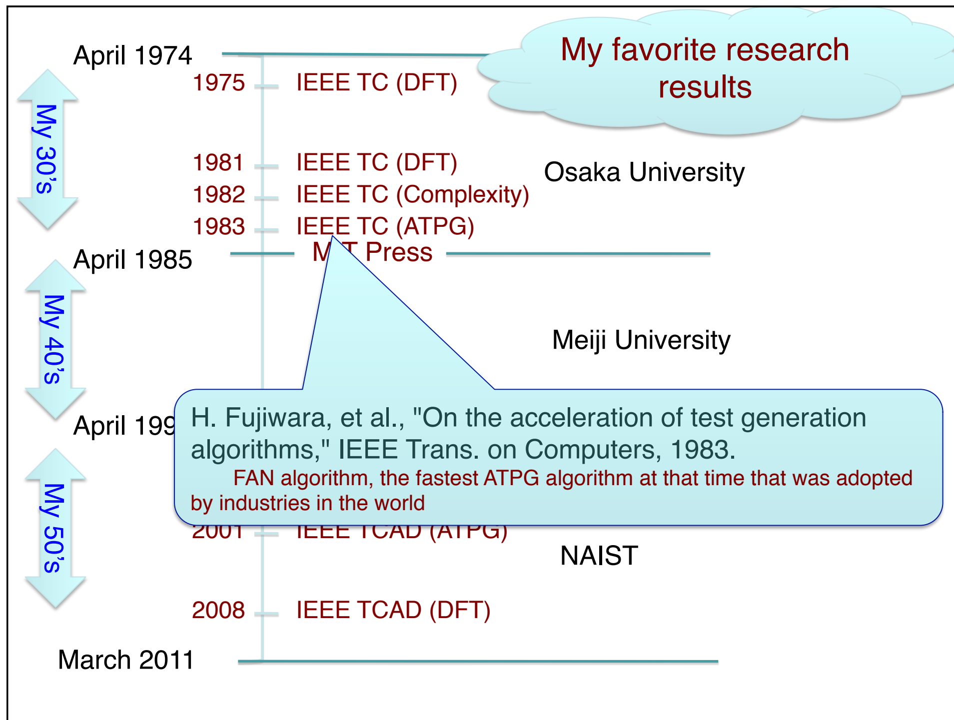


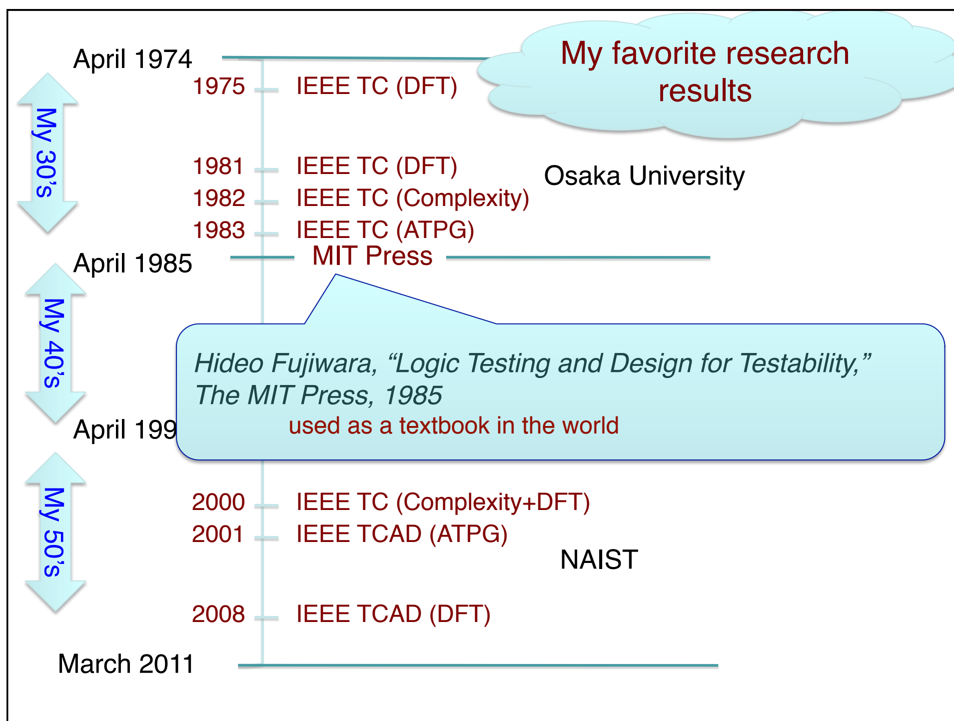

My favorite research results
April 1974
1975 IEEE TC (DFT)
My 30's
1981 IEEE TC (DFT)
1982 IEEE TC (Complexity)
1983 IEEE TC (ATPG)
Osaka University
TC: Trans. on Computers
TCAD: Trans. on Computer-Aided-Design
April 1985
MIT Press
My 40's
Meiji University
April 1993
My 50's
2000 IEEE TC (Complexity+DFT)
2001 IEEE TCAD (ATPG)
NAIST
2008 IEEE TCAD (DFT)
March 2011

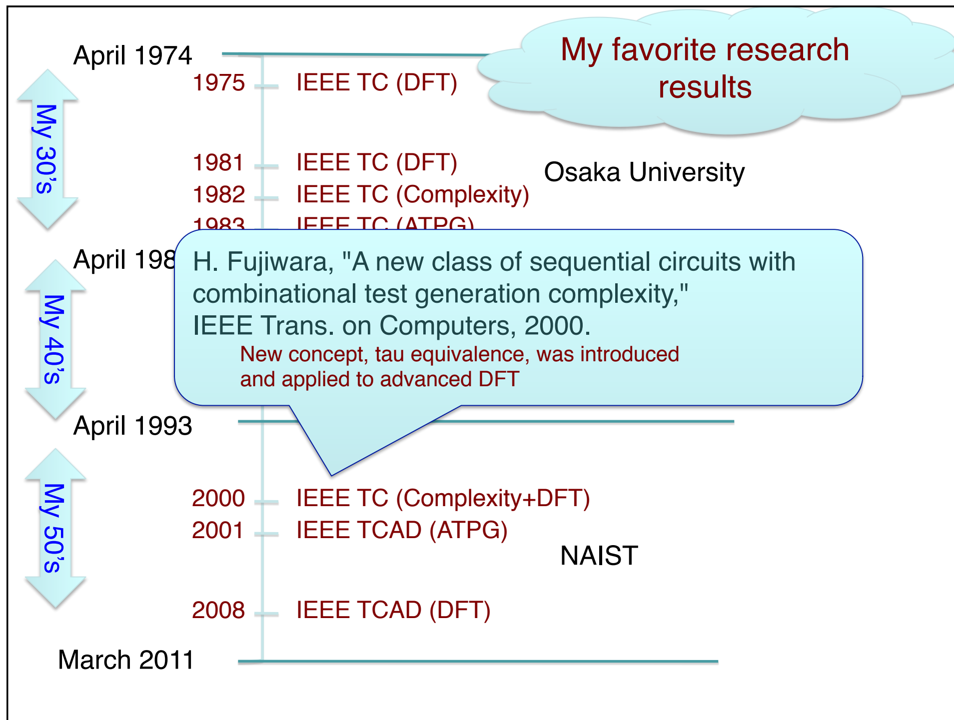

My favorite research results
April 1974
1975 IEEE TC (DFT)
My 30's
1981
1982
1983
Osaka University
My 40's
H. Fujiwara, et al., "Easily testable sequential machines with extra inputs," IEEE Trans. on Computers,1975.
Theoretical research on scan-design
April 1993
My 50's
2000 IEEE TC (Complexity+DFT)
2001 IEEE TCAD (ATPG)
NAIST
2008 IEEE TCAD (DFT)
March 2011

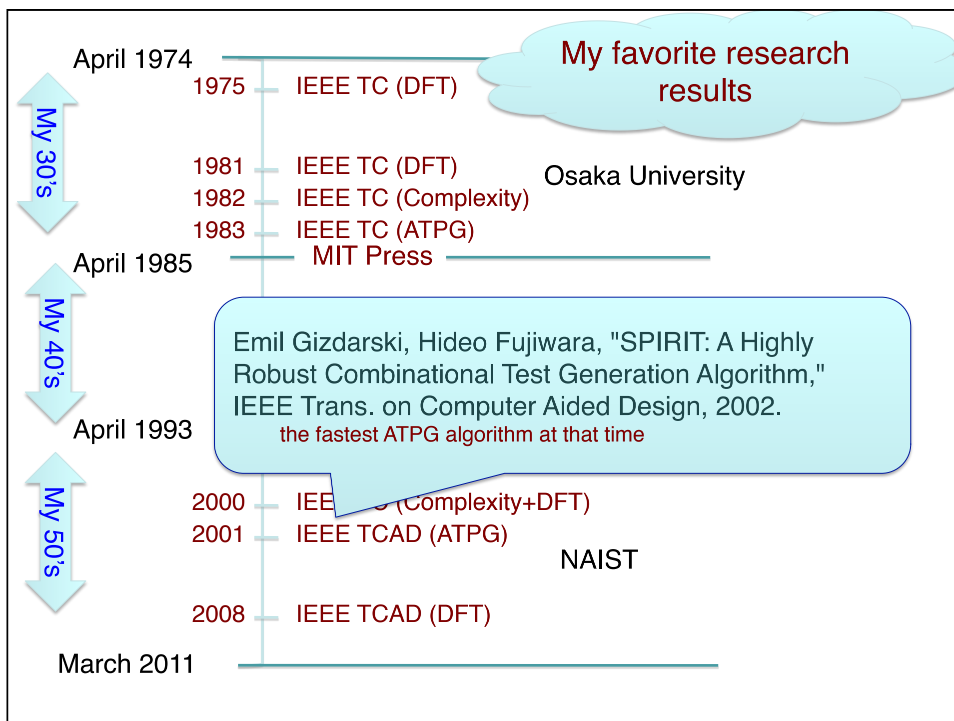

My favorite research results
April 1974
1975 IEEE TC (DFT)
1981 IEEE TC (DFT)
1982
1983
Osaka University
April 1985
2001 IEEE TCAD (ATPG)
NAIST
2008 IEEE TCAD (DFT)
March 2011
My 30's
My 40's
My 50's
H. Fujiwara, et al., "A design of programmable logic arrays with universal tests," IEEE Trans. on Computers, 1981.
followed by the group of Prof. McCluskey, Stanford Univ.

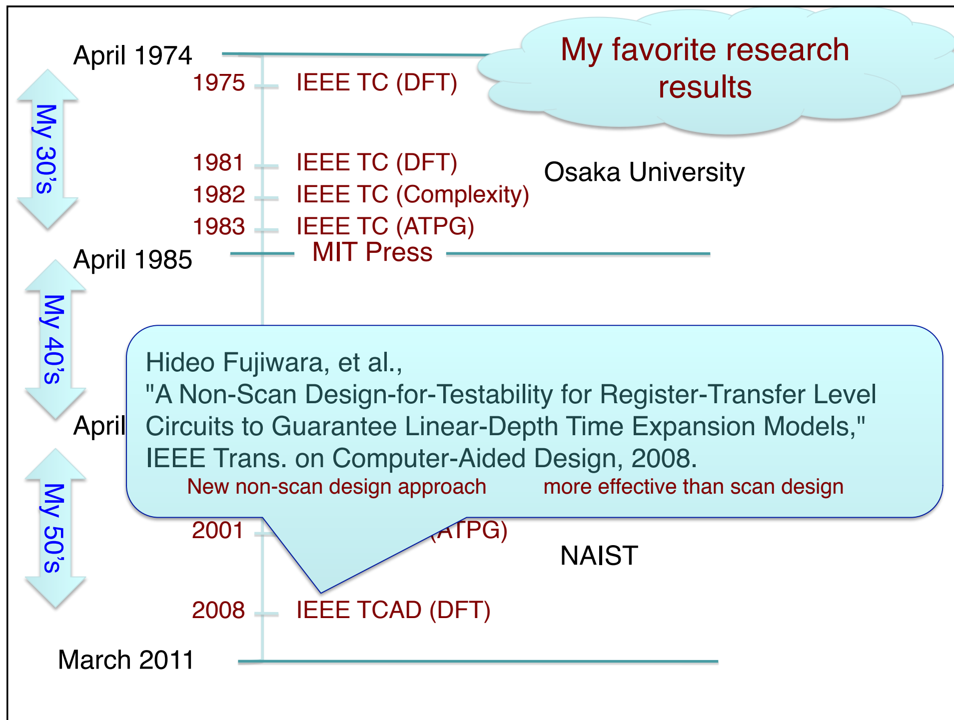

My favorite research results
April 1974
1975 IEEE TC (DFT)
1981 IEEE TC (DFT)
1982 IEEE TC (Complexity)
1983
Osaka University
April 1985
2000 IEEE TC (Complexity+DFT)
2001 IEEE TCAD (ATPG)
NAIST
2008 IEEE TCAD (DFT)
March 2011
My 30's
My 40's
My 50's
H. Fujiwara, et al., "The complexity of fault detection problems for combinational circuits," IEEE Trans. on Computers, 1982.
Theoretical paper that became the basis of invention of FAN algorithm


My favorite research results
April 1974
1975 IEEE TC (DFT)
My 30's
1981 IEEE TC (DFT)
1982 IEEE TC (Complexity)
1983 IEEE TC (ATPG)
Osaka University
April 1985
MIT Press
My 40's
Meiji University
April 199
H. Fujiwara, et al., "On the acceleration of test generation algorithms," IEEE Trans. on Computers, 1983.
FAN algorithm, the fastest ATPG algorithm at that time that was adopted by industries in the world
My 50's
NAIST
2008 IEEE TCAD (DFT)
March 2011


My favorite research results
April 1974
1975 IEEE TC (DFT)
My 30's
1981 IEEE TC (DFT)
1982 IEEE TC (Complexity)
1983 IEEE TC (ATPG)
Osaka University
April 1985
MIT Press
My 40's
Hideo Fujiwara, "Logic Testing and Design for Testability," The MIT Press, 1985
used as a textbook in the world
April 199
My 50's
2000 IEEE TC (Complexity+DFT)
2001 IEEE TCAD (ATPG)
NAIST
2008 IEEE TCAD (DFT)
March 2011


My favorite research results
April 1974
1975
IEEE TC (DFT)
My 30's
1981
IEEE TC (DFT)
1982
IEEE TC (Complexity)
Osaka University
April 198
My 40's
H. Fujiwara, "A new class of sequential circuits with combinational test generation complexity," IEEE Trans. on Computers, 2000.
New concept, tau equivalence, was introduced and applied to advanced DFT
April 1993
My 50's
2000
IEEE TC (Complexity+DFT)
2001
IEEE TCAD (ATPG)
NAIST
2008
IEEE TCAD (DFT)
March 2011


My favorite research results
April 1974
1975
IEEE TC (DFT)
My 30's
1981
IEEE TC (DFT)
1982
IEEE TC (Complexity)
1983
IEEE TC (ATPG)
Osaka University
April 1985
MIT Press
My 40's
Emil Gizdarski, Hideo Fujiwara, "SPIRIT: A Highly Robust Combinational Test Generation Algorithm," IEEE Trans. on Computer Aided Design, 2002.
the fastest ATPG algorithm at that time
April 1993
My 50's
2000
2001
IEEE TCAD (ATPG)
NAIST
2008
IEEE TCAD (DFT)
March 2011

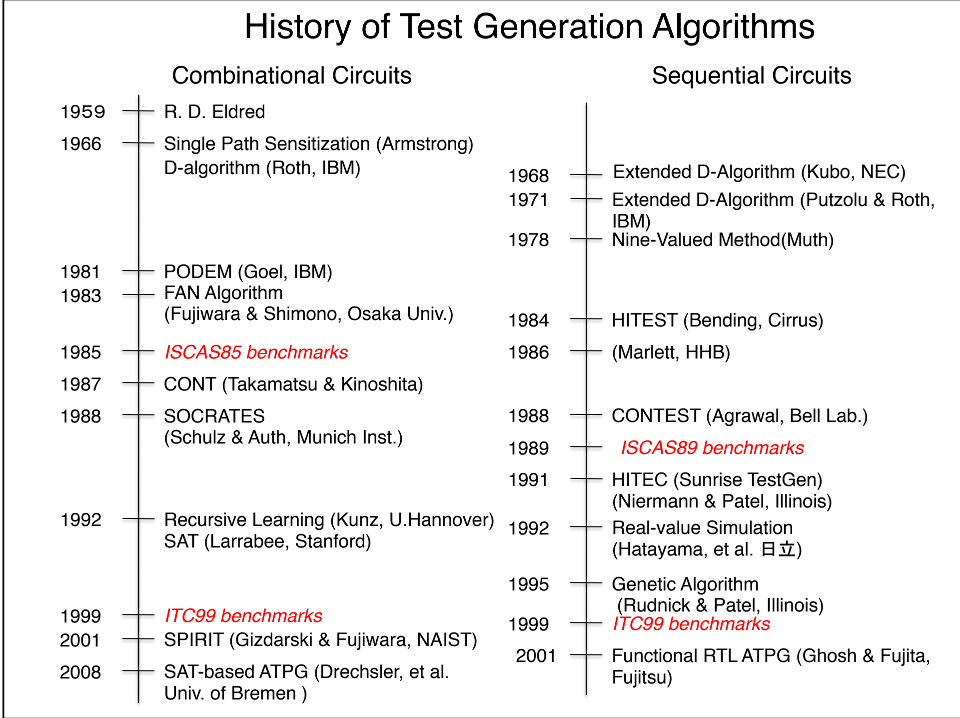


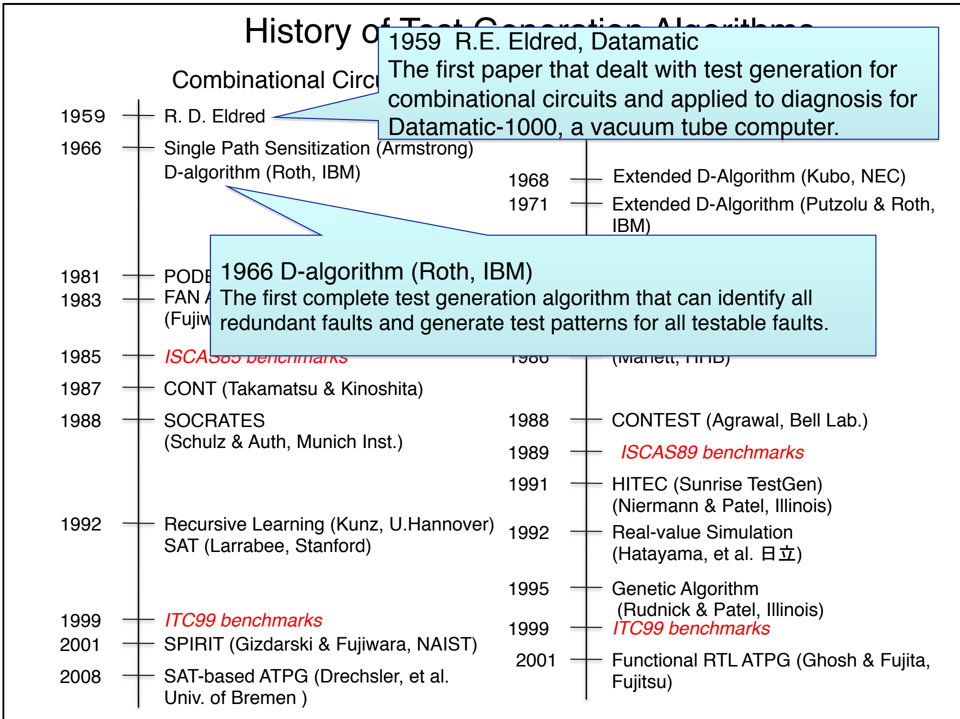
Outline

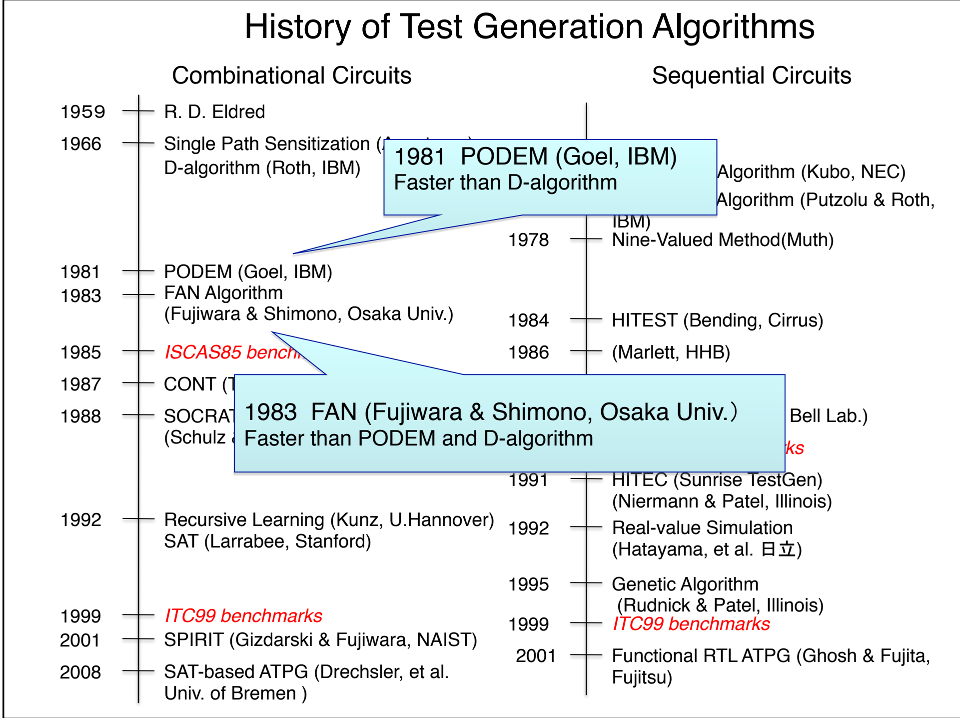
- My Personal History
- History of Test Generation Algorithms
- Digression: FAN and Non-Scan
- History of Benchmarks

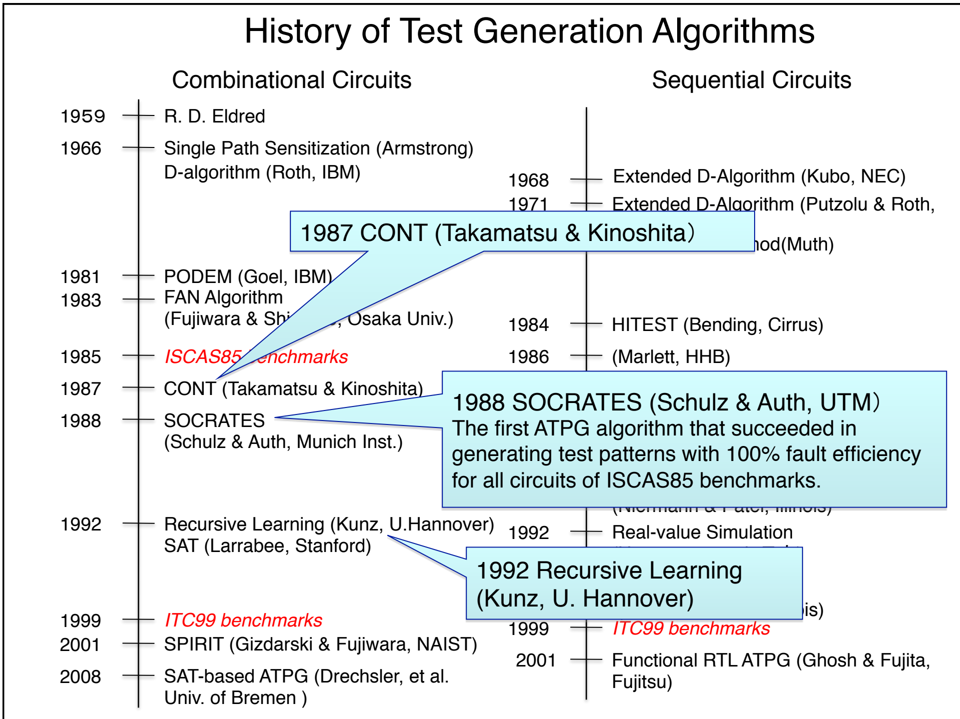
Nara Institute of Science and Technology NAIST

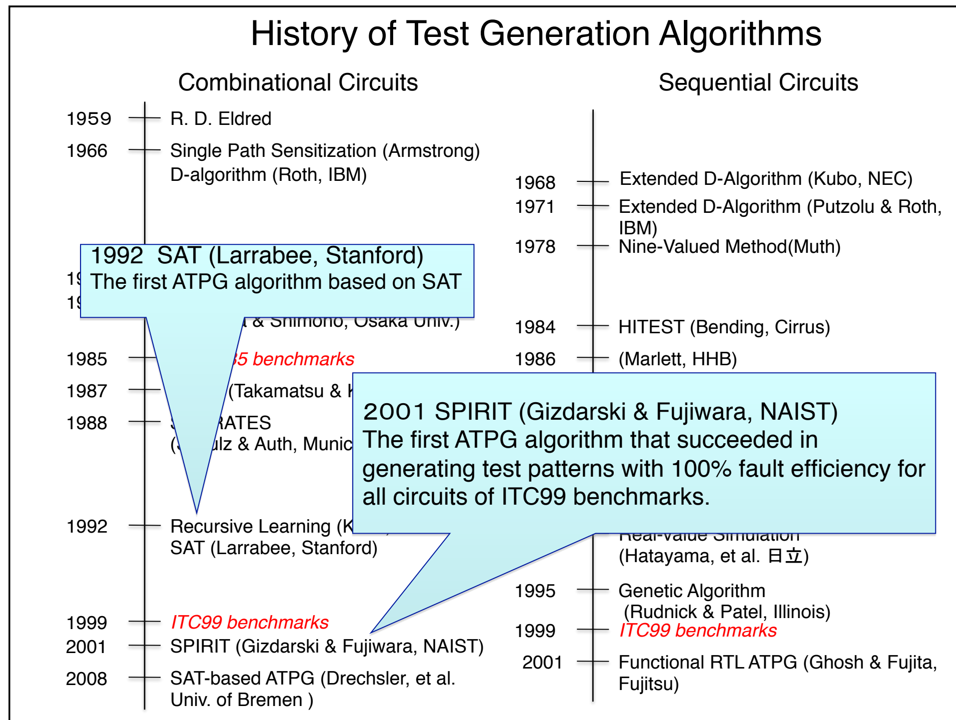
14

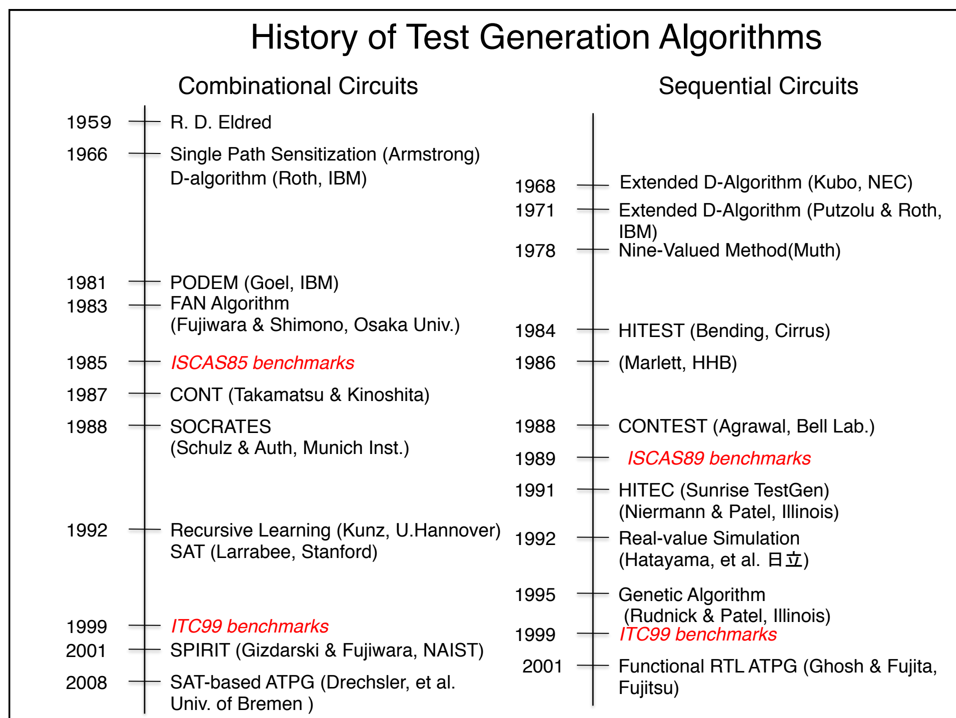

History of Test Generation Algorithms
Combinational Circuits
Sequential Circuits
1959 R. D. Eldred
1966 Single Path Sensitization (Armstrong)
D-algorithm (Roth, IBM)
1981 PODEM (Goel, IBM)
1983 FAN Algorithm
(Fujiwara & Shimono, Osaka Univ.)
1985 ISCAS85 benchmarks
1987 CONT (Takamatsu & Kinoshita)
1988 SOCRATES
(Schulz & Auth, Munich Inst.)
1992 Recursive Learning (Kunz, U.Hannover)
SAT (Larrabee, Stanford)
1999 ITC99 benchmarks
2001 SPIRIT (Gizdarski & Fujiwara, NAIST)
2008 SAT-based ATPG (Drechsler, et al.
Univ. of Bremen)
1968 Extended D-Algorithm (Kubo, NEC)
1971 Extended D-Algorithm (Putzolu & Roth, IBM)
1978 Nine-Valued Method(Muth)
1984 HITEST (Bending, Cirrus)
1986 (Marlett, HHB)
1988 CONTEST (Agrawal, Bell Lab.)
1989 ISCAS89 benchmarks
1991 HITEC (Sunrise TestGen)
(Niermann & Patel, Illinois)
1992 Real-value Simulation
(Hatayama, et al. 日立)
1995 Genetic Algorithm
(Rudnick & Patel, Illinois)
1999 ITC99 benchmarks
2001 Functional RTL ATPG (Ghosh & Fujita, Fujitsu)


1959 R.E. Eldred, Datamatic
The first paper that dealt with test generation for combinational circuits and applied to diagnosis for Datamatic-1000, a vacuum tube computer.
1966 D-algorithm (Roth, IBM)
The first complete test generation algorithm that can identify all redundant faults and generate test patterns for all testable faults.


History of Test Generation Algorithms
Combinational Circuits
Sequential Circuits
1959 R. D. Eldred
1966 Single Path Sensitization (
D-algorithm (Roth, IBM)
1981 PODEM (Goel, IBM)
Faster than D-algorithm
Algorithm (Kubo, NEC)
Algorithm (Putzolu & Roth,
IBM)
1978 Nine-Valued Method(Muth)
1981 PODEM (Goel, IBM)
1983 FAN Algorithm
(Fujiwara & Shimono, Osaka Univ.)
1984 HITEST (Bending, Cirrus)
1985 ISCAS85 bench
1986 (Marlett, HHB)
1987 CONT (T
1988 SOCRAT
(Schulz
1983 FAN (Fujiwara & Shimono, Osaka Univ.)
Faster than PODEM and D-algorithm
Bell Lab.)
1991 HITEC (Sunrise TestGen)
(Niermann & Patel, Illinois)
1992 Recursive Learning (Kunz, U.Hannover)
SAT (Larrabee, Stanford)
1992 Real-value Simulation
(Hatayama, et al. 日立)
1995 Genetic Algorithm
(Rudnick & Patel, Illinois)
1999 ITC99 benchmarks
2001 SPIRIT (Gizdarski & Fujiwara, NAIST)
1999 ITC99 benchmarks
2008 SAT-based ATPG (Drechsler, et al.
Univ. of Bremen)
2001 Functional RTL ATPG (Ghosh & Fujita,
Fujitsu)

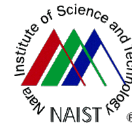

History of Test Generation Algorithms
Combinational Circuits
Sequential Circuits
1959 R. D. Eldred
1966 Single Path Sensitization (Armstrong)
D-algorithm (Roth, IBM)
1968 Extended D-Algorithm (Kubo, NEC)
1971 Extended D-Algorithm (Putzolu & Roth,
1987 CONT (Takamatsu & Kinoshita)
1981 PODEM (Goel, IBM)
1983 FAN Algorithm
(Fujiwara & Shi , Osaka Univ.)
1984 HITEST (Bending, Cirrus)
1985 ISCAS85 enchmarks
1986 (Marlett, HHB)
1987 CONT (Takamatsu & Kinoshita)
1988 SOCRATES
(Schulz & Auth, Munich Inst.)
1988 SOCRATES (Schulz & Auth, UTM)
The first ATPG algorithm that succeeded in
generating test patterns with 100% fault efficiency
for all circuits of ISCAS85 benchmarks.
1992 Recursive Learning (Kunz, U.Hannover)
SAT (Larrabee, Stanford)
1992 Real-value Simulation
1992 Recursive Learning
(Kunz, U. Hannover)
1999 ITC99 benchmarks
2001 SPIRIT (Gizdarski & Fujiwara, NAIST)
1999 ITC99 benchmarks
2008 SAT-based ATPG (Drechsler, et al.
Univ. of Bremen)
2001 Functional RTL ATPG (Ghosh & Fujita,
Fujitsu)


History of Test Generation Algorithms
Combinational Circuits
Sequential Circuits
1959 R. D. Eldred
1966 Single Path Sensitization (Armstrong)
D-algorithm (Roth, IBM)
1992 SAT (Larrabee, Stanford)
The first ATPG algorithm based on SAT
1985
1987
1988
1992 Recursive Learning
SAT (Larrabee, Stanford)
1999 ITC99 benchmarks
2001 SPIRIT (Gizdarski & Fujiwara, NAIST)
2008 SAT-based ATPG (Drechsler, et al. Univ. of Bremen)
1968 Extended D-Algorithm (Kubo, NEC)
1971 Extended D-Algorithm (Putzolu & Roth, IBM)
1978 Nine-Valued Method(Muth)
1984 HITEST (Bending, Cirrus)
1986 (Marlett, HHB)
2001 SPIRIT (Gizdarski & Fujiwara, NAIST)
The first ATPG algorithm that succeeded in generating test patterns with 100% fault efficiency for all circuits of ITC99 benchmarks.
(Hatayama, et al. 日立)
1995 Genetic Algorithm
(Rudnick & Patel, Illinois)
1999 ITC99 benchmarks
2001 Functional RTL ATPG (Ghosh & Fujita, Fujitsu)


History of Test Generation Algorithms
Combinational Circuits
Sequential Circuits
1959 R. D. Eldred
1966 Single Path Sensitization (Armstrong)
D-algorithm (Roth, IBM)
1981 PODEM (Goel, IBM)
1983 FAN Algorithm
(Fujiwara & Shimono, Osaka Univ.)
1985 ISCAS85 benchmarks
1987 CONT (Takamatsu & Kinoshita)
1988 SOCRATES
(Schulz & Auth, Munich Inst.)
1992 Recursive Learning (Kunz, U.Hannover)
SAT (Larrabee, Stanford)
1999 ITC99 benchmarks
2001 SPIRIT (Gizdarski & Fujiwara, NAIST)
2008 SAT-based ATPG (Drechsler, et al. Univ. of Bremen)
1968 Extended D-Algorithm (Kubo, NEC)
1971 Extended D-Algorithm (Putzolu & Roth, IBM)
1978 Nine-Valued Method(Muth)
1984 HITEST (Bending, Cirrus)
1986 (Marlett, HHB)
1988 CONTEST (Agrawal, Bell Lab.)
1989 ISCAS89 benchmarks
1991 HITEC (Sunrise TestGen)
(Niermann & Patel, Illinois)
1992 Real-value Simulation
(Hatayama, et al. 日立)
1995 Genetic Algorithm
(Rudnick & Patel, Illinois)
1999 ITC99 benchmarks
2001 Functional RTL ATPG (Ghosh & Fujita, Fujitsu)

Outline

- My Personal History
- History of Test Generation Algorithms
- Digression: FAN and Non-Scan
- History of Benchmarks



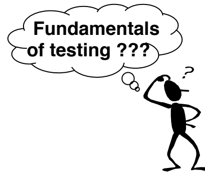
21

The basis is necessary for development

- For a tree to grow larger, its root must grow bigger and deeper into the ground.
- Similarly, for test technologies (leaves) to develop, substantial results of the fundamental research (root) are necessary.
- The more enriched the fundamental research results become, the more enriched the practical research results become.

22

Fundamental problems of testing

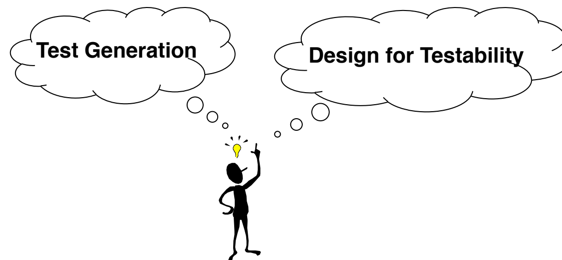


What are the fundamentals of testing?

I had the opportunity to ask myself the same question 28 years ago when I was requested to write a book from MIT Press.

23

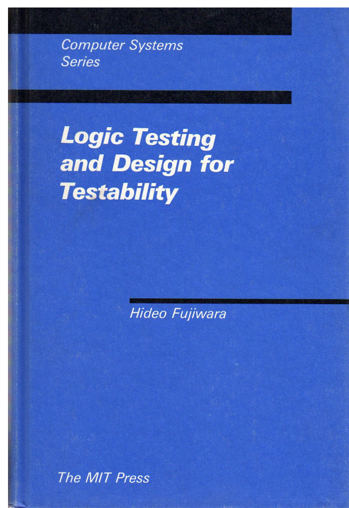
Fundamental problems of testing



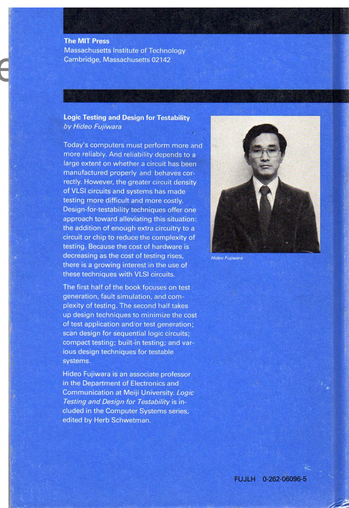
So, I decided to write a book with the following title.

Hideo Fujiwara, *Logic Testing and Design for Testability*, The MIT Press, 1985

24



roble



The MIT Press
Massachusetts Institute of Technology
Cambridge, Massachusetts 02142

Logic Testing and Design for Testability
by Hideo Fujiwara

Today's computers must perform more and more reliably. And reliability depends to a large extent on whether a circuit has been manufactured properly and behaves correctly. However, the greater circuit density of VLSI circuits and systems has made testing more difficult and more costly. Design-for-testability techniques offer one approach toward alleviating this situation: the addition of enough extra circuitry to a circuit or chip to reduce the complexity of testing. Because the cost of hardware is decreasing as the cost of testing rises, there is a growing interest in the use of these techniques with VLSI circuits.

The first half of the book focuses on test generation, fault simulation, and complexity of testing. The second half takes up design techniques to minimize the cost of test application and/or test generation; scan design for sequential logic circuits; compact testing; built-in testing; and various design techniques for testable systems.

Hideo Fujiwara is an associate professor in the Department of Electronics and Communication at Meiji University. *Logic Testing and Design for Testability* is included in the Computer Systems series, edited by Herb Schwetman.

FUJLH 0-262-06096-5

So, I decided to write a book with the following title.

Hideo Fujiwara, *Logic Testing and Design for Testability*,
The MIT Press, 1985

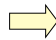
25

From my experience,

Theoretical / basic research can contribute to practical research

For test generation (30's at Osaka Univ.)

Polynomial Time Class ???



FAN algorithm

Complexity analysis for test generation

Efficient test generation algorithm

For design-for-testability (50's at NAIST)

Acyclic testability???

Non-scan DFT

26

Classification of sequential circuits

Optimal design-for-testability

Complexity of test generation

[Fujiwara, et al, IEEE Trans. Comp, 1982]

- *Fault detection* (FD): Is a given single stuck-at fault detectable?
  kM-FD: Fault detection problem for k-level monotone circuits
  kU-FD: Fault detection problem for k-level unate circuits

- *Theorem 1 :*
  3M-FD is NP-complete.
  Hence,
  3U-FD and FD are NP-complete.

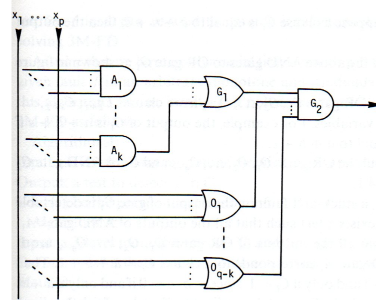


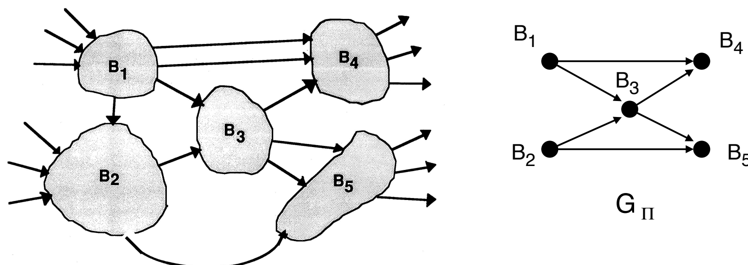
Figure 4.1
A 3-level monotone circuit Q_1

27

Complexity of test generation

[Fujiwara, et al, IEEE Trans. Comp, 1982]

- A combinational circuit C is said to be *k-bounded* if there exists a partition $\Pi=\{B_1, B_2, \ldots, B_t\}$ such that
  (1) the number of inputs of each block Bi is at most *k*, and
  (2) graph G_Π has no cycle.



28

Complexity of test generation

[Fujiwara, et al, IEEE Trans. Comp, 1982]

- *Theorem 2:* Let C be a *k-bounded* circuit. Then there is an algorithm of time complexity $O(16^k m)$ to find a test for a single stuck-at fault in C, where m is the number of lines in C.

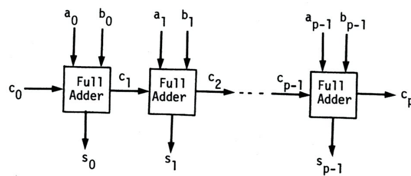


Figure 4.3
Ripple-carry adder

3-bounded circuit

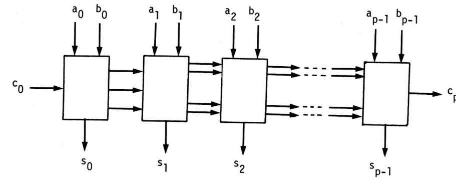
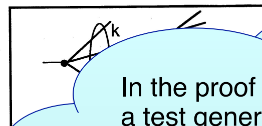


Figure 4.4
Gate-minimum *p*-bit adder

6-bounded circuit

Complexity of test generation

[Fujiwara, et al, IEEE Trans. Comp, 1982]



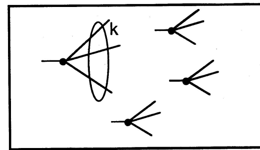
In the proof of this theorem, we showed a test generation algorithm that assigns 4 values, 0, 1, D, and D', at each fanout-point.
This algorithm became the basis for the later FAN algorithm.

- k-FL-FD:
- k-FPB-FD: Fault ... -bounded circuits

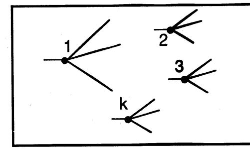
Theorem 3 :
k-FL-FD is NP-complete if k>2.
k-FPB-FD is solvable in $O(4^k m)$ where m is the number of lines in C.

Complexity of test generation

[Fujiwara, et al, IEEE Trans. Comp, 1982]



k-fanout-limited



k-fanout-point-bounded

- Observation:
  - k-FL-FD is NP-complete even if k is a constant.
  - k-FPB-FD is solvable in O(m) if k is a constant.

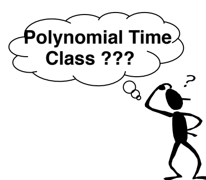
- The complexity of test generation is affected
  not by the number of fanout branches from a fanout point
  but by the number of fanout points.

31

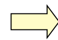
Complexity of test generation

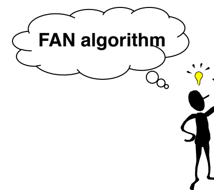
[Fujiwara, et al, IEEE Trans. Comp, 1982]

The algorithm shown in the theorem became the basis for the later FAN algorithm.



Complexity analysis for test generation





Efficient test generation algorithm

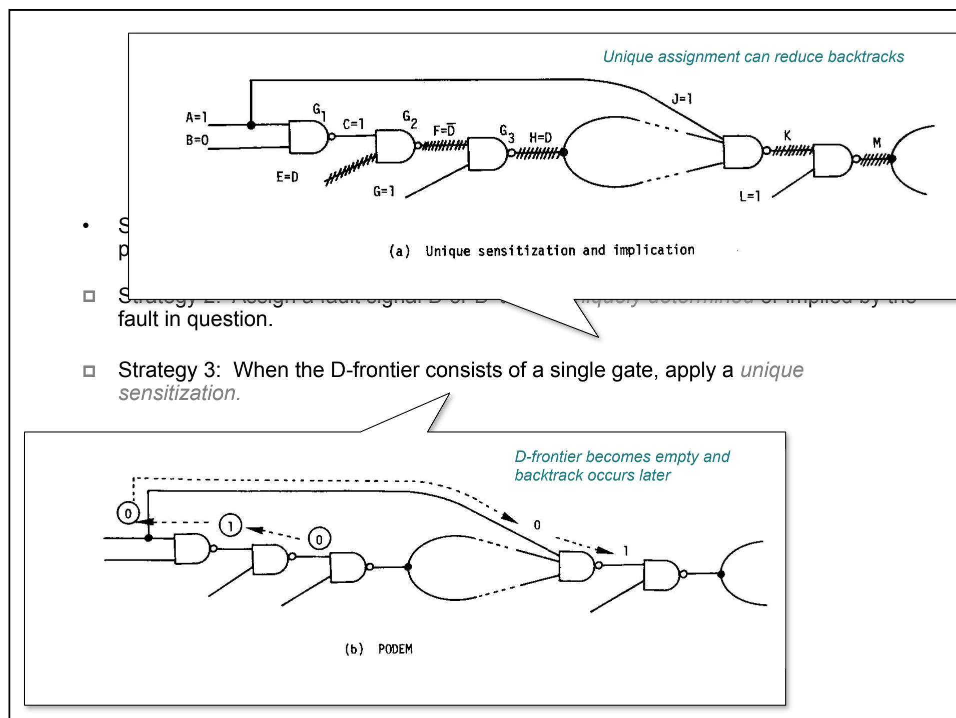
32

Heuristics of the FAN algorithm

[Fujiwara, et al, IEEE Trans. Comp., 1983]

- Strategy 1: In each step of the algorithm, determine as many signal values as possible that can be *uniquely implied*.
- Strategy 2: Assign a fault signal D or D' that is *uniquely determined* or implied by the fault in question.
- Strategy 3: When the D-frontier consists of a single gate, apply a *unique sensitization.*
- Strategy 4: Stop the backtrace at a *head line*, and postpone the line justification for the head line to later.
- Strategy 5: *Multiple backtracing* (concurrent backtracing of more than one path) is more efficient than backtracing along a single path.

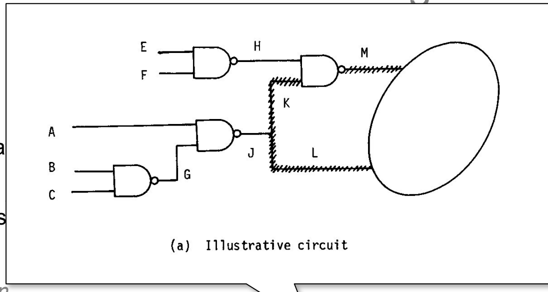
33



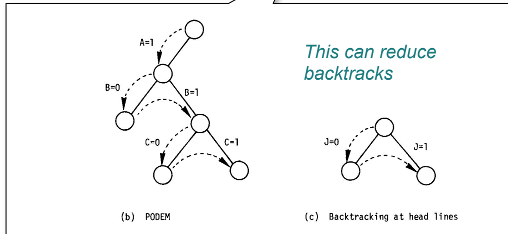
Heuristics of the FAN algorithm

3]

- Strategy 1: ... possible tha... ...alues as
- Strategy 2: ... fault in ques... ...implied by the
- Strategy 3: ... *...ue sensitization.*



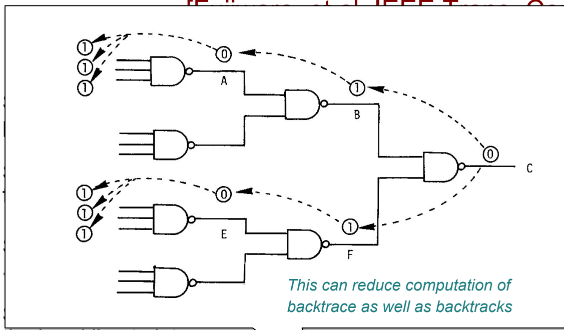
- Strategy 4: Stop the backtrace at a *head line*, and postpone the line justification for the head line to later.



Heuristics of the FAN algorithm

[F... ...mp., 1983]

- ...y signal values as
- ...*ermined* or implied by the
- ...pply a *unique*
- ... the line justification for the head line to later.



- Strategy 5: *Multiple backtracing* (concurrent backtracing of more than one path) is more efficient than backtracing along a single path.

Heuristics of the FAN algorithm

[Fujiwara, et al, IEEE Trans. Comp., 1983]

- Strategy 1: In each step of the algorithm, determine as many signal values as possible that can be *uniquely implied*.
- St fa
- St se
- St th
- St m

PODEM assigns a binary value only to primary inputs.
So, backtracks occur at primary inputs.

FAN assigns a binary value only to head lines and fanout points.
So, backtracks occur at headlines and fanout points.

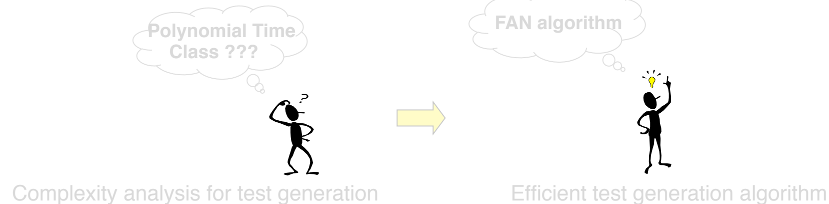
This is effective to reduce the number of backtracks.

- Strategy 6: In the multiple backtrace, if an objective at a fanout point p has a contradictory requirement, stop the backtrace so as to *assign a binary value to the fanout point.*

37

From my experience,
Theoretical / basic research can contribute to practical research

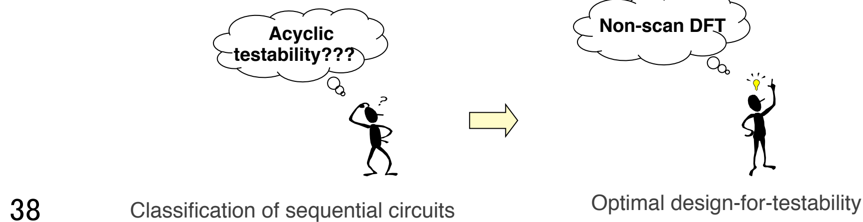
For test generation (30's at Osaka Univ.)



Complexity analysis for test generation

Efficient test generation algorithm

Next is as for design-for-testability (50's at NAIST)



38

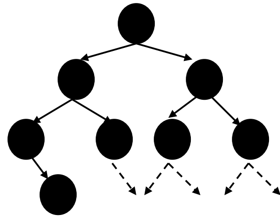
Classification of sequential circuits

Optimal design-for-testability

Classification of sequential circuits

Combinational test generation complexity

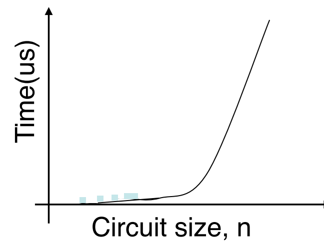
Theoretically,



CTG is NP-hard.

CTG = Combinational Test Generation Problem

Empirically,



CTG seems to be solved in time $O(n^r)$ for some constant r.

[Goel 1980], [Prasad 1999]

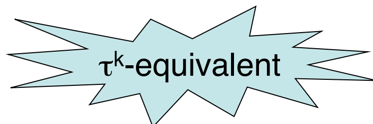
39

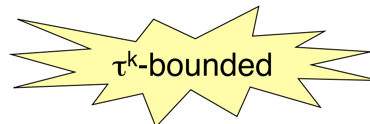
Classification of sequential circuits

τ^k notation

[Fujiwara, IEEE Trans. Comp., 2000]
[Fujiwara, et al, IEEE Trans. CAD, 2008]

- Introduced τ^k **notation** to clarify the time complexity for the test generation problem.





- Classified sequential circuits based on τ^k **notation** .

40

Classification of sequential circuits

Test generation complexity [Fujiwara, IEEE TCAD, 2008]

- Let
  - P_C : combinational test generation problem.
  - P_S : sequential test generation problem.
  - P_α : class α test generation problem.

- Let $T_C(n)$, $T_S(n)$ and $T_\alpha(n)$ be the *time complexity* of P_C , P_S and P_α respectively.
- We assume that $T_C(n) = \Theta(n^r)$ for some constant r larger than 2.
- *Combinational test generation complexity:* $\tau(n) = T_C(n)$

41

Classification of sequential circuits

τ^k-equivalent and τ^k-bounded [Fujiwara, IEEE TCAD, 2008]

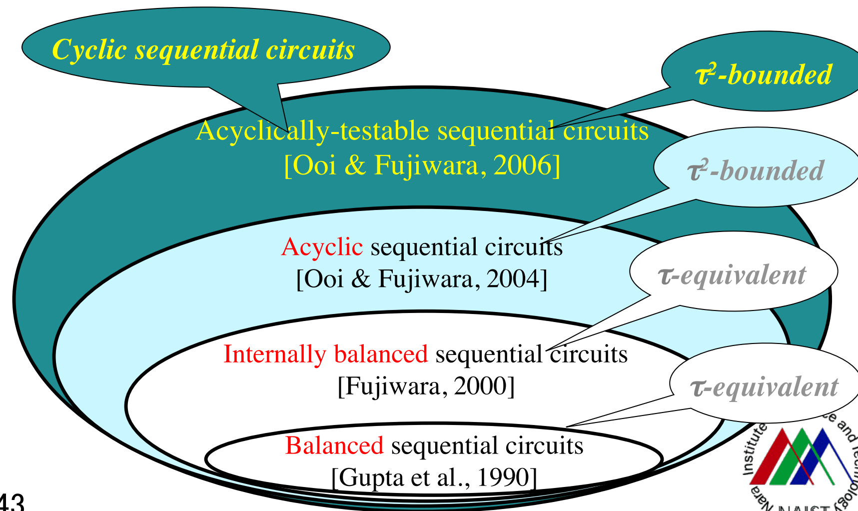
- A class α is *τ^k-equivalent* if $T_\alpha(n)=\Theta(\tau^k(n))$
  and *τ^k–bounded* if $T_\alpha(n)=O(\tau^k(n))$
  where k is a positive integer.

- A class of circuits with *combinational test generation complexity* is *τ-equivalent*

42

Classification of sequential circuits

Class of acyclic test generation complexity



43

Classification of sequential circuits

Design for acyclic testability

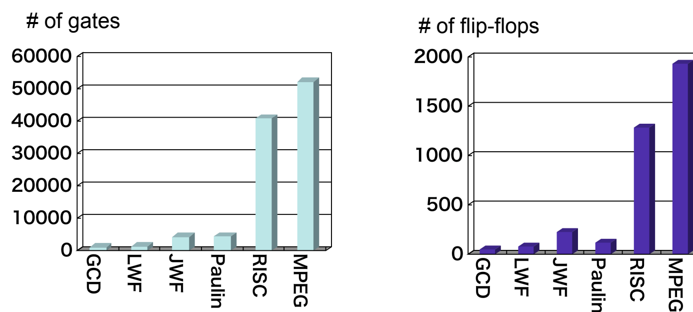
- Introduced two classes of acyclically-testable circuits
  - Thru-testable circuits (at gate level)
    [C.Y.Ooi, H.Fujiwara, ICCD 2006]
  - Linear-depth time-bounded circuits (at RTL)
    [H.Iwata, T.Yoneda, H.Fujiwara, DAC 2007]
- Proposed Non-Scan type DFT for acyclic testability
  - Non-scan
  - At-speed test
  - 100% fault efficiency
  - Hardware overhead is lower than Full Scan
  - Test application time is much shorter than Full Scan

44

Design for acyclic testability

[Fujiwara, et al, IEEE Trans. CAD, 2008]

- Linear-depth time-bounded RTL circuits

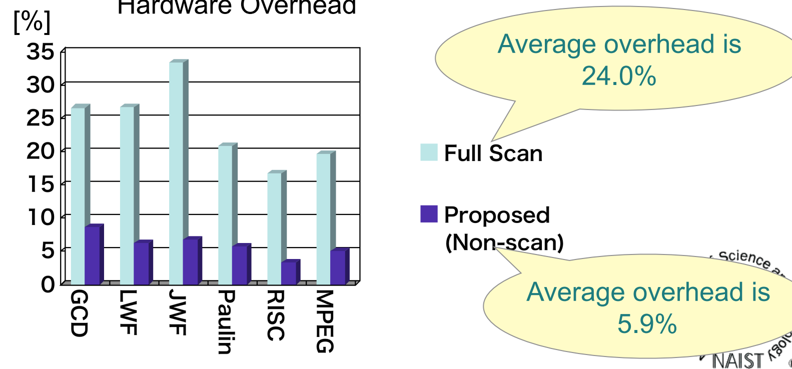


45

Design for acyclic testability

[Fujiwara, et al, IEEE Trans. CAD, 2008]

- Linear-depth time-bounded RTL circuits



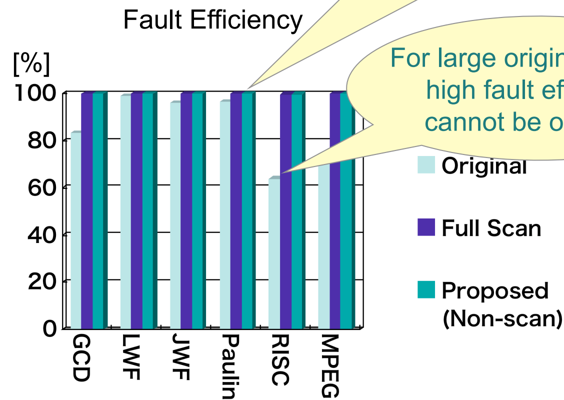
46

Design for acyclic testability

[Fujiwara, et al. IEEE T... CAD, 2008]

- Linear-depth time-bounded...

Full scan & Proposed Non-Scan can achieve almost 100% fault efficiency



For large original circuits, high fault efficiency cannot be obtained

47

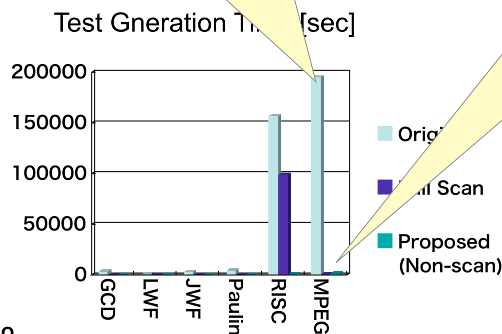
Design for acyclic testability

[Fujiwara, et al, IEEE Trans. CAD, 2008]

For original circuits, test generation is very time-consuming, even for low fault efficiency

...ed RT...

For full scan & proposed non-scan, test generation is very fast



...its	Test Generation Time [sec]		
	Original	Full Scan	Proposed Non Scan
GCD	3,070.07	0.27	1.72
LWF	85.45	0.17	1.01
JWF	2,873.34	0.88	5.91
Paulin	4,290.51	0.53	8.07
RISC	156,808.67	98,870.71	166.88
MPEG	195,260.82	55.72	1,208.90

48

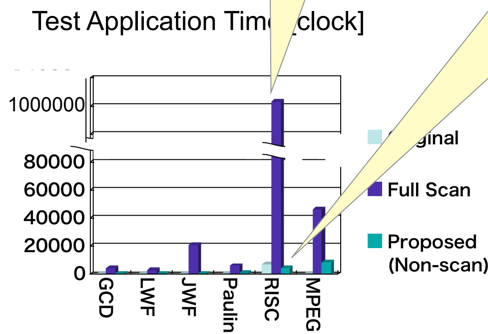
Design for acyclic testability

Test application time is very long for full scan

Test application time for full scan is 284 times longer than proposed non-scan for RISC, and 54 times longer for MPEG

- Linear-depth t... RTL ci...

Test Application Tim... [clock]



Circuits	Test Application Time [clock]		
	Original	Full Scan	Proposed Non Scan
GCD	421	4,232	588
LWF	392	2,904	108
JWF	412	20,975	675
Paulin	201	6,147	798
RISC	6,928	1,233,859	4,345
MPEG	148	462,942	8,515

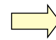
49

From my experience,

We showed some examples that theoretical / basic research can contribute to practical research

For test generation (30's at Osaka Univ.)

Polynomial Time Class ???



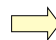
FAN algorithm

Complexity analysis for test generation

Efficient test generation algorithm

Next is as for design-for-testability (50's at NAIST)

Acyclic testability???



Non-scan DFT

Classification of sequential circuits

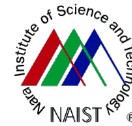
Optimal design-for-testability

50

Outline

- My Personal History
- History of Test Generation Algorithms
- Digression: FAN and Non-Scan
- History of Benchmarks

51



History of Benchmarks

1983 (37 years old) — FAN algorithm FTCS-13@Milano

1984 (38 years old) — Sabbatical McGill Univ.@Montreal

1985 (39 years old) — ISCAS'85 benchmarks ISCAS'85@Kyoto

1988 (42 years old) — Lunch Meeting ITC'88@Washington D.C.

1989 (43 years old) — ISCAS'89 benchmarks ISCAS'89@Portland,Oregon

1998 (52 years old) — The Last Byte H.Fujiwara@IEEE_Design&Test

1999 (53 years old) — ITC'99 benchmarks ITC'99@Atlantic City, NJ

2010 (64 years old) — The Last Byte R.Aitken@IEEE_Design&Test

History of Benchmarks

1983 (37 years old) — FAN algorithm — FTCS-13@Milano

1984 (38 years old) — Sabbatical — McGill Univ.@Montreal

1985 (39 years old) — ISCAS'85 ...

1988 (42 years old) — Lunch ... ...gton D.C.

1989 (43 years old) — ISCAS'89 benchmarks — ISCAS'89@Portland,Oregon

1998 (52 years old) — The Last Byte — H.Fujiwara@IEEE_Design&Test

1999 (53 years old) — ITC'99 benchmarks — ITC'99@Atlantic City, NJ

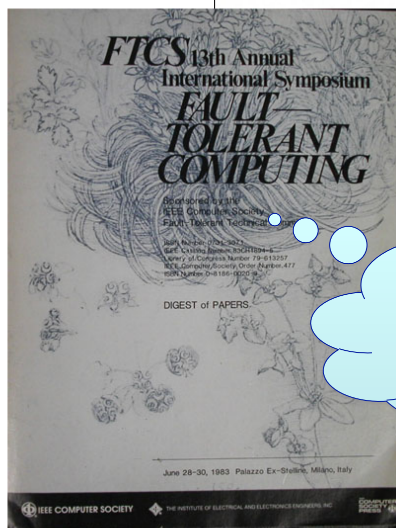
2010 (64 years old) — The Last Byte — R.Aitken@IEEE_Design&Test

Presentation of FAN algorithm raised the necessity of benchmarks for ATPG

FTCS−13

13th International Symposium on Fault-Tolerant Computing

June 28-30, 1983 Palazzo Ex-Stelline, Milano, Italy



ON THE ACCELERATION OF TEST GENERATION ALGORITHMS

Hideo Fujiwara and Takeshi Shimono

Department of Electronic Engineering
Osaka University
2-1, Yamada-Oka, Suita
Osaka, 565 JAPAN

occurrence of backtracks in the algorithm and to shorten the processing time between backtracks. In this paper we consider several techniques to accelerate test generation and present a new algorithm for generating tests called FAN (FANout-oriented test generation algorithm). FAN is a complete algorithm in that it will generate a test if one exists. Experimental results on large combinational circuits of up to 3000 gates demonstrate that the FAN algorithm is ...

... logical 0 (s-a-0) or stuck at logical 1 (s-a-1). A fault consisting of a single stuck line is called a single fault. We shall focus our attention only on detecting single stuck faults.

In this section, aiming at the acceleration of test generation, we shall point out some defects of the PODEM algorithm and consider several effective techniques to eliminate these disadvantages.

In generating a test, the algorithm creates a decision tree in which there is more than one choice

... generation algorithm only for combinational circuits.

Many test generation algorithms have been pro-

- H.Fujiwara, T. Shimono (Osaka Univ.)
- E. Fujiwara (NTT)
- T. Nanya, Y. Thoma (TIT)
- K. Yoshihara, Y.Koga, T. Ishihara (NDA)
- K.Furuya, Y. Akita, Y. Thoma (TIT)

History of Benchmarks

1983 (37 years old) — FAN algorithm FTCS-13@Milano

1984 (38 years old) — Sabbatical McGill Univ.@Montreal

1985 (39 years old) — ISC '85 benchmarks ISCAS'85@Kyoto

During my sabbatical at McGill University, I met Franc Brglez of Bell Northern Research (currently, professor of North Carolina State University) and planned to organize Special Session for Benchmarking at ISCAS'85 in Kyoto.

1988 (42 years .

1989 (43 years nd,Oregon

1998 (52 years old) — The Last Byte H.Fujiwara@IEEE_Design&Test

1999 (53 years old) — ITC'99 benchmarks ITC'99@Atlantic City, NJ

2010 (64 years old) — The Last Byte R.Aitken@IEEE_Design&Test

History of Benchmarks

1983 (37 years old) — FAN algorithm FTCS-13@Milano

1984 (38 years old) — Sabbatical McGill Univ.@Montreal

1985 (39 years old) — ISCAS'85 benchmarks ISCAS'85@Kyoto

Franc Brglez and I organized a special session on benchmarking for ATPG at ISCAS'85 in Kyoto. We collected 10 real industrial circuits thanks to industries of USA and Japan. This ISCAS'85 benchmarks proved to be the trigger which one after another new ATPG algorithms have been invented continuously.

1988 (42 years

1989 (43 years on

1998 (52 years old) — The Last Byte H.Fujiwara@IEEE_Design&Test

1999 (53 years old) — ITC'99 benchmarks ITC'99@Atlantic City, NJ

2010 (64 years old) — The Last Byte R.Aitken@IEEE_Design&Test

ISCAS'85

1985 International Symposium on Circuits and Systems

June 5-7, 1985 Kyoto Hotel, Kyoto, Japan

15 February 1985

Dear colleague,

Attached please find several items c
consider and follow the suggestions

- conformation from the ISCAS '85
- agenda for our session; we shoul
presentations to allow for discu
- addresses of single contact pers
once the mats for ISCAS are comp
copy of your work to every addre
- "Table 1" that describes the cir
is working with. It will be incl
the last in the session; you hav
of it on your own pages or simpl
|our paper, this proceedings|.

Prof. Fujiwara and myself have discussed the review process and agreed to suggest that you proceed as follows:

- have your draft of the paper by reviewed by your peers and colleagues within the company or university.
- in presenting quantitative results, emulate the principles and the spirit of profiles established in the paper by Fujiwara and Shimono (FTCS '83, Trans on Comp. Dec '83). In my opinion, these results have provided us with important milestones. The best we can do is to provide similar challenges for others to follow. Some of the examples in this session are identical with the ones described in FTCS '83; correlate fanout stems (points) for identification.
- submit the camera-ready copy on the mats directly to ISCAS organizers by the requested deadline.

Good luck. Thank you all for participation.

Franc Brglez

Franc Brglez

Prof. Fujiwara and myself have discussed the review process and agreed to suggest that you proceed as follows:

- have your draft of the paper by reviewed by your peers and colleagues within the company or university.
- in presenting quantitative results, emulate the principles and the spirit of profiles established in the paper by Fujiwara and Shimono (FTCS '83, Trans on Comp. Dec '83). In my opinion, these results have provided us with important milestones. The best we can do is to provide similar challenges for others to follow. Some of the examples in this session are identical with the ones described in FTCS '83; correlate fanout stems (points) for identification.

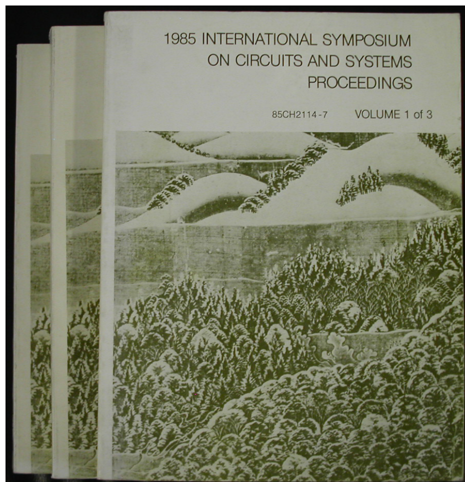
Presentation of FAN made a chance for benchmarking

CIRCUIT NAME										MAX ...NIN
C432									2.10	9
C499	202								2.02	5
C880	383	880	60	26			3.50	8	1.90	4
C1355 (2)	546	1355	41	32	259	1574	2.97	12	1.95	5
C1908	880	1908	33	25	385	1879	2.58	16	1.70	8
C2670	1193	2670	233	140	454	2748	2.74	11	1.74	5
C3540	1669	3540	50	22	579	3431	3.15	16	1.76	8
C5315	2307	5315	178	123	806	5350	3.51	15	1.90	9
C6288	2406	6288	32	32	1456	7744	2.64	16	1.99	2
C7552	3512	7552	207	108	1300	7550	2.95	15	1.75	5

ISCAS'85

1985 International Symposium on Circuits and Systems

June 5-7, 1985 Kyoto Hotel, Kyoto, Japan



Special Session

Recent Algorithms for Gate-Level ATPG with Fault Simulation and Their Performance Assessment

Organizer/Chairman: F. Brglez, *Bell Northern Research, Ottawa, ONT, Canada*
Co-Organizer/Co-Chairman: H. Fujiwara, *Meiji University, Kawasaki, Japan*

S6AB. 1: Automatic Test Pattern Generator for Large Combinational Circuits 663
M. Kawai, K. Oozeki, M. Takahashi, M. Ono, Y. Ishizaka, T. Masui, *NEC Corporation, Fuchu, Japan*

S6AB. 2: Results from Applications of a Commercial ATG System to Large-Scale Combinational Circuits 667
B.C. Rosales, P. Goel, *Gateway Design Automation Corporation, Littleton, MA, USA*

S6AB. 3: FAN: A Fanout-Oriented Test Pattern Generation Algorithm 671
H. Fujiwara, *Meiji University, Kawasaki, Japan*

S6AB. 4: Test Generation for LSI Circuits Using Extended Nine-Valued Method 675
M. Murakami, H. Kikuchihara, *Oki Electric Industry Co. Ltd., Hachioji, Japan*

S6AB. 5: An Efficient Test Generation Method by 10-V Algorithm 679
Y. Takamatsu, *Saga University, Saga, Japan*, K. Kinoshita, *Hiroshima University, Hiroshima, Japan*

S6AB. 6: ATPG via Random Pattern Simulation 683
J.L. Carter, S. Dennis, V.S. Iyenger, B.K. Rosen, *IBM Corporation, Yorktown Heights, NY, USA*

S6AB. 7: Probabilistically Guided Test Generation 687
V.D. Agrawal, *AT&T Bell Laboratories, Murray Hill, NJ, USA*, S.C. Seth, C.C. Chuang, *University of Nebraska, Lincoln, NE, USA*

S6AB. 8: Applications of Testability Analysis to ATG 691
E. Trischler, *Siemens AG, Munich, F.R. Germany*, M. Schulz, *Technical University of München, Munich, F.R. Germany*

S6AB. 9: Accelerated ATPG and Fault Grading via Testability Analysis 695
F. Brglez, P. Pownall, R. Hum, *Bell Northern Research, Ottawa, ONT, Canada*

ISCAS’85

1985 International Symposium on Circuits and Systems

June 5-7, 1985 Kyoto Hotel, Kyoto, Japan

Co-Chairs: F. Brglez, H. Fujiwara

M. Kawai, et al. NEC Corp.

H. Fujiwara, Meiji Univ.

M. Murakami, Oki Electric

Y. Takamatsu, Saga Univ.,
K. Kinoshita, Hiroshima Univ.

Special Session

Recent Algorithms for Gat… …TPG with Fault Simulation and Thei… …orma… Assessment

Organizer/Chairman: F. Brglez, *Bell Northern R… Ottawa, ONT, Canada*

Co-Organizer/Co-Chairman: H. Fujiwara, … *Universi-ty, Kawasa… Japan*

S6AB. 1: **Automatic Test Pattern Generator for Large Combinational Circuits**
M. Kawai, K. Ozeki, M. Takahash… Ishizaka, T. Masui, *NEC Corporatio…*

S6AB. 2: **Results from Applications of a Com… …TG System to Large-Scale Combi…**
B.C. Rosales, P. Goel, *Gateway … poration, Littleton, MA, USA*

S6AB. 3: **FAN: A Fanout-Oriented Test Pat… …eration Algorithm**
H. Fujiwara, *Meiji University, Ka… , Japan*

S6AB. 4: **Test Generation for LSI C…rcuits Using Extended Nine-Valued Method**
M. Murakami, H. Kikuchihara, *Oki Electric Industry Co. Ltd., Hachioji, Japan*

S6AB. 5: **An Efficient Test Generation Method by 10-V Algorithm**
Y. Takamatsu, *Saga University, Saga, Japan*, K. Kinoshita, *Hiroshima University, Hiroshima, Japan*

S6AB. 6: **ATPG via Rando… Pattern Simulation**
…er, S. Denn… …S. Iyenger, B.K. Rosen, *IBM …ion, York… …eights, NY, USA*

…ilisticall… …l Test Generation
V.D. Agrawal, *A… …boratories, Murray Hill, NJ,* …S.C. Seth, *…, University of Nebraska,*

S6AB. 8: **Appli…**
E. Tris… Schulz, … Germany

S6AB. 9: **Accelerated ATPG and Fault Grading via Testability Analysis**
F. Brglez, P. Pownall, R. Hum, *Bell Northern Research, Ottawa, ONT, Canada*

ISCAS’85

1985 International Symposium on Circuits and Systems

June 5-7, 1985 Kyoto Hotel, Kyoto, Japan

F. Brglez and H. Fujiwara, "A neutral netlist of 10 combinational benchmark circuits and a target translator in FORTRAN," Special Session on ATPG and Fault Simulation, Proc. 1985 IEEE Int. Symp. Circuits and Systems, Kyoto, Japan, June 5-7, 1985.

Hideo Fujiwara
Department of Elec… and
Communication
Meiji University
1-1-1 Higashi-mit…
Kawasaki 214, Japa…

July 3, 1985

Dear Colleague,

Below please find information on how to read on the ta… containing "ISCAS'85 combinational benchmark circuits." If … are to publish your experiences with these circuits, … reference this tape in any publications as follows:

F. Brglez and H. Fujiwara, "A neutral netlist of 10 combinational benchmark circuits and a target translator in FORTRAN," Special Session on ATPG and Fault Simulation, Proc. 1985 IEEE Int. Symp. Circuits and Systems, Kyoto, Japan, June 5-7, 1985.

and send a pre-print to us.

Feel free to distribute the tape further, however please send us a note so that we can keep an up-to-date list of all recipients.

The magnetic tape contains a short FORISCAS FORTRAN program and a set of combinational logic descriptions written in an inefficient but easily convertable "neutral file format". From the attached documentation of a simple example you will discover that the FORISCAS FORTRAN program translates the neutral file into the format of your choice: FUNSIM, TEGAS, OSAKA, CADAT. Should e.g. your TEGAS format be somewhat different, small changes within a subroutine of FORISCAS FORTRAN will give you what you want. The exception is the CADAT format that will require insertion of more code, but the code will be quite similar to the one supported for the test example.

Very truly yours,

Hideo Fujiwara

Hideo Fujiwara

Tape density = 1600 BPI

Label processing = no labels

Character format = EBCDIC

Physical block length = 800 bytes

Logical record length = 80 bytes

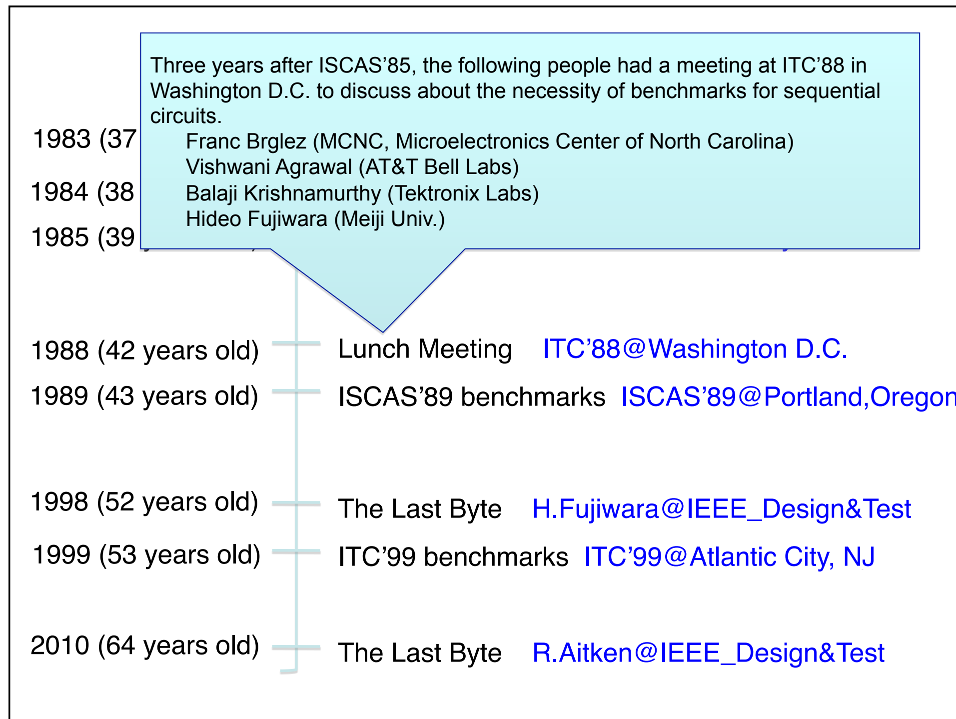
==> 10 logical records per physical block on tape

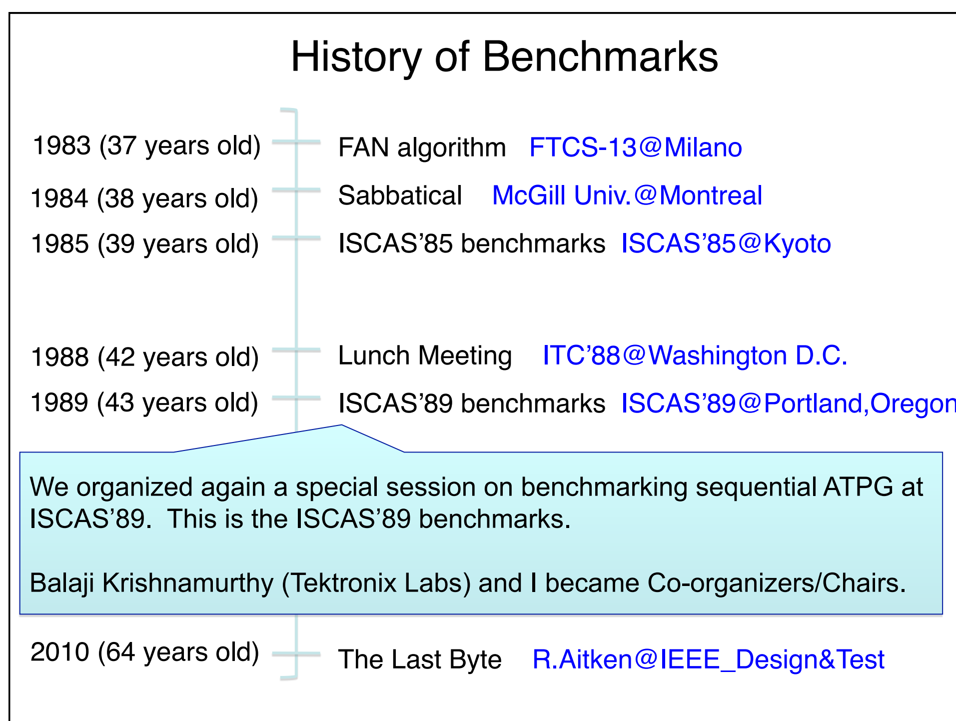
File order on tape:

```
FORISCAS FORTRAN
FORISCAS EXEC
C17      ISCAS
C432     ISCAS
C499     ISCAS
C880     ISCAS
C1355    ISCAS
C1908    ISCAS
C2670    ISCAS
C3540    ISCAS
C5315    ISCAS
C6288    ISCAS
C7552    ISCAS
```

Tape terminated with 5 write marks

60


Three years after ISCAS'85, the following people had a meeting at ITC'88 in Washington D.C. to discuss about the necessity of benchmarks for sequential circuits.
Franc Brglez (MCNC, Microelectronics Center of North Carolina)
Vishwani Agrawal (AT&T Bell Labs)
Balaji Krishnamurthy (Tektronix Labs)
Hideo Fujiwara (Meiji Univ.)
1983 (37
1984 (38
1985 (39
1988 (42 years old) Lunch Meeting ITC'88@Washington D.C.
1989 (43 years old) ISCAS'89 benchmarks ISCAS'89@Portland,Oregon
1998 (52 years old) The Last Byte H.Fujiwara@IEEE_Design&Test
1999 (53 years old) ITC'99 benchmarks ITC'99@Atlantic City, NJ
2010 (64 years old) The Last Byte R.Aitken@IEEE_Design&Test


History of Benchmarks
1983 (37 years old) FAN algorithm FTCS-13@Milano
1984 (38 years old) Sabbatical McGill Univ.@Montreal
1985 (39 years old) ISCAS'85 benchmarks ISCAS'85@Kyoto
1988 (42 years old) Lunch Meeting ITC'88@Washington D.C.
1989 (43 years old) ISCAS'89 benchmarks ISCAS'89@Portland,Oregon
We organized again a special session on benchmarking sequential ATPG at ISCAS'89. This is the ISCAS'89 benchmarks.
Balaji Krishnamurthy (Tektronix Labs) and I became Co-organizers/Chairs.
2010 (64 years old) The Last Byte R.Aitken@IEEE_Design&Test

ISCAS - 89
Benchmarks for Sequential Test Generation
Names and Addresses

People who cooperated in collecting benchmarks

Balaji Krishnamurthy
(Chairman)
Tektronix Labs
Tektronix
PO Box 500, MS 50-662
Beaverton, OR 97077
(503) 627-6191

Hideo Fujiwara
(Co-Chairman)
Dept. of Electronics & Comm.
Meiji University
10101 Higashi-mita, Tama-ku
Kawasaki 214, Japan

Franc Brglez
MCNC
PO Box 12889
Research Triangle Park, NC 27709-2889
(919) 248-1800

Vishwani Agrawal
AT&T Bell Labs
600 Mountain Avenue
Room 2c-476
Murray Hill, NJ 07974
(201) 582-4349

Ralph Marlett
HHB Systems
1000 Wyckoff Avenue
Mahwah, NJ 07430
(201) 848-8000

T. Sridhar
Gateway Automation
Two Lowell Research Center Drive, Ste. 300
Lowell, MA 01852-4995
(508) 458-1900

Antonio Lioy
Politecnico di Torino
Dip. Automatica e Informatica
corso Duca degli Abruzzi 24
10129 Torino, ITALY
39-11-556-7011

Scott Davidson
AT&T Eng. Research Center
PO Box 900
Princeton, NJ 08540
(609) 639-2289

Terumine Hayashi
Hitachi Research Laboratory
The 3rd Dept.
4026 Kuji-cho, Hitachi-shi
Ibaraki-ken, 319-12
Japan
0294-52-5111

63

ISCAS'89

1989 International Symposium on Circuits and Systems
1989 Portland, Oregon

Special Session: Benchmarks for Sequential Test Generation
Chairs: B. Krishnamurthy
Tektronix Labs
Beaverton, OR

H. Fujiwara
Meiji University
Kawasaki, Japan

Chairs: B. Krishnamurthy, H. Fujiwara

1. **Combinational Profiles of Sequential Benchmark Circuits,** F. Brglez, D. Bryan and K. Kozminski, *MCNC, Research Triangle Park, NC.*
2. **A Concurrent Test Generator [...] Testing,** V. Agrawal and K-T. Cheng, *AT[...]*
3. **Sequential Circuit Test Generator (ST[...] [...]ark Results,** S. Davidson and W-T. Cheng, *A[...] Engineering Research Center, Princeton, NJ.*
4. **Two Test Generation Methods for Sequential Circuits,** T. Hayashi, *Hitachi Research Laboratory, Ibaraki-ken, Japan.*
5. **The Complexity of Sequential ATPG,** A. Lioy, *Politecnico di Torino, Torino, Italy.*
6. **The Coupling of Sequential ATG with Partial Scan,** R. Marlett, *HHB Systems, Mahwah, NJ.*
7. **Benchmarking Results for a Sequential ATPG Program,** T. Sridhar, *Gateway Automation, Lowell, MA.*

T. Hayashi, Hitachi Research Laboratory

64

History of Benchmarks

1983 (37 ye

1984 (38 ye

1985 (39 ye

1988 (42 ye

1989 (43 ye

ISCAS'85 benchmarks is considered to be the first generation of ATPG benchmarks and ISCAS'89 benchmarks is the second generation. After those two benchmarks, the size of circuits under test generation had increased drastically.
I wrote a short column in IEEE Design and Test of Computers, to bring up a question on the necessity of the third generation of ATPG benchmarks. (H. Fujiwara、"Needed, Third-generation ATPG benchmarks", The Last Byte, IEEE Design & Test of Computers, p.96, 1998.)

on

1998 (52 years old) — The Last Byte H.Fujiwara@IEEE_Design&Test

1999 (53 years old) — ITC'99 benchmarks ITC'99@Atlantic City, NJ

2010 (64 years old) — The Last Byte R.Aitken@IEEE_Design&Test

THE LAST BYTE

Scott Davidson; scott.davidson@eng.sun.com

Needed: Third-generation ATPG benchmarks

96 — 0740-7475/98/$10.00 © 1998 IEEE — IEEE DESIGN & TEST OF COMPUTERS

66

In 1983 I published the FAN algorithm, and by using actual combinational circuits, showed its superiority over both the D-algorithm (by J.P. Roth) and the PODEM algorithm (by P. Goel). In 1984 I discussed ATPG (automatic test pattern generation) benchmarking with Franc Brglez (then with Bell Northern Research and now with North Carolina State University) while I was on sabbatical visiting Vinod Agarwal at McGill University.

Before this, we had no benchmarks for ATPG algorithms. Brglez and I agreed that benchmark circuits helped advance ATPG algorithm research and development. We organized a special session on combinational ATPG benchmarking at ISCAS 85 (the 1985 International Symposium on Circuits and Systems) in Kyoto, Japan. With the cooperation of many people from industry and universities in the USA, Canada, Europe, and Japan, we collected excellent benchmarks with various and useful characteristics.

Later, others reported many better, more-efficient ATPG algorithms for combinational circuits. The widespread availability of these benchmarks drove the development of new algorithms, as researchers strove to generate the best-known results in terms of runtime, vector length, and fault coverage.

tical computation time.

The current benchmarks are described in a simple netlist format. Future benchmarks should be available at the behavioral, register-transfer, and gate levels. They should be described in a high-level language such as VHDL to facilitate research on high-level ATPG.

Today, new benchmarks are required again. The existing ISCAS 85/89 benchmarks are no longer close to the size of industrial designs. We need much larger circuits (perhaps several million gates) to realistically study ATPG efficiency. We need circuits with features found in modern designs and not found in the current benchmarks. We encourage the development of advanced ATPG algorithms that can achieve almost 100% fault efficiency for very large, realistic circuits within prac-

The ISCAS 85 benchmarks were first-generation benchmarks for ATPG algorithms, and the ISCAS 89 benchmarks were the second generation. We now need a third generation to tackle urgent current issues and continue to stimulate research on solutions for future issues. Perhaps the solutions to the impossible challenges of today, when represented in third-generation benchmarks, will become the new products of tomorrow.

History of Benchmarks

1983 (37 years old) — FAN algorithm FTCS-13@Milano

1984 (38 years old) — Sabbatical McGill Univ.@Montreal

1985 (39 years old) — ISCAS'85 benchmarks ISCAS'85@Kyoto

1988 (42 yea

1989 (43 yea ... egon

Scott Davidson, the editor of the Last Byte, organized a special session on benchmarking ATPG with new benchmark circuits, at ITC'99. This is ITC'99 benchmarks.

1998 (52 years old) — The ...st Byte H.Fujiwara@IEEE_Design&Test

1999 (53 years old) — ITC'99 benchmarks ITC'99@Atlantic City, NJ

2010 (64 years old) — The Last Byte R.Aitken@IEEE_Design&Test

History of Benchmarks

1983 (37 years old) — FAN algorithm FTCS-13@Milano

1984 (38 years old) — Sabbatical McGill Univ.@Montreal

1985 (39 years old) — ISCAS'85 benchmarks ISCAS'85@Kyoto

1988 (42 years old) — Lu

1989 (43 years old) — IS egon

1998 (52 years old) — The Last ujiwara@IEEE_Design&Test

1999 (53 years old) — ITC'99 be arks ITC'99@Atlantic City, NJ

2010 (64 years old) — The Last Byte R.Aitken@IEEE_Design&Test

Last year when a quarter of a century has passed since ISCAS'85 benchmarks, an interesting column appeared in the Last Byte of IEEE Design & Test.

The Last Byte

Time to retire our benchmarks

Rob Aitken
ARM

On a June day 25 years ago, Franc Brglez and Hideo Fujiwara forever changed the world of design and test of computers. On that day, they distributed copies of a tape containing 10 sample circuits, with ortran parser, to a group of attendees at a special sion on ATPG at the International Symposium for cuits and Systems. The ISCAS85 benchmarks, as y quickly became known, have been used by gen- tions of students and written up in thousands of pers—in ATPG of course, but also for logic synthe- , place and route, and who knows what else. Every- e who has worked with them knows that, like figure ISCAS benchmarks have individual also like the occasional figure skat- ht manipulate a score, sometimes a e in to the temptation to manipu- Papers describing algorithms that dom-untestable circuits—circuits m set of patterns applied to them verage—are likely to have C2670 . Methods that fail on large designs 0, or C1908, or even C432. There's n stepchild, C17, by and large ignored in favor of its better known relatives.

On a June day 25 years ago, Franc Brglez and Hideo Fujiwara forever changed the world of design and test of computers. ……

……. The ISCAS85 benchmarks

Rob Aitken is an R&D Fellow at ARM, San Jose, California. Contact him at rob.aitken@arm.com.

Yet, despite their astounding and undeniable success, as we approach the benchmarks' silver anniversary, I would like to suggest that it is time for them to retire. Consider: in 1985, C7552 was a substantial circuit, containing more than ... and consuming enough area to ...
In 2010, however, ev...
bined (13,258 gate...
1/200th of a square...
about a quarter of t...
of this sentence. Th...
circuits are older than many current masters degree students. How many students in 1985 would have wanted a set of benchmark circuits from 1960? The benchmarks (mostly arithmetic circuits) predate logic synthesis, and contain ... power
networks, I/O p...
other troubleso...

What's out there to replace them? The ISCAS89 circuits are also coming up on retirement age, but the ITC99 circuits have plenty of life left in them. There are also some open source RTL processors and the like out there. You might ask: But aren't these too big? Isn't a virtue of the ISCAS85 circuits the fact that academic methods can be demonstrated on some small circuits and then generalized by industrial practitioners later? This was not the case in 1985—the benchmarks

algorithm will survive when ramped up to industrial scale. This uncertainty creates a growing divide between the problems (and solutions) of academic interest and those solutions that succeed commercially. The benchmarks have served the world well, but, like mul-
...as passed.
...oast. To the
...ccessful set
...story. ■

Yet, despite their astounding and undeniable success,
as we approach the benchmarks' silver anniversary,
I would like to suggest that it is time for them to retire.

How many students in 1985 would have wanted
a set of benchmark circuits from 1960?

71

Yet, despite their astounding and undeniable success, as we approach the benchmarks' silver anniversary, I would like to suggest that it is time for them to retire. Consider: in 1985, C7552 was a substantial circuit, containing more than 3,500 gates and consuming enough area to make a reasonably sized chip. In 2010, however, even with all 10 benchmarks combined (13,258 gates), this corresponds to about
1/200th...
about...
of this...
circuits...
studen...
wanted...
bench...
logic s...
networks, I/O pads, tristate circuitry, or any of the other troublesome features of modern design.

What's out there to replace them? The ISCAS89 circuits are also coming up on retirement age, but the ITC99 circuits have plenty of life left in them. There are also some open source RTL processors and the like out there. You might ask: But aren't these too big? Isn't a virtue of the ISCAS85 circuits the fact that academic methods can be demonstrated on some small circuits and then generalized by industrial practitioners later? This was not the case in 1985—the benchmarks were so large that they broke most academic systems (certainly a couple of mine!). The size argument emerged in the 1990s and was somewhat valid then,
...l ATPG programs
...s really no way to
...esults, whether an
...d up to industrial
...owing divide be-
...of academic inter-
...commercially. The
...vell, but, like mul-
lets, ...nd VCRs, their time has passed.

So, I'm asking you to join me in a toast. To the ISCAS85 benchmarks, a wonderfully successful set of circuits: may they pass quietly into history. ■

So, I'm asking you to join me in a toast.
To the ISCAS85 benchmarks,
a wonderfully successful set of circuits:
may they pass quietly into history.

72

“Time to retire our benchmarks”

-- Rob Aitken, 2010

73

“Time to retire our benchmarks”

-- Rob Aitken, 2010

“Time to retire Fujiwara”

-- Hideo Fujiwara, 2011

74

Thanks to

a lot of wonderful encounters,

I was able to enjoy taking part in the history of

test generation algorithms and benchmarks with

such dear and happy memories.

In my life from now on,

I would like to continue

treasuring every encounter with people.

Lastly,

I very much appreciate all the kindness

you have shown me so far.

Thank you very much!