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PAPER

Defect Level vs. Yield and Fault Coverage in the Presence of an Unreliable BIST

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SUMMARY Built-in self-test (BIST) hardware is included today in many chips. This hardware is used to test the chip's functional circuits. Since this BIST hardware is manufactured using the same technology as the functional circuits themselves, it is possible for it to be faulty. It is important, therefore, to assess the impact of this unreliable BIST on the product defect level after test. Williams and Brown's formula, relating the product defect level as a function of the manufacturing yield and fault coverage, is re-examined in this paper. In particular, special attention is given to the influence of an unreliable BIST on this relationship. We show that when the BIST hardware is used to screen the functional product, an unreliable BIST circuitry tends, in many cases, to reduce the effective fault coverage and increase the corresponding product defect level. The BIST unreliability impact is assessed for both early life phase, and product maturity phase.

key words: *BIST, fault coverage, defect level*

1. Introduction

Design for testability (DFT) has been a major area of research and practice for the last 40 years. This has emerged after many digital systems manufacturers have realized that test can no longer be an "after-thought".

Computer and semiconductor manufacturers have changed their design practices to incorporate test as an integral part of their design cycle. Strict coverage requirements have been put in place before tape-out stage. Coverage requirements in the high ninety percent against single stuck-at faults are quite common today. In order to reach this goal, two major DFT methodologies have been adopted: scan design and built-in self-test (BIST).

Even though scan design [1]–[3] has greatly alleviated the test process, it did not bring the test generation time and the test data file down to acceptable levels. The breakthrough in this domain has been achieved through BIST. BIST may come in many different flavors. There are BIST designs that rest on *exhaustive* or *pseudo-exhaustive* patterns, that use functional patterns (mostly for off the shelf products where there is no knowledge of the design details), and there are BIST designs that use *pseudo-random* patterns [3]. Pseudo-random BIST designs are the most widely used due to their relative simplicity and low cost. They also enjoy the added benefit of potentially detecting many unmodeled defects, and therefore achieving a higher shipped-quality level.

In pseudo-random-based BIST designs, the patterns are generated by a *linear feedback shift register* (LFSR) and the test responses are compressed in a *multiple-input signature register* (MISR). At the end of the test, the MISR contains a short signature (typically 16-64 bits) of the entire test history. The good machine signature is computed beforehand for reference during test. A product is declared fault-free if the measured signature coincides with the reference signature. A circuit is declared faulty if these two signatures differ from one another.

All BIST-based methodologies, without exception, are subject to what is called *masking*, or *aliasing*, a phenomenon of having a faulty product end up with a measured signature that equals the fault-free signature. This phenomenon is inevitable because all BIST-based methodologies *lose* test information during the data compression process. The question is how much loss in test quality is encountered using BIST. In pseudo-random-based BIST designs the probability of aliasing is approximately 2^{-n}, where n is the number of stages in the MISR. Thus, the probability of aliasing is negligible for $n \geq 16$, for which it is already below 0.1%. The attainable fault coverage in BIST-based designs is a function of the test length. The higher the test length the higher is the fault coverage.

Williams and Brown [4] had shown the relationship between the product defect level, the manufacturing yield, and the fault coverage of the test process used to screen it into either a *good* lot or a *bad* lot. This well-known relationship is derived assuming that the test equipment is fault-free.

Many chips today have BIST circuitry in them. These BIST circuits are used to test the chips and perform the screening described above. Since the BIST hardware is manufactured using the same technology and process as the functional circuits, it is unrealistic to assume that it is fault-free. Moreover, chip manufacturers do not insert any redundancy into their BIST hardware in order to keep the cost down. As a result, the BIST hardware is not made to be fault-tolerant. It is, therefore, imperative to allow the BIST hardware be subjected (during the analysis) to the same defect density as the functional circuits themselves. It is the subject of this paper to investigate the effects of an unreliable (possibly faulty) BIST environment on the Williams and Brown's equation.

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For the context of this paper we use the following definition:

Definition: BIST circuitry is said to be *unreliable* if

Pr{BIST is faulty}>0 □

Consequently, BIST circuitry is considered reliable if Pr{BIST is faulty}=0 .

Generally speaking, there are two side effects resulting from an unreliable BIST. One side effect is to cause a good product (i.e. no functional defects present) be declared faulty, resulting in a yield loss [5]–[7]. A second side effect is to have a bad product be passed as good, increasing the shipped-product defect level.

In [5], [6] the effects of an unreliable tester on the resulting yield during a delay (AC) test is discussed. Modeling of yield loss is discussed in [7]. In [8], [9] a more generalized fault probability model is introduced to re-examine the Williams and Brown's defect vs. yield equation. Poisson's probability model is used in [8] along with a weighting scheme biased towards faults that are more likely to occur. The authors of [8] show that the Williams and Brown's equation still holds. A non-uniform fault probability model is introduced in [9]. In [10] a defect level model for other fault types (delay faults and stuck-open faults) as a function of yield and fault coverage is proposed. The authors in [10] show that the relationship between defect level, fault coverage and yield, depicted in [4], still holds. However, [8]–[10] still assume that the test equipment is fault-free.

This paper is organized as follows. Section 2 is a brief review of Williams and Brown's formula. Section 3 derives the yield equation in BISTed products with unreliable BIST circuitry. We show that the Williams and Brown's equation is a special case of our more generalized formula, i.e. our new formula reduces to Williams and Brown's in the absence of BIST circuitry. Section 4 discusses the properties of the newly derived formulas by displaying the graphs of some typical case studies. The case studies involve both an early life phase, and a product maturity phase. Section 5 draws some conclusions from this analysis.

2. Recapitulation of Williams and Brown's Equation

Let the circuit under test (CUT) have n_c possible faults, each having the same probability of occurrence, p. The yield, Y, is the probability that the circuit is fault-free, i.e.

$$Y = (1-p)^{n_c}. \tag{1}$$

The raw defect level of the product coming out of the manufacturing line (without any test) is

$$D_0 = 1 - Y = 1 - (1-p)^{n_c}. \tag{2}$$

Assuming that the test process can detect m out of the n_c possible faults, the fault coverage is given by[†]

$$F = \frac{m}{n_c}. \tag{3}$$

A circuit that passes the test is guaranteed to be free of any covered faults (m in total), but can still possess an uncovered fault that escaped the test. Since there are $n_c - m$ uncovered faults, the defect level after test is given by

$$D = 1 - (1-p)^{n_c - m}, \tag{4}$$

which can be further reduced to

$$D = 1 - [(1-p)^{n_c}]^{(1-\frac{m}{n_c})} = 1 - Y^{1-F}. \tag{5}$$

Thus, this equation assumes that the test process is *fault-free,* i.e. a circuit being declared by the test process to be faulty is *truly faulty*. This is the underlying assumption in the derivation of this formula.

3. Enhanced Equation in the Presence of an Unreliable BIST

3.1 Fault Detection Scenarios in the Presence of an Unreliable BIST

The BIST hardware tests the CUT in order to determine whether it is faulty or fault-free. The BIST hardware is an entity residing on chip and is separate from the CUT. If the BIST hardware happens to be fault-free, the outcome of the test will depend on its fault coverage against functional faults, which the Williams and Brown's equations already accounts for.

If the BIST circuitry is faulty, the outcome of the test will also depend upon the ability of the impaired BIST to detect CUT faults on one hand, and its ability not to "accuse" a fault-free CUT as being faulty, on the other. As a result, the test may encounter both fault escapes [3] and yield loss[††] [5]–[7]. Notice that in the Williams and Brown's case a yield loss is not possible. Table 1 displays all the possible test outcomes in the presence of an unreliable BIST hardware. The assumption in Table 1 is that BIST faults do not affect the functional operation of the CUT.

In this section we derive a new set of formulas that cover the case where there is no knowledge prior to the launch of the CUT test as to the state of the BIST hardware. This uncertainty as to whether or not the BIST hardware is faulty or fault-free is likely to cause an increase in the shipped-product defect level. This increment in defect level is later analyzed based upon our newly derived formulas.

3.2 The Enhanced Equations

In the sequel we will refer to the product functional circuits as the CUT. We use the following parameters in our analysis:

D - Product defect level after test under fault-free BIST hardware

D' - Product defect level after test under unreliable BIST hardware

[†]Note: Fault detection is independent of fault occurrence.

[††]Note: Yield loss is the probability that the fault-free circuit fails the test.

Table 1 Test outcomes in the presence of an unreliable BIST.

CUT	BIST	Test Result	CUT Fault Condition
Fault-free	Fault-free	Pass	No fault. Case covered by Williams and Brown.
Faulty	Fault-free	Pass	Fault escapes. Case covered by Williams and Brown.
		Fail	Fault detected. Case covered by Williams and Brown.
Fault-free	Faulty	Pass	No fault.
		Fail	No fault. Case of yield loss.
Faulty	Faulty	Pass	Fault escapes.
		Fail	Fault detected.

F - Fault coverage of the CUT under fault-free BIST hardware

F' - Effective fault coverage of the CUT in the presence of an unreliable BIST hardware

Y - Product yield

p - Fault occurrence probability in both CUT and BIST hardware

A_c - CUT area

A_b - BIST area

n_c - Total number of possible faults in the CUT, $n_c = GA_c$, where G is a constant.

n_b - Total number of possible faults in the BIST hardware, $n_b = GA_b$, where G is a constant.

m - Number of CUT faults covered by fault-free BIST hardware

m' - Expected number of CUT faults covered by an unreliable BIST hardware

k - Average number of CUT faults covered by a faulty BIST hardware

α - Ratio between BIST area and CUT area

ρ - Fault coverage alteration factor

The meaning of α and ρ will become evident from the following analysis.

Notice that we are allowing the test procedure, as conducted by the faulty BIST hardware, to detect CUT faults. The number of CUT faults detected by a faulty BIST depends upon the type of fault actually existing in the BIST hardware. Let k_{f_i} $(0 \le k_{f_i} \le n_c)$ be the number of detected CUT faults[†] in the presence of BIST fault f_i $(1 \le i \le n_b)$. Further denote by k the average number of all such k_{f_i}s.

We proceed to calculate m', the expected number of CUT faults covered by the unreliable BIST.

$$m' = m \times \Pr\{\textit{Fault-free BIST}\}$$

$$+k \times \Pr\{\textit{Faulty BIST}\}$$

Therefore,

$$m' = m(1-p)^{n_b} + k[1-(1-p)^{n_b}]. \tag{6}$$

The expected CUT fault coverage, as conducted by the BIST circuitry, is:

$$F' = \frac{m'}{n_c} = \frac{m}{n_c}(1-p)^{n_b} + \frac{k}{n_c}[1-(1-p)^{n_b}]$$

$$= \frac{m}{n_c}\{(1-p)^{n_b} + \frac{k}{m}[1-(1-p)^{n_b}]\}.$$

Define:

$$\rho = \frac{k}{m} \tag{7}$$

to be the *fault coverage alteration factor*. Notice that ρ can be larger than 1. The reason for this is that it is possible for a BIST fault to create a situation where every CUT, good or bad, is rejected by the test. We refer to this case as a *catastrophic* case. Thus, the largest ρ may become is $n_c/m = 1/F$. The possible range for ρ is, therefore, $0 \le \rho \le 1/F$. Notice also that the case of $\rho > 1$ is actually a case of fault coverage "amplification" rather than a case of fault coverage reduction. We can rewrite the expected CUT fault coverage, as exercised by the unreliable BIST, as:

$$F' = F\{(1-p)^{n_b} + \rho[1-(1-p)^{n_b}]\}. \tag{8}$$

We call this expected CUT fault coverage the *effective CUT fault coverage* in the presence of the unreliable BIST.

Eq. (8) can also be written as:

$$F' = F\left[Y^{\frac{n_b}{n_c}} + \rho(1-Y^{\frac{n_b}{n_c}})\right]. \tag{9}$$

Denote by $\alpha = n_b/n_c = GA_b/GA_c = A_b/A_c$ (see relationship in list of parameters earlier in this section).

The effective fault coverage, F', can now be written as

$$F' = F[Y^{\alpha} + \rho(1-Y^{\alpha})]. \tag{10}$$

The new formula relating the product defect level to the yield and the effective fault coverage becomes:

$$D' = 1-(1-p)^{n_c-m'} = 1-(1-p)^{n_c\left(1-\frac{m'}{n_c}\right)}.$$

Notice that D' behaves similar to D (see Eq. 4), with the exception of the replacement of m by m'. This leads to:

$$D' = 1-Y^{1-F'}. \tag{11}$$

Example 1: Consider a chip manufacturing line with 90% yield. The chips are screened using their BIST circuitry. The BIST circuitry constitutes 5% of the entire chip area. The BIST procedure has 95% coverage of the functional faults when assumed to be fault-free, and only 40% coverage when assumed faulty. Compute the chip defect level after its BIST screening.

Solution: We have the following parameters:

$$\alpha = \frac{5}{95} = \frac{1}{19} = 5.263 \times 10^{-2}$$

[†]Note: A catastrophic BIST fault will end up rejecting all CUTs, good or bad, resulting in $k_{f_i} = n_c$.

$$\rho = \frac{40}{95} \approx 0.4211$$

$$F' = 0.95 \times [0.9^{5.263\times10^{-2}}$$

$$+0.4211 \times (1 - 0.9^{5.263\times10^{-2}})]$$

$$\approx 0.9470$$

$$D' \approx 1 - 0.9^{1-0.9470} \approx 1 - 0.9^{0.053} \approx 5.569 \times 10^{-3}$$

$$\approx 5569\, ppm$$

Notice that if we ignore the effects of the BIST, the defect level is:

$$D = 1 - 0.9^{1-0.95} = 1 - 0.9^{0.05} \approx 5.254 \times 10^{-3}$$

$$\approx 5254\, ppm$$

□

It is interesting to take note of the following special cases:

1. If there is no BIST circuitry ($\alpha = 0$), we have $F' = F$, and $D' = D$. This is the Williams and Brown's case.
2. If there is no CUT fault coverage alteration by the BIST circuitry ($\rho = 1$), we have $F' = F$, and $D' = D$. This is, again, the Williams and Brown's case.
3. If the BIST procedure has zero coverage against functional faults while being itself faulty, then $\rho = 0$. The effective fault coverage, in this case, reduces to:

$$F' = FY^{\alpha}. \tag{12}$$

4. For the extreme case of $\rho = 1/F$ we get:

$$F' = 1 - (1 - F)Y^{\alpha}. \tag{13}$$

The impact of the BIST impurity on the product defect level can be best measured by the differential $\Delta D = D' - D$, or, even better, by its normalized form, $\Delta D/D$. When a product manufacturing process reaches maturity, its yield is close to 1, and its defect level is close to 0 ($Y \approx 1$, $D \approx 0$). By using calculus approximation techniques, and under the restrictions just described,ΔD and $\Delta D/D$ can be approximated as follows.

$$D' = 1 - Y^{1-F'} = 1 - \left(Y^{1-F}\right)^{\frac{1-F'}{1-F}} = 1 - (1-D)^{\frac{1-F'}{1-F}}. \tag{14}$$

But since for this case $D \approx 0$, Eq. 14 can be approximated as:

$$D' \approx 1 - \left(1 - \frac{1 - F'}{1 - F}D\right) = \frac{1 - F'}{1 - F}D. \tag{15}$$

From Eqs. 10 and 15 we get:

$$\frac{\Delta D}{D} \approx \frac{F - F'}{1 - F} = \frac{F(1 - \rho)(1 - Y^{\alpha})}{1 - F}, \tag{16}$$

and since for $Y \approx 1$ we can approximate

$$1 - Y^{\alpha} = 1 - [1 - (1 - Y)]^{\alpha} \approx \alpha(1 - Y), \tag{17}$$

then, Eq. 16, for the case where $Y \approx 1$, can be further approximated as:

$$\frac{\Delta D}{D} \approx \frac{F\alpha(1 - \rho)(1 - Y)}{1 - F}. \tag{18}$$

From Eq. 5, and for $Y \approx 1$, we get:

$$D = 1 - Y^{1-F} = 1 - [1 - (1 - Y)]^{1-F}$$

$$\approx (1 - Y)(1 - F). \tag{19}$$

From Eqs.18 and 19 we get:

$$\Delta D \approx F\alpha(1 - \rho)(1 - Y)^2. \tag{20}$$

Example 2: Consider again the case described in Ex. 1. By using Eqs.19 and 20 we get:

$$\Delta D \approx 0.95\times5.263\times10^{-2}\times(1-0.4211)\times(1-0.9)^2$$

$$\approx 289\, ppm$$

$$\frac{\Delta D}{D} \approx \frac{0.95\times5.263\times10^{-2}\times(1-0.4211)\times(1-0.9)}{1-0.95}$$

$$\approx 5.789 \times 10^{-2}$$

Compare these to the exact results of $315\, ppm$ and 5.995×10^{-2} respectively, derived from Ex. 1. □

It is interesting to see what will the $\Delta D/D$ be in the extreme case of $\rho = 1/F$. From Eq 18 we get:

$$\frac{\Delta D}{D} \approx -\alpha(1 - Y). \tag{21}$$

4. Some Typical Behavior

During the product's early life its yield is relatively low. This is mostly due to not quite knowing how to best fine-tune the manufacturing parameters of an emerging new technology. Typical early life yields may vary between 40% to 60%, even though lower figures are also possible. As the manufacturing process matures, the yield figures may rise to as much as 90%, or even higher. In this section we try to shed some light on the impact of the BIST unreliability during these two distinct periods of the product's life. The parameters chosen in this study reflect likely operating conditions of an IC manufacturing fab.

4.1 Early Life Impact

In order to study the impact of the BIST circuitry on the product's early life defect level after test, we let $0.4 \le Y \le 0.6$. The other parameter ranges are $0.9 \le F \le 0.99$, $0.4 \le \rho \le 1.1$, and $0.05 \le \alpha \le 0.1$. These parameter ranges are used again in the next subsection, and they reflect practical values for BIST-based IC products.

In Fig. 1 we show the behavior of F'/F and $\Delta D/D$ as a function of Y, while keeping the other parameters fixed at

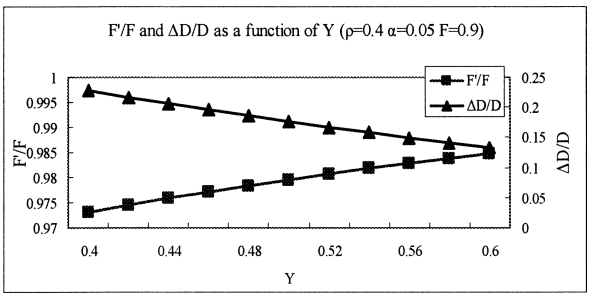

Fig. 1 F'/F and $\Delta D/D$ as a function of Y.

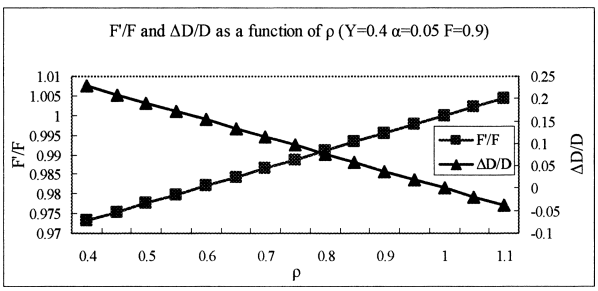

Fig. 2 F'/F and $\Delta D/D$ as a function of ρ.

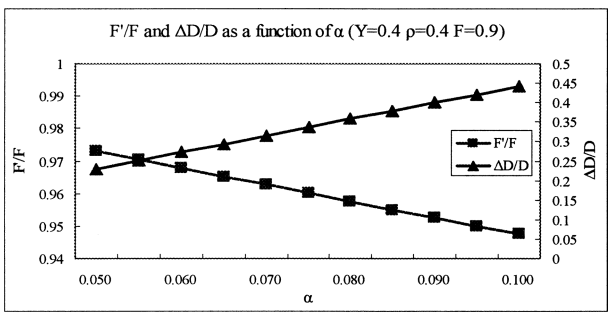

Fig. 3 F'/F and $\Delta D/D$ as a function of α.

$F = 0.9, \rho = 0.4$, and $\alpha = 0.05$.

In Fig. 2 we show the behavior of F'/F and $\Delta D/D$ as a function of ρ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.4$, and $\alpha = 0.05$.

In Fig. 3 we show the behavior of F'/F and $\Delta D/D$ as a function of α, while keeping the other parameters fixed at $F = 0.9, \rho = 0.4$, and $Y = 0.4$.

In Fig. 4 we show the behavior of F'/F and $\Delta D/D$ as a function of F, while keeping the other parameters fixed at $Y = 0.4, \rho = 0.4$, and $\alpha = 0.05$.

4.2 Impact at Maturity

Since at maturity $Y \approx 1$, we plot F'/F and $\Delta D/D$ for the parameter ranges $0.9 \leq Y \leq 0.95$, $0.9 \leq F \leq 0.99$, $0.4 \leq \rho \leq 1.1$, and $0.05 \leq \alpha \leq 0.1$.

In Fig. 5 we show the behavior of F'/F and $\Delta D/D$ as a function of Y, while keeping the other parameters fixed at $F = 0.9, \rho = 0.4$, and $\alpha = 0.05$.

In Fig. 6 we show the behavior of F'/F and $\Delta D/D$ as a function of ρ, while keeping the other parameters fixed at $F = 0.9, Y = 0.9$, and $\alpha = 0.05$.

In Fig. 7 we show the behavior of F'/F and $\Delta D/D$ as a function of α, while keeping the other parameters fixed at $F = 0.9, \rho = 0.4$, and $Y = 0.9$.

In Fig. 8 we show the behavior of F'/F and $\Delta D/D$ as a function of F, while keeping the other parameters fixed at

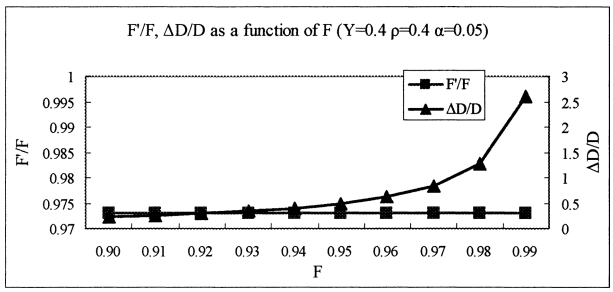

Fig. 4 F'/F and $\Delta D/D$ as a function of F.

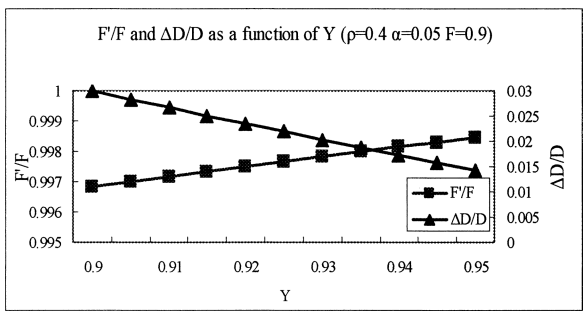

Fig. 5 F'/F and $\Delta D/D$ as a function of Y.

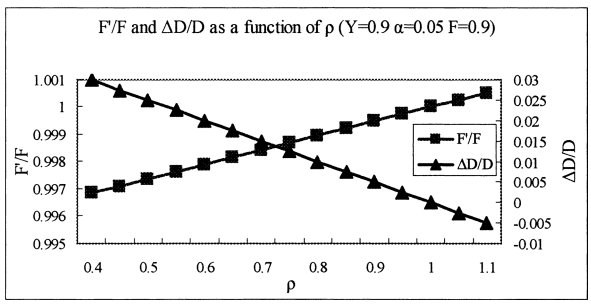

Fig. 6 F'/F and $\Delta D/D$ as a function of ρ.

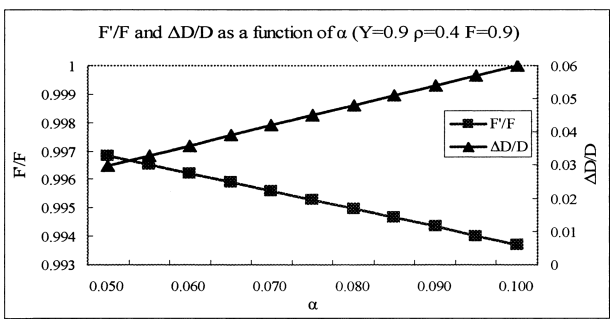

Fig. 7 F'/F and $\Delta D/D$ as a function of α.

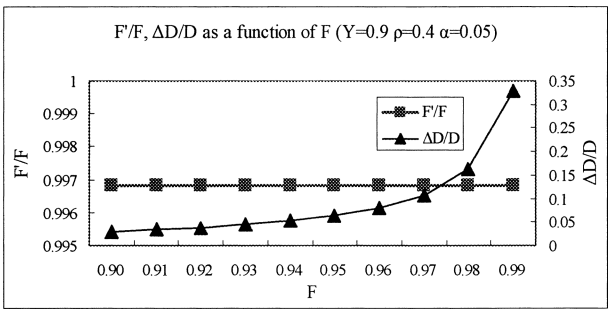

Fig. 8 F'/F and $\Delta D/D$ as a function of F.

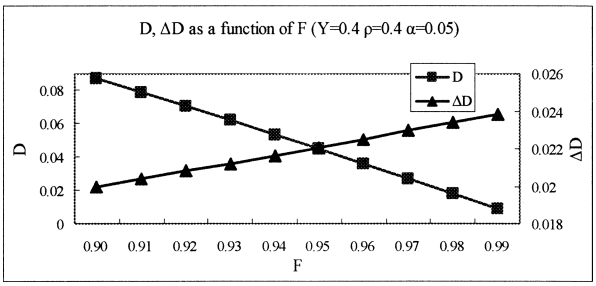

Fig. 9 D and ΔD as a function of F.

$Y = 0.9$, $\rho = 0.4$, and $\alpha = 0.05$.

4.3 The Impact Trend

At maturity, and for fault coverages under 98%, the impact of the BIST circuitry unreliability is mostly minor. In this case, the drop in fault coverage, and the defect level increment, rising from the presence of an unreliable BIST circuitry, is relatively small (few percent). During early life, on the other hand, the impact of the BIST circuitry unreliability is far more significant. Even for fault coverages around, or under, 98%, the defect level increment can easily exceed 100%.

It is important to note that regardless of which stage in life the product is in, when F is very close to 1 (say $F = 0.99$), the ΔD differential starts to grow substantially faster (see trend in Figs. 4 & 8). The reason for this phenomenon is that in this range of fault coverages D is already very small, and the impact of the unreliable BIST makes D' so much worse compared to D. Since $\Delta D = D' - D$, this differential worsens when F approaches 0.99 (see Fig. 9). The behavior of $\Delta D/D$ is even more pronounced since ΔD is increasing while D is decreasing. In these range of fault coverages, therefore, there is a very significant departure from the Williams and Browns' results.

5. Conclusions

This paper extends Williams and Brown's formula for products with BIST hardware, where the screening into pass/fail lots is done by the BIST hardware itself. The BIST hardware is assumed to suffer from the same defect density as the functional circuits themselves. The impact of this unreliable BIST is studied in detail. We have shown that the general form of Williams and Brown's formula still holds in this case, provided the CUT's fault coverage is replaced by the CUT's *effective fault coverage*. If the BIST circuitry does not possess a catastrophic fault, its impact is to increase the defect level of the products passing the test procedure. If the BIST does possess a catastrophic fault, it may decrease the defect level of the products passing the test procedure. This "artificial" improvement in defect level comes at the expense of having to reject almost every circuit, good or bad, subjected to the test. Formulas to assess these impacts have been derived.

During maturity, and for fault coverages under 98%, the impact of the BIST circuitry unreliability is minor (about a 5% departure). In this case the Williams and Brown's formula constitutes a reasonable approximation even in the presence of an unreliable BIST. For fault coverages above 98%, however, the defect level increment can easily grow by 30-50%. Therefore, the Williams and Brown's formula no longer represents the true situation.

During early life, and even for fault coverages below 98%, we see a considerable departure from the Williams and Brown's results. The departures in defect levels, for example, may be as small as 20% and as high as 150%. These departures worsen for fault coverages above 98%. Thus, the Williams and Brown's formula cannot be used for this stage in the product's life. It is paramount to use our enhanced equations instead.

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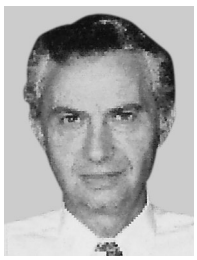

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