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PAPER

Effect of BIST Pretest on IC Defect Level

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SUMMARY In [1] the impact of BIST on the chip defect level after test has been addressed. It was assumed in [1] that no measures are taken to ensure that the BIST circuitry is fault-free before launching the functional test. In this paper we assume that a BIST pretest is first conducted in order to get rid of all chips that fail it. Only chips whose BIST circuitry has passed the pretest are kept, while the rest are discarded. The BIST pretest, however, is assumed to have only a limited coverage against its own faults. This paper studies the product quality improvements as induced by the BIST pretest, and provides some insight as to when it may be worthwhile to perform it.
key words: *BIST, fault coverage, defect level*

1. Introduction

Williams and Brown [2] had shown the relationship between the product defect level, the manufacturing yield, and the fault coverage of the test process used to screen it into either a good lot or a bad lot. This well-known relationship is derived assuming that the test equipment is fault-free.

Many chips today have built-in self-test (BIST) circuitry in them. These BIST circuits are used to test the chips and perform the screening described above. Since the BIST hardware is manufactured using the same technology and process as the functional circuits, it is unrealistic to assume that it is fault-free. Moreover, chip manufacturers do not insert any redundancy into their BIST hardware for the sake of keeping the cost down. As a result, the BIST hardware is not made to be fault-tolerant. It is, therefore, imperative to subject the BIST hardware (during the analysis) to the same defect density as the functional circuits themselves.

Nakamura et al. [1] have derived formulas to assess the impact of the BIST circuitry on the final integrated circuit (IC) defect level after test. The authors in [1] assume that no measures are taken to ensure that the BIST circuitry is, in fact, working properly before the initiation of the functional test. The formulas derived in [1] show a considerable departure from those in [2].

In this paper we assume that a BIST pretest is first conducted in order to get rid of all chips that fail it. Only chips whose BIST circuitry has passed the pretest are kept, while the rest are discarded. The BIST pretest, however, is assumed to have only a limited coverage against its own faults. The reason for this is that only primitive operations, such as scan and capture, are possible during pretest. A more comprehensive BIST pretest will require the use of external test equipment, which defeats the incentive for BIST altogether. Thus, only a subset of chips with faulty BIST can be identified and eliminated. Chips with faulty BIST that escape the pretest are used later on to conduct the functional test*. Generally speaking, therefore, there are two side effects resulting from this BIST pretest. One side effect is to cause a good product (i.e. no functional defects present) to be dropped, resulting in a yield loss. A second side effect is to have a bad product be passed as good by a faulty BIST during the functional test, increasing the shipped-product defect level.

It is important to note that the BIST circuitry is also indirectly tested during the functional test. At this point, however, you cannot separate one from the other. As a result, any conclusion drawn from this test affects the pass/fail decision of the chip at hand. In particular, if the test fails the entire chip is declared faulty and is being discarded, even if it was in fact due to a failure in the BIST circuitry. This is another example of a possible yield loss that might occur.

This paper assumes that all potential faults in either the CUT, or the BIST circuitry, are equally likely to occur. Under this assumption we may employ counting techniques in computing detection probabilities and defect levels. Examples of fault classes that meet this criterion are, for example, the stuck at fault class, the bridging fault class, etc. The results of this paper, therefore, do not directly apply to non-uniform fault probability classes. These cases, however, can still be addressed by adding the different weights associated with the faults, thus extending our newly derived formulas.

Reference [3] is a preliminary version of Ref. [1]. In [4], [5] the effects of an unreliable tester on the resulting yield during a delay (AC) test is discussed. Modeling of yield loss is discussed in [6]. In [7], [8] a more generalized fault probability model is introduced to re-examine Williams and Brown's defect vs. yield equations. Poisson's probability model is used in [7] along with a weighting scheme biased towards faults that are more likely to occur. The authors of [7] show that Williams and Brown's equations still holds. A non-uniform fault probability model is introduced in [8]. In [9] a defect level model for other fault

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*In this paper functional test means a CUT BIST test, to distinguish it from the BIST pretest.

types (delay faults and stuck-open faults) as a function of yield and fault coverage is proposed. The authors in [9] show that the relationship between defect level, fault coverage and yield, depicted in [2], still holds. References [12]–[35] discuss multitude of subjects relating to yield, fault coverage and defect level after test.

This paper is organized as follows. Section 2 is a brief review of the earlier results reported in [1], [2]. Section 3 derives the defect equations in BIST-based products that have undergone both a pretest and a functional test. We show that Williams and Brown's equations [2] and the Nakamura et al.'s equations [1] are special cases of our more generalized formulas. Section 4 discusses the properties of the newly derived formulas by displaying the graphs of some typical case studies. The case studies involve both an early life phase, and a product maturity phase. Section 5 draws some conclusions from this study.

2. Recapitulation of Earlier Results

Let the circuit under test (CUT) have n_c possible faults, each having the same probability of occurrence, p. The yield, Y, is the probability that the circuit is fault-free, i.e.

$$Y = (1-p)^{n_c} \tag{1}$$

The raw defect level of the product coming out of the manufacturing line (without any test) is

$$D_0 = 1 - Y = 1 - (1-p)^{n_c} \tag{2}$$

Williams and Brown [2] analyzed the defect level of the product after test, under the assumption that the test process is fault-free. Assuming that the test process can detect m out of the n_c possible faults, the fault coverage against functional faults is given by

$$F = \frac{m}{n_c} \tag{3}$$

A circuit that passes the test is guaranteed to be free of any covered faults (m in total), but can still possess an uncovered fault that escaped the test. The defect level after test was derived in [2], and is given by

$$D = 1 - Y^{1-F} \tag{4}$$

The work of Williams and Brown was extended in [1] for ICs having BIST circuitry in them. The BIST circuitry is used to test the functional circuits and screen them into either a *good lot* or a *bad lot*. The underlying assumption in [1] was that the BIST circuitry is *unreliable*, i.e. it is possible for the BIST circuitry itself to be faulty. The reason for this assumption is that the BIST circuitry is manufactured using the same technology as the functional circuits themselves, and therefore is subjected to the same process impurity. The effects of using this unreliable BIST circuitry as a test vehicle where analyzed in [1], and are repeated here for the reader's convenience.

The defect level after test in BIST-based products is given by

$$D' = 1 - Y^{1-F'}, \tag{5}$$

where F' is the *effective CUT fault coverage* as conducted by the BIST circuitry, and is given by

$$F' = F[Y^{\alpha} + \rho(1 - Y^{\alpha})]. \tag{6}$$

The parameter α is the ratio between the BIST circuitry area and the area of the CUT. The parameter ρ is the CUT *fault coverage alteration factor*. Notice that ρcan be larger than 1. The reason for this is that it is possible for a BIST fault to create a situation where every CUT, good or bad, is rejected by the test. We refer to this case as a *catastrophic* case. Thus, the largest ρ may become is $n_c/m = 1/F$. The possible range for ρ is, therefore, $0 \le \rho \le 1/F$.

The impact of the BIST impurity on the product defect level can be best measured by the differential $\Delta D' = D' - D$, or, equivalently, by its normalized form, $\Delta D'/D$. When a product manufacturing process reaches maturity, its yield is close to 1. Furthermore, in most real–life cases $F' \approx F$, $\alpha \ll 1$. The normalized surge in product defect level under these conditions is approximately:

$$\frac{\Delta D'}{D} \approx \frac{F\alpha(1-\rho)(1-Y)}{1-F} \tag{7}$$

3. Effects of BIST Pretest

3.1 Analysis

In this case the BIST circuitry undergoes an operation pretest in order to discard of any chips with faulty BIST in them. This pretest, however, is conducted by the BIST circuitry itself, and is far from being comprehensive. In this primitive test, the LFSRs/MISRs are cycled, starting with a known seed, to see if they can end up with a correct signature after a predetermined number of clocks. BIST circuitry that passes this pretest is by no means guaranteed to be fault-free. BIST circuitry that passes this test can still possess, for example, interconnect faults between the LFSRs/MISRs and the CUT. This pretest, therefore, has relatively low fault coverage against its own faults. The reason why a primitive, rather than a comprehensive, pretest is conducted is that the latter requires the use of external test equipment that totally defeats the purpose of BIST to begin with.

We use the following notations in the following analysis:

- D - Product defect level after test under fault-free BIST hardware
- D' - Product defect level after test under unreliable BIST hardware and without BIST pretest
- D'' - Product defect level after test under unreliable BIST hardware and with BIST pretest
- F - Fault coverage of the CUT under fault-free BIST hardware
- F' - Effective fault coverage of the CUT in the presence of an unreliable BIST hardware and without BIST pretest

F'' - Effective fault coverage of the CUT in the presence of an unreliable BIST hardware and with BIST pretest
Y - Product yield
p - Fault probability
n_c - Total number of possible faults in the CUT
n_b - Total number of possible faults in the BIST hardware
m - Number of CUT faults covered by fault-free BIST hardware
m_b - The number of BIST circuitry faults covered by the BIST operation pretest
m' - Expected number of CUT faults covered by an unreliable BIST hardware and without BIST pretest
m'' - Expected number of CUT faults covered by an unreliable BIST hardware and with BIST pretest
k - Average number of CUT faults covered by a faulty BIST hardware and without BIST pretest
k^* - Average number of CUT faults covered by a faulty BIST hardware and with BIST pretest
α - Ratio between BIST area and the CUT area
ρ - CUT Fault coverage alteration factor without BIST pretest
ρ' - CUT Fault coverage alteration factor with BISTpretest
μ - BIST circuitry fault coverage during pretest
λ - Yield coefficient

Notice that we are allowing the test procedure, as conducted by the faulty BIST hardware, to detect CUT faults. The number of CUT faults detected by a faulty BIST depends upon the type of fault actually existing in the BIST hardware. Further denote by k the average number of all the k_{f_i}s, where k_{f_i} $(0 \le k_{f_i} \le n_c)$ is the number of CUT faults detected in the presence of BIST circuitry fault f_j $(1 \le j \le n_b)$. Note that a catastrophic BIST fault will end up rejecting all CUTs, good or bad, resulting in $k_{f_i} = n_c$. Similarly, denote by k^* the average number of all k_{f_j}s, where k_{f_j} $(0 \le k_{f_j} \le n_c)$ is the number of CUT faults detected in the presence of BIST circuitry fault f_j, that passed the BIST pretest, $1 \le j \le (n_b - m_b)$.

The parameter ρ is the CUT *fault coverage alteration factor* without BIST pretest [1], and is given by,

$$\rho = \frac{k}{m} \quad (0 \le \rho \le 1/F),$$

Let ρ' be the CUT *fault coverage alteration factor* with BIST pretest. Thus,

$$\rho' = \frac{k^*}{m} \quad (0 \le \rho' \le 1/F),$$

We proceed to calculate m'', the expected number of CUT faults covered by BIST. Since the BIST circuitry that conducts the CUT test has passed the operation pretest, it is guaranteed to be free of the m_b faults covered by it. Therefore,

$$m'' = m \times \Pr\{\textit{Fault-free BIST}\} + k^* \times \Pr\{\textit{Faulty BIST}\}$$
$$m'' = m(1-p)^{n_b-m_b} + k^*[1-(1-p)^{n_b-m_b}] \tag{8}$$

The expected CUT fault coverage, as conducted by the BIST circuitry, is:

$$F'' = \frac{m''}{n_c} = \frac{m}{n_c}(1-p)^{n_b-m_b} + \frac{k^*}{n_c}\left[1-(1-p)^{n_b-m_b}\right]$$
$$= \frac{m}{n_c}\left\{(1-p)^{n_b-m_b} + \frac{k^*}{m}[1-(1-p)^{n_b-m_b}]\right\}$$
$$F'' = F\left[Y^{\frac{n_b-m_b}{n_c}} + \rho'\left(1-Y^{\frac{n_b-m_b}{n_c}}\right)\right] \tag{9}$$

The exponent in Eq. (9) can be written as

$$\frac{n_b-m_b}{n_c} = \frac{n_b}{n_c}\left(1-\frac{m_b}{n_b}\right) = \alpha(1-\mu),$$

where $\alpha = n_b/n_c$, and $\mu = m_b/n_b$.

We define $\lambda = \alpha(1-\mu)$. We call λ the *yield coefficient*, $0 \le \lambda \le 1$. The parameter μ is the BIST circuitry fault coverage during the pretest.

The effective fault coverage, F'', can now be written as

$$F'' = F[Y^\lambda + \rho'(1-Y^\lambda)], \tag{10}$$

and the defect level after the CUT functional test becomes

$$D'' = 1 - Y^{1-F''}. \tag{11}$$

Example 1: Consider a chip manufacturing line with 90% yield. The chips are screened using their BIST circuitry. The BIST circuitry constitutes 5% of the entire chip area. The BIST procedure has 95% coverage of the functional faults when assumed to be fault-free, and only 40% coverage when assumed faulty. Let the BIST circuitry undergo a pretest with self-fault coverage of $\mu = 0.3$. All chips failing the pretest are discarded. The chips passing the pretest are kept and used to perform the BIST CUT test. Chips that fail the CUT test are discarded. Compute the defect level of the chips passing both tests.

Solution: We have the following parameters:

$$\alpha = \frac{5}{95} = \frac{1}{19}, \quad \mu = 0.3,$$
$$\lambda = \frac{0.7}{19} \approx 3.68\times10^{-2}, \quad \rho' = \frac{40}{95} \approx 0.421$$
$$F'' = 0.95 \times \left[0.9^{3.68\times10^{-2}} + 0.421 \times \left(1-0.9^{3.68\times10^{-2}}\right)\right]$$
$$\approx 0.9479$$
$$D'' \approx 1-0.9^{1-0.9479} \approx 1-0.9^{0.0521} \approx 5.474\times10^{-3}$$
$$\approx 5474 \text{ ppm}$$

Which is 95 ppm smaller than the detect level obtained without a pretest [1]. □

It is interesting to take note of the following special cases:

If there is no BIST circuitry ($\alpha = 0$), we have $F'' = F$, and $D'' = D$. This is the Williams and Brown's case. Also, in the case of an ideal BIST pretest, we have $\mu = 1$. In this case also, the formulas reduce to the Williams and Brown's case. The reason for this is that when $\mu = 1$ the BIST pretest is able to get rid of *all* the chips with faulty BIST hardware. The CUT, therefore, is tested by a *reliable* "tester", which

was the underlying assumption used by Williams and Brown in the first place.

If the BIST procedure has zero coverage against functional faults while being itself faulty, then $\rho' = 0$. The effective fault coverage, in this case, reduces to:

$$F'' = FY^{\lambda} \tag{12}$$

Note that the case of $\mu = 0$ is the case of a "pretest with no coverage against its own faults". This is, therefore, identical to the case of CUT screening without a BIST pretest. The formulas in this case reduce to those derived in [1], and shown earlier in Sect. 2 for the reader's convenience.

We measure the impact of the BIST impurity on the product defect level by the differential $\Delta D'' = D'' - D$, or, equivalently, by its normalized form, $\Delta D''/D$. When a product manufacturing process reaches maturity, its yield is close to 1. Furthermore, in most real-life cases $F'' \approx F$, $\lambda \ll 1$. By using calculus approximation techniques we get two sets of approximation formulas. The first set:

$$\Delta D'' \approx F\lambda(1-\rho')\ln^2 Y, \tag{13}$$

and

$$\frac{\Delta D''}{D} \approx \frac{F\lambda(1-\rho')\ln^2 Y}{(1-F)(1-Y)}. \tag{14}$$

The second set of formulas can be obtained from the first set by letting $\ln Y \approx -(1-Y)$:

$$\Delta D'' \approx F\lambda(1-\rho')(1-Y)^2 \tag{15}$$

$$\frac{\Delta D''}{D} \approx \frac{F\lambda(1-\rho')(1-Y)}{1-F} \tag{16}$$

For the catastrophic case ($\rho' = 1/F$), we get from Eqs. (15) and (16):

$$\Delta D''\,|_{cat} \approx -\lambda(1-F)(1-Y)^2 \tag{17}$$

$$\left.\frac{\Delta D''}{D}\right|_{cat} \approx -\lambda(1-Y) \tag{18}$$

3.2 Sizing the Effect of the BIST Pretest

It is interesting to assess the influence of the BIST pretest on the shipped-product defect level. To assess this impact we compute the difference in $\Delta D/D$ with and without the BIST pretest. This will help determine if the alteration in product defect level, achieved as a result of the BIST pretest, is worth the added risk of having to compromise the loss in product yield.

Let δD be the difference between the two defect level differentials with and without a BIST pretest. Let $\delta D/D$ denote the difference between the two normalized differentials (normalized against the Williams and Brown's case). We, therefore, have:

$$\delta D = \Delta D' - \Delta D''$$

At maturity, and under relatively high fault coverages, we get:

$$\delta D \approx F\alpha[\mu(1-\rho') + (\rho' - \rho)]\ln^2 Y \tag{19}$$

and

$$\frac{\delta D}{D} \approx \frac{F\alpha[\mu(1-\rho') + (\rho' - \rho)]\ln^2 Y}{(1-F)(1-Y)} \tag{20}$$

We define the *differential impact factor* as:

$$\zeta = \frac{\Delta D'}{\Delta D''}$$

The differential impact factor is a measure of the improvement in shipped-product defect level with and without BIST pretest.

At maturity, and under relatively high fault coverages, we get:

$$\zeta \approx \frac{1-\rho}{(1-\mu)(1-\rho')} \tag{21}$$

There is no good reason why k^* should (statistically) be any different from k. The reason for this is that the BIST operation pretest will only guarantee that those ICs that pass it are free of some, but not all, of the totality of possible faults. Thus, some of the BIST faults are likely to remain in the circuitry even after passing the pretest. Out of these faults that do remain in the circuitry, the fraction of BIST circuitry faults f_i, $1 \le i \le n_b$, with $k_{f_i} > k$ or $k_{f_i} < k$ are statistically equal to the fraction of BIST circuitry faults f_j, $1 \le j \le (n_b - m_b)$, that passed the BIST pretest, under $k_{f_j} > k$ or $k_{f_j} < k$ condition. Therefore, the eliminated BIST circuitry faults will not affect (in principle) the average k.

By letting $k^* \approx k$ we get $\rho' \approx \rho$. In this case we, therefore, get:

$$\delta D \approx F\alpha\mu(1-\rho)\ln^2 Y \tag{22}$$

and

$$\frac{\delta D}{D} \approx \frac{F\alpha\mu(1-\rho)\ln^2 Y}{(1-F)(1-Y)} \tag{23}$$

By letting $\ln Y \approx -(1-Y)$ in Eq. (23) we get:

$$\frac{\delta D}{D} \approx \frac{F\alpha\mu(1-\rho)(1-Y)}{1-F} \tag{24}$$

$$\zeta \approx \frac{1}{1-\mu} \tag{25}$$

For the catastrophic case ($\rho = 1/F$), we get from Eq. (24):

$$\left.\frac{\delta D}{D}\right|_{cat} \approx -\alpha\mu(1-Y) \tag{26}$$

Example 2: As a continuation of Ex.1, we use Eqs. (22)–(26) to assess the BIST pretest impact on the final product defect level:

Solution: We have:

$$\delta D \approx .95 \times .0526 \times .3 \times (1 - .421) \times \ln^2 0.9 = 96\,\text{ppm}$$

Compare this to the 95 ppm computed in Ex.1. Similarly,

$$\frac{\delta D}{D} \approx \frac{\delta D}{(1-0.95)(1-0.9)} \approx 0.019,$$

which is less than 2%. The differential impact factor in this case is:

$$\zeta \approx \frac{1}{0.7} = 1.4285,$$

which indicates that the BIST pretest strategy has reduced the defect level by a factor larger than 1.4. □

4. Some Typical Behavior

During the product's early life its yield is relatively low. This is mostly due to not quite knowing how to best fine-tune the manufacturing parameters of an emerging new technology. Typical early life yields may vary between 40% to 60% [36], even though lower figures are also possible. As the manufacturing process matures, the yield figures may rise to as much as 90%, or even higher [36]. In this section we try to shed some light on the impact of the BIST pretest during these two distinct periods of the product's life. The parameters chosen in this study reflect likely operating conditions of an IC manufacturing house. In the following study we assume $\rho' \approx \rho$.

4.1 Early Life Impact

In order to study the impact of the BIST pretest on the product's early life defect level after the CUT test, we let $0.4 \leq Y \leq 0.6$. The other parameter ranges are $0.9 \leq F \leq 0.99$, $0.4 \leq \rho \leq 0.6$, $0.05 \leq \alpha \leq 0.1$ and $0.4 \leq \mu \leq 0.6$. These parameter ranges are used again in the next subsection, and they reflect practical values for BIST-based IC products [10], [11].

In Fig. 1 we show the behavior of F''/F and $\delta D/D$ as a function of Y, while keeping the other parameters fixed at $F = 0.9$, $\rho = 0.4$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 2 we show the behavior of F''/F and $\delta D/D$ as a function of ρ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.4$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 3 we show the behavior of F''/F and $\delta D/D$ as a function of α, while keeping the other parameters fixed at $F = 0.9$, $\rho = 0.4$, $\mu = 0.5$, and $Y = 0.4$. In Fig. 4 we show the behavior of F''/F and $\delta D/D$ as a function of F, while keeping the other parameters fixed at $Y = 0.4$, $\rho = 0.4$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 5 we show the behavior of F''/F and $\delta D/D$ as a function of μ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.4$, $\rho = 0.4$, $\alpha = 0.05$.

Figure 1 shows that during early life the BIST pretest has improved the product defect level by about 6–10%. Figures 2 and 3 show the defect level trend as a function of the CUT fault coverage alteration factor ρ, and ratio between BIST area and the CUT area α. Figure 4 shows that this quality improvement grows to 80% for CUT fault coverages F around 98%. Figure 5 shows an improvement of 10–14% in defect level for the chosen range of the self-fault coverage μ.

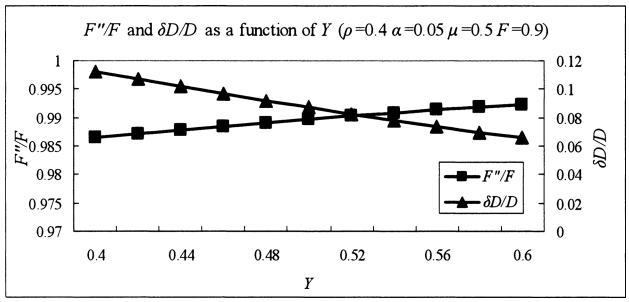

Fig. 1 F''/F and $\delta D/D$ as a function of Y.

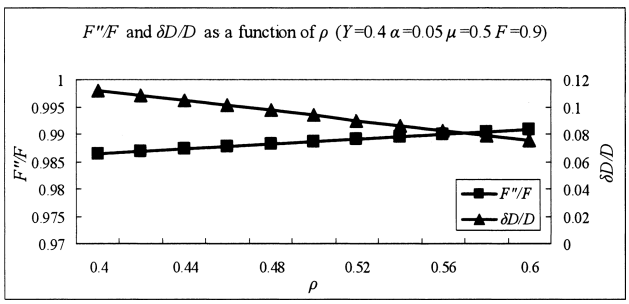

Fig. 2 F''/F and $\delta D/D$ as a function of ρ.

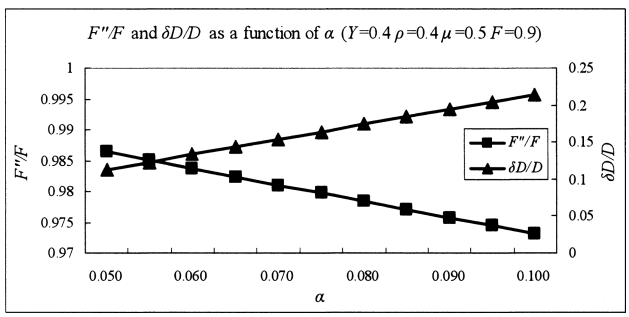

Fig. 3 F''/F and $\delta D/D$ as a function of α.

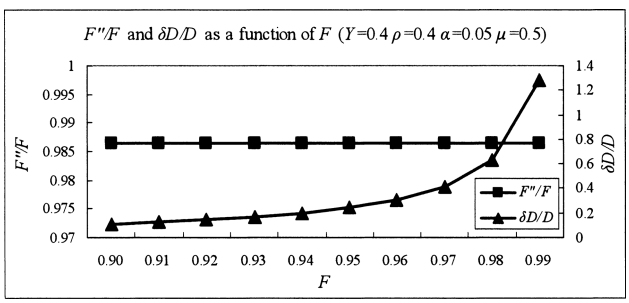

Fig. 4 F''/F and $\delta D/D$ as a function of F.

4.2 Impact at Maturity

Since at maturity $Y \approx 1$, we plot F''/F and $\delta D/D$ for the parameter ranges $0.9 \leq Y \leq 0.95$, $0.9 \leq F \leq 0.99$, $0.4 \leq \rho \leq 0.6$, $0.05 \leq \alpha \leq 0.1$ and $0.4 \leq \mu \leq 0.6$. In Fig. 6 we show the behavior of F''/F and $\delta D/D$ as a function of Y, while

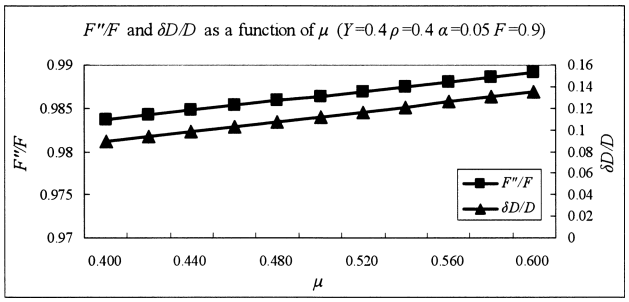

Fig. 5 F''/F and $\delta D/D$ as a function of μ.

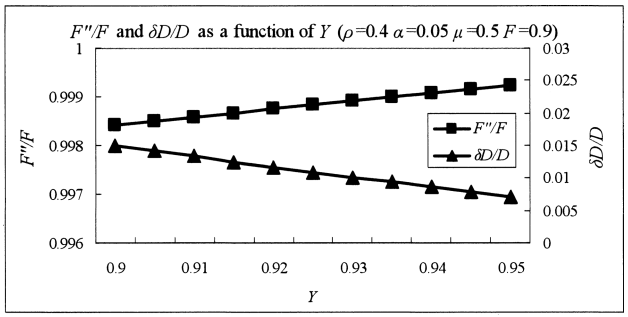

Fig. 6 F''/F and $\delta D/D$ as a function of Y.

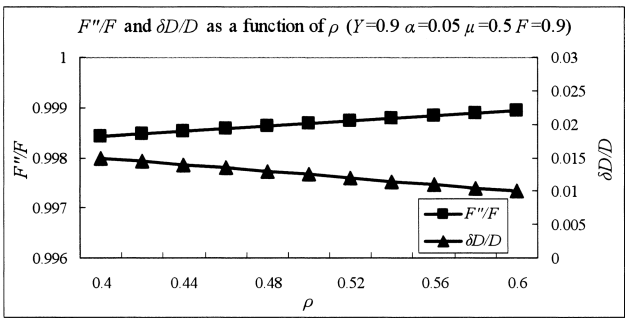

Fig. 7 F''/F and $\delta D/D$ as a function of ρ.

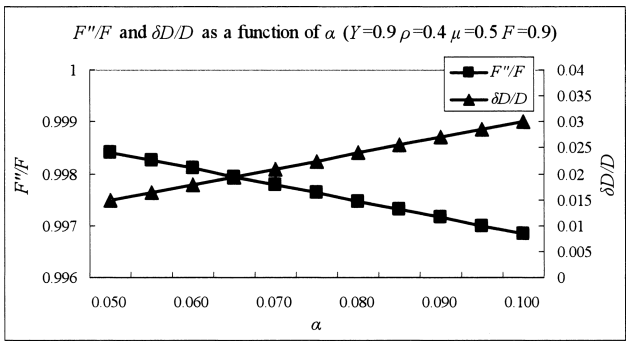

Fig. 8 F''/F and $\delta D/D$ as a function of α.

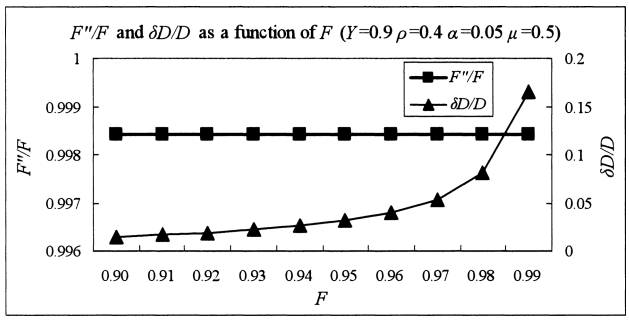

Fig. 9 F''/F and $\delta D/D$ as a function of F.

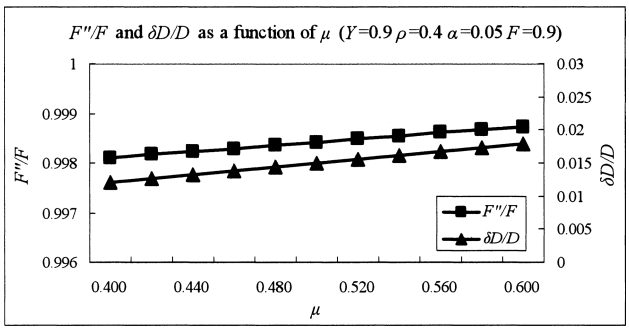

Fig. 10 F''/F and $\delta D/D$ as a function of μ.

keeping the other parameters fixed at $F = 0.9$, $\rho = 0.4$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 7 we show the behavior of F''/F and $\delta D/D$ as a function of ρ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.9$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 8 we show the behavior of F''/F and $\delta D/D$ as a function of α, while keeping the other parameters fixed at $F = 0.9$, $\rho = 0.4$, $Y = 0.9$. and $\mu = 0.5$. In Fig. 9 we show the behavior of F''/F and $\delta D/D$ as a function of F, while keeping the other parameters fixed at $Y = 0.9$, $\rho = 0.4$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 10 we show the behavior of F''/F and $\delta D/D$ as a function of μ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.9$, $\rho = 0.4$, $\alpha = 0.05$.

Figures 6–10 show the product defect level dependency on the various parameters at maturity stage. The product defect level trend is similar to early life, however the impact of the various parameters is much smaller than those observed before. Figure 6 shows that for CUT fault coverages below 98% the impact of the pretest on the product defect level is quite minor (around 2%). However, Fig. 9 shows that this quality improvement grows substantially when the CUT fault coverage exceeds 98%, and can be as high as 20–30%.

4.3 Comparison of Defect Levels with and without BIST Pretest

In this section, we explore the impact of the BIST pretest on the defect level by comparing the value of $\Delta D''/D$ (with BIST pretest) to that of $\Delta D'/D$ (without BIST pretest). The parameters chosen are the same as in previous sections, i.e. $0.4 \le Y \le 0.6$ for early life analysis, and $0.9 \le Y \le 0.95$ for maturity life period. The other parameter ranges are $0.9 \le F \le 0.99$, $0.4 \le \rho \le 0.6$, $0.05 \le \alpha \le 0.1$ and $0.4 \le \mu \le 0.95$.

In Fig. 11 we show the behavior of $\Delta D''/D$, $\Delta D'/D$, and the differential impact factor ζ as a function of Y, while

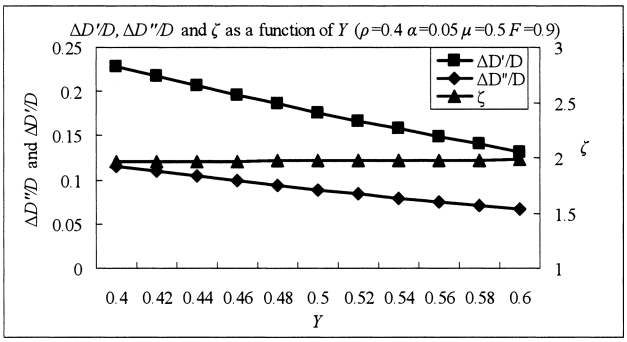

Fig. 11 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of Y (early life).

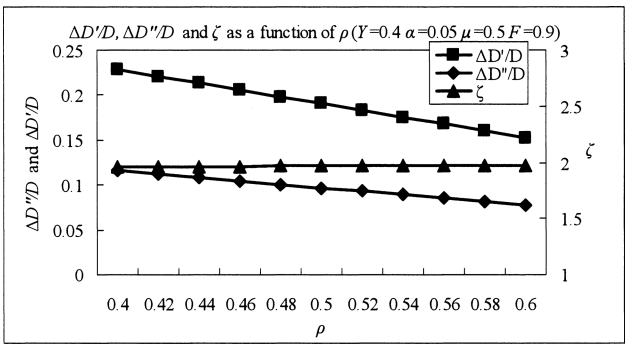

Fig. 12 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of ρ (early life).

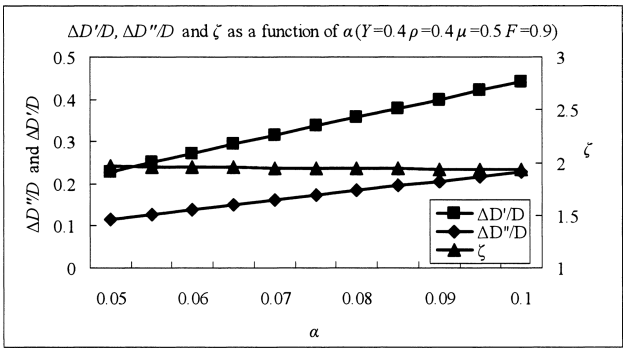

Fig. 13 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of α (early life).

keeping the other parameters fixed at $F = 0.9$, $\rho = 0.4$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 12 we show the behavior of $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of ρ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.4$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 13 we show the behavior of $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of α, while keeping the other parameters fixed at $F = 0.9$, $\rho = 0.4$, $\mu = 0.5$, and $Y = 0.4$. In Fig. 14 we show the behavior of $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of F, while keeping the other parameters fixed at $Y = 0.4$, $\rho = 0.4$, $\alpha = 0.05$ and $\mu = 0.5$. In Fig. 15 we show the behavior of $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of μ, while keeping the other parameters fixed at $F = 0.9$, $Y = 0.4$, $\rho = 0.4$, $\alpha = 0.05$.

In Figs. 16–20 we show the corresponding behavior at maturity. The difference between these figures and Figs. 11–

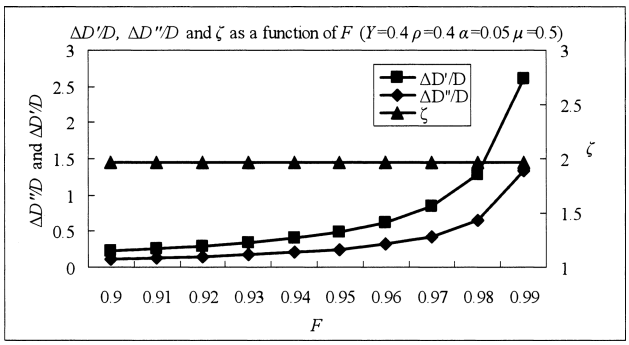

Fig. 14 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of F (early life).

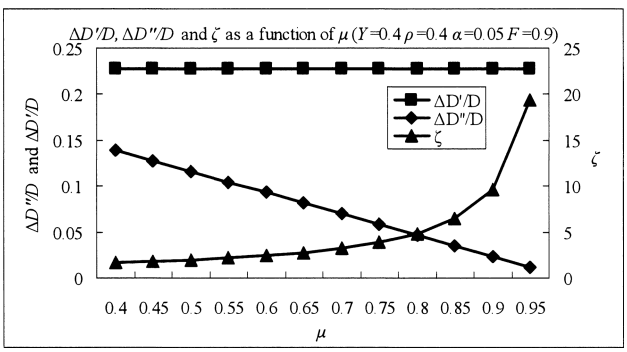

Fig. 15 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of μ (early life).

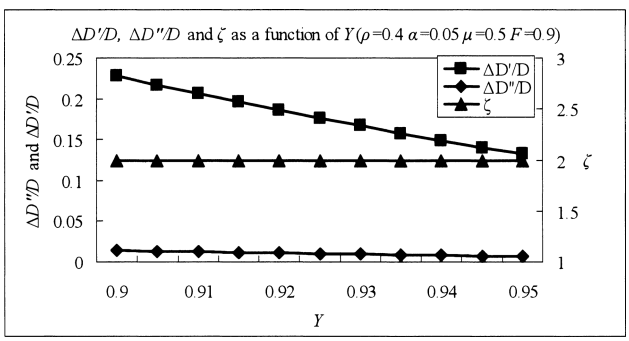

Fig. 16 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of Y (maturity life).

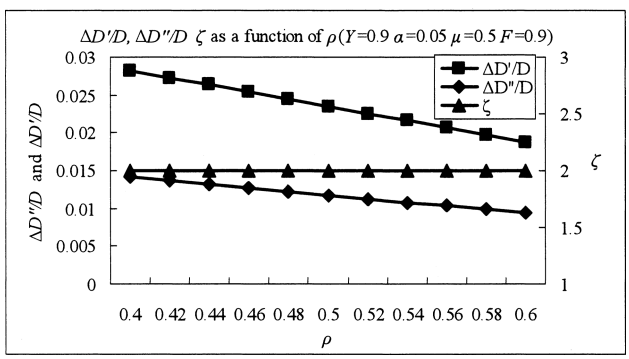

Fig. 17 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of ρ (maturity life).

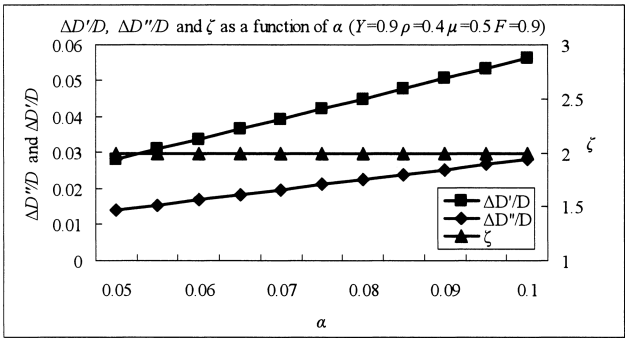

Fig. 18 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of α (maturity life).

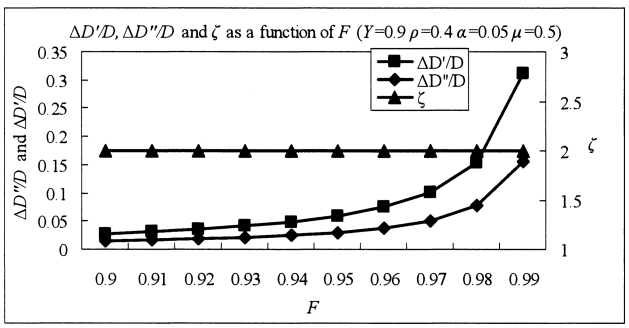

Fig. 19 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function F (maturity life).

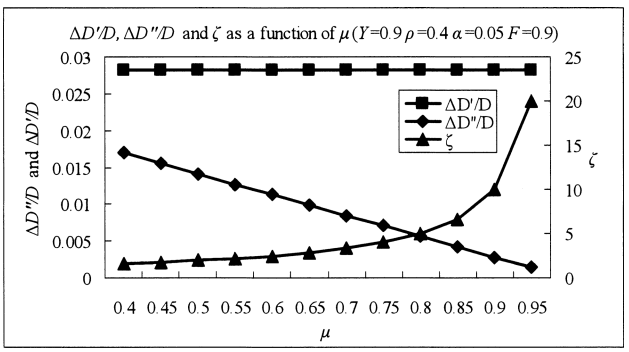

Fig. 20 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of μ (maturity life).

15, is that the range of Y is $0.9 \leq Y \leq 0.95$ in Fig. 16, and Y is fixed at 0.9 in Figs. 17–20.

Figures 11–15 and 17–19 show that even when the BIST self-fault coverage is a modest 50%, the BIST pretest strategy may reduce the defect level by a factor of 2. Therefore, the equation derived in [1] do not constitute a good estimate for the defect level in the presence of a BIST pretest. Our new equations, derived in this paper, should be used instead. Figures 16 and 20 show that for cases where the BIST circuitry self-fault coverage is close to 90%, the differential impact factor is around 10, i.e., the BIST pretest strategy has managed to reduce the overall defect level by a factor of about 10.

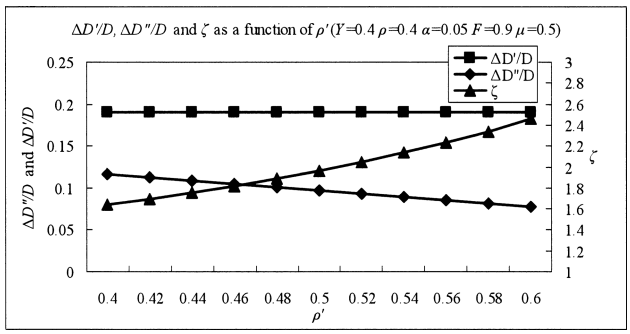

Fig. 21 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of ρ' (early life).

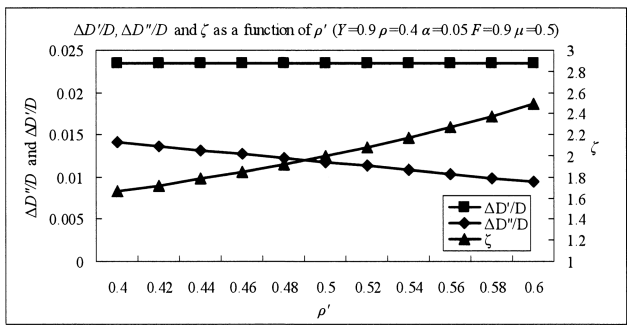

Fig. 22 $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of ρ' (maturity life).

4.4 The Case $\rho' \neq \rho$

In Sects. 4.1–4.3, we assumed that $\rho' \approx \rho$. In this section we investigate the defect level behavior when $\rho' \neq \rho$.

In the following graphs we let $Y = 0.4$ during early life and $Y = 0.9$ during maturity life. The other parameters are fixed at $F = 0.9$, $\rho = 0.5$, $\alpha = 0.05$ and $\mu = 0.5$. The parameter ρ' is chosen to cover the range $0.4 \leq \rho' \leq 0.6$. In Figs. 21 and 22 we show the behavior of $\Delta D''/D$, $\Delta D'/D$ and ζ as a function of ρ' during early life and at maturity, respectively.

Figures 21 and 22 show the influence of the difference between ρ' and ρ on the differential impact factor. As seen in these graphs, when this difference grows larger, the differential impact factor is increasing in value. Figures 21 and 22 indicate that even when ρ and ρ' only differ by about 10%, the BIST pretest is still efficient.

4.5 The Impact Trend

As was mentioned earlier, by discarding the chips that fail the pretest we are risking loosing products that would otherwise be functional. This will, undoubtedly, increase the yield loss. Given the fact that the pretest will not get rid of all chips with faulty BIST circuitry, some people may argue that this pretest is not worth the risk of loosing yield.

As seen in the previous subsection, unless the CUT fault coverage is in the high 90 percent, the pretest won't buy you much quality improvement during maturity. For CUT

fault coverages below 98% the impact of the pretest on the product defect level is quite minor (around 2%). This quality improvement grows substantially when the CUT fault coverage exceeds 98%, and can be as high as 20–30%.

During early life the BIST pretest has a greater effect on the product defect level. Even for CUT fault coverages around 90%, the BIST pretest can decrease the product defect level by as much as 10%. This quality improvement grows to 80% for fault coverages around 98%.

The *differential impact factor* highly depends upon the BIST circuitry self-fault-coverage during pretest. We have shown that even when this BIST self-fault-coverage is relatively low, the BIST pretest strategy may reduce the defect level by a factor of 2. For cases where the BIST circuitry fault coverage during pretest are closer to 90%, the differential impact factor is around 10, i.e., the BIST pretest strategy has managed to reduce the overall defect level by a factor of about 10. The differential impact factor also depends upon the CUT fault coverage alteration factors, ρ' and ρ. We assumed that $\rho' \approx \rho$ in the analysis of Sects. 4.2 and 4.3. However, Figs. 21 and 22 show that even when ρ' and ρ differ by about 10%, the BIST pretest is still efficient.

5. Conclusions

In this paper we assume that the BIST circuitry is pretested before launching the CUT functional test. The intent of the BIST pretest is to get rid of all chips that fail it, and, therefore, avoid a situation where a faulty BIST has to determine whether or not the functional circuits operate correctly. By discarding the chips that fail the pretest we are risking loosing chips that would otherwise be functional. This will, undoubtedly, increase the yield loss. Given the fact that the pretest will not eliminate all chips with faulty BIST circuitry, some people may argue that this pretest is not worth the risk of loosing yield. This paper provides some insight as to when this BIST pretest maybe worthwhile.

We show that the BIST pretest has an effect of reducing the product defect level of chips passing the CUT BIST. The question is whether or not the improvement in the shipped-product defect level is worth loosing functional chips as well.

Our analysis indicates that for products with CUT fault coverages exceeding 98%, it makes sense to do the BIST pretest. The BIST pretest has the effect of reducing the product defect level by at least 80% during early life, and by as much as 10% during maturity.

During early life, and even for fault coverages below 98%, the BIST pretest offers a non-negligible improvement in product quality. Since this improvement can be as small as 20–30%, and as high as 100%, BIST pretest is worthwhile performing.

The analysis provided in this paper covers a wide range of possible fault models. Different fault models, however, require different parameter values. For example, AC (timing) faults require different parameter values than permanent (stuck-at) faults. Take for example the fault coverage parameter. Its value for permanent faults may be close to 98%, while its value for AC-type faults may be closer to 70%. Thus, by properly selecting the parameter values, realistic sizing of the defect levels may be achieved.

Acknowledgments

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