Constraining Transition Propagation for Low-Power Scan Testing Using a Two-Stage Scan Architecture

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***Abstract*—A two-stage scan architecture is proposed to constrain transition propagation within a small part of scan flip-flops. Most scan flip-flops are deactivated during test application. The first stage includes multiple scan chains, where each scan chain is driven by a primary input. Each scan flip-flop in the multiple scan chains drives a group of scan flip-flops in the second stage. Scan flip-flops in different stages use separate clock signals. Test signals assigned to scan flip-flops in the multiple scan chains are applied to the scan flip-flops of the second stage in one clock cycle after the test vector has been applied to the multiple scan chains. There exists no transition at the scan flip-flops in the second stage when a test vector is applied to the multiple scan chains.**

***Index Terms*—Clock disabling, clock tree test power consumption, scan testing, test application cost, test power.**

I. Introduction

TEST application time, test power, and test data volume of scan testing can be very large. It is essential to propose an effective method that can reduce test application time, test data volume, and test power consumption simultaneously. Test power reduction can be completed by test-compression techniques [1], [3], [12], test sequence or scan flip-flop ordering [2], new scan architectures [2], [7], [10], [13], [14], and transition propagation reduction techniques [6], [13], and low-power built-in self-test (BIST) generator design.

Techniques were presented to minimize test power by maximizing clock disables. References [6], [13] inserted extra logic into the circuit to block transition propagation from the scan chain into the combinational part. These methods constrained test power inside the scan chain. Test energy is proportional to the total number of transitions in the whole process of test application.

Test energy in a circuit (except the clock tree) to apply a test vector includes four separate parts: 1) scan-in; 2) scan-out; 3) capturing; and 4) transferring. The capturing test energy represents the test energy consumed by the transitions from the state that a test vector has been shifted to the state that the test responses have been captured. The transferring test energy is the test power from captured test responses of the previous test vector to the next test vector, which occurs at the root of a scan tree or the first scan flip-flop of a scan chain.

Test energy for the scan forest [14] is still similar to scan design with a scan chain, where a transition at a scan flip-flop can be propagated globally into all scan flip-flops in a scan tree and the whole combinational circuits. We would like to limit transition propagation within a very small part of the scan flip-flops during scan shifts, which effectively blocks propagation of transitions at the scan flip-flops to the combinational part of the circuit for scan shift cycles. The test data stored in the scan flip-flops in the first stage are then propagated to the scan flip-flops in the second stage easily.

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II. Two-Stage Scan Architecture

A two-stage scan architecture is proposed in this section to achieve a scan testing scheme with very low test energy, test application cost and test data volume. The proposed scan architecture consists of two separate parts: The multiple scan chains in the first stage and the scan flip-flop groups driven by the scan flip-flops of the multiple scan chains in the second stage. Each scan flip-flop in the multiple scan chains and the scan flip-flop group driven by it are in the same group. All the scan flip-flops in the same group have no common successor in the combinational part of the circuit. We say two scan flip-flops u and v have a common successor if there exists a gate $v^{'}$, such that there exist combinational paths from u to $v^{'}$ and from v to $v^{'}$, respectively. There is no new reconvergent fanout if any pair of scan flip-flops in the same group do not have any common combinational successor as stated above.

Each scan flip-flop in the multiple scan chains and the scan flip-flops driven by it are assigned the same values for all test vectors. All scan-in signals of the multiple scan chains are driven by primary inputs. Two scan-out signals can be connected to an XOR gate if the following condition is met: Let $(v_1, v_2, \ldots, v_k)$ and $(v_1', v_2', \ldots, v_k')$ be two scan chains. The scan-out signals of both scan chains can be connected with an XOR gate without generating any aliasing faults if each pair of scan flip-flops v_1 and v_1', v_2 and v_2', $\ldots$, v_k and v_k' do not have any common predecessor in the combinational part of the circuit, respectively.

There exists a lot of flexibility when multiple scan chains are connected with the same XOR gate. As for each test vector, each scan flip-flop in the multiple scan chains and the scan flip-flop group driven by it are assigned the same value. Any one of the scan flip-flops in the scan flip-flop group can be exchanged with the one that drives it in order to satisfy the condition. Each scan flip-flop group in the second stage and the scan flip-flop in the multiple scan chains in the first stage that drives it share the same pseudo primary input in the test circuit. The XOR trees are added

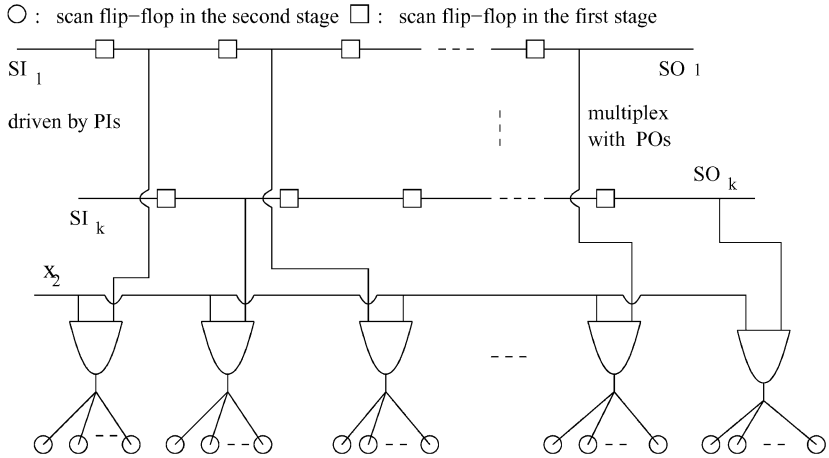

Fig. 1. Two-stage scan architecture.

into the test circuit to do fault simulation using HOPE [10] after the test vectors have been generated.

The two-stage scan architecture is given in Fig. 1. The boxes shown in Fig. 1 are scan flip-flops in the multiple scan chains. The scan flip-flops in the second stage are connected with multiple XOR trees, where all scan flip-flops connected with the same XOR tree have no common predecessor in the combinational part of the circuit. This technique avoids aliasing faults when compacting test responses of the scan flip-flops. All scan flip-flops having no common predecessor can form another scan flip-flop group. Sizes of the scan flip-flop groups can be regulated. The regulation of scan flip-flop group sizes can be completed easily because of flexibility of the scan flip-flop grouping scheme for the XOR trees. Outputs of the XOR trees are multiplexed with the primary outputs in order to reduce the number of extra pins. The two-stage scan architecture can be extended to the one that has multiple level trees in the second stage, which can greatly reduce the number of leaf scan flip-flops, area overhead and routing overhead. The multiplexer that connects with an output of an XOR tree is controlled by *test* signal, which controls multiplexers of all scan flip-flops. The circuit is in test mode when *test* is set to 1, and in functional mode when it is set to 0.

The scan flip-flops are grouped as stated earlier. The multiple scan chain in the first stage is constructed by selecting one scan flip-flop from each scan flip-flop group, where each scan flip-flop selected drives the remaining scan flip-flops in the same group. The remaining scan flip-flops in the group construct a tree structure of the new scan architecture shown in Fig. 1. Therefore, the number of scan flip-flops in the first stage is equal to the number of scan flip-flop groups in the second stage. The sequence of the scan flip-flops in the first stage does not influence testability of the circuit. Splitting the scan flip-flop groups into two stages does not influence test data-compression feature because scan flip-flops in the same group are still assigned the same values for all test vectors based on the two-stage scan architecture.

Different clock signals C_1 and C_2 are used for scan flip-flops in both stages, respectively. However, we still only use a single clock C as shown in Fig. 2. Two extra pins X_1 and X_2 are utilized to activate clock signals C_1 and C_2 for separate parts of the scan architecture. The clock C is active during the process

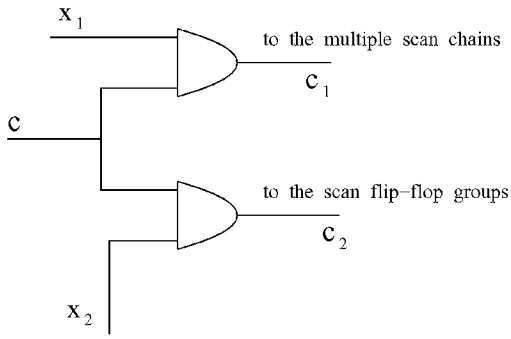

Fig. 2. Clock control scheme.

of test application for each test. The extra pin X_1 is set as 1 and X_2 is set as 0 during the scan shift cycles. The clock signal C_1 is activated, and the clock signal C_2 is disabled at this point. All transitions at the multiple scan chains cannot be propagated to the corresponding scan flip-flop groups in the second stage. The extra pin X_1 is set as 0 and X_2 is set to 1 after the test vector has been shifted into the multiple scan chains in the first stage. That is, clocks of the scan flip-flops in the second stage are activated and the clocks of the scan flip-flops in the first stage are disabled. The test pattern shifted to the multiple scan chains is shifted to the scan flip-flop groups in the second stage. The scan flip-flops in the multiple scan chains are not connected with the scan flip-flops in the second stage directly. Each scan flip-flop in the multiple scan chains drives an AND gate, which is also connected with the extra pin X_2.

Fig. 3 presents an improved two-stage scan architecture, using which multiple clock cycles is requested to transfer the test data stored in the first stage to the second stage. The scan flip-flops in the second stage driven by the same scan flip-flop in the first stage are established as multiple scan chains. Only the first scan flip-flops of the multiple scan chains are connected to the scan flip-flop in the first stage, and only the leaf scan flip-flops of the multiple scan flip-flops are connected to the XOR trees. This technique can greatly reduce wiring overhead and area overhead of the XOR trees. Suppose two scan chains $(v_{1,1}, v_{1,2}, \ldots, v_{1,k})$ and $(v_{2,1}, v_{2,2}, \ldots, v_{2,k})$ be connected to the same XOR tree. Then, $v_{1,1}$ and $v_{2,1}, v_{1,2}$ and $v_{2,2}, \ldots, v_{1,k}$ and $v_{2,k}$ do not have any common combinational predecessor, respectively.

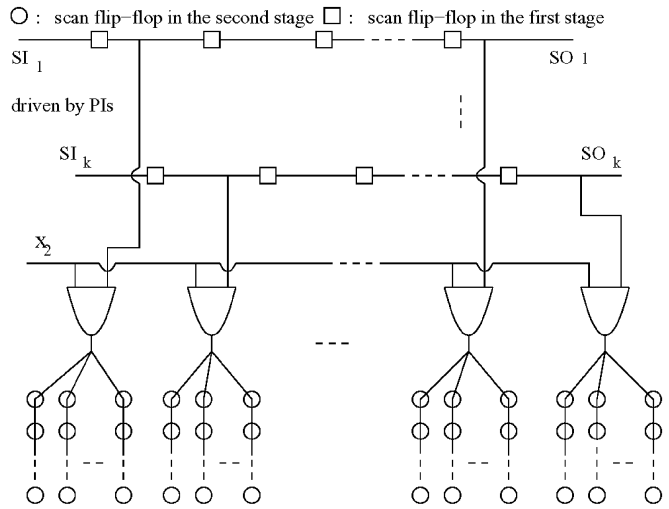

Fig. 3. Improved two-stage scan architecture.

III. Test Application Scheme

The test application scheme is also partitioned into two steps.

1) A test vector is shifted into the multiple scan chains.
2) The vector is propagated to the scan flip-flops in the second stage, which is followed by a functional cycle to receive test responses.

The clocks of the scan flip-flops in the second stage are disabled during the scan shift cycles in order to localize test power consumption inside the multiple scan chains. The clocks of the scan flip-flops in the first stage are disabled after all shift cycles in order to maintain values in the multiple scan chains. The values shifted into the multiple scan chains are propagated to the second stage at this point. The test responses captured at the scan flip-flops are shifted out when shifting into the next test vector.

The *test* pin connected with all multiplexers is set to 1, which turns the circuit into the test mode. The extra pins X_1 and X_2 are set to 1 and 0, respectively. This activates all scan flip-flops in the first stage, and disables all scan flip-flops in the second stage. The test vector is shifted into the scan flip-flops via primary inputs during this phase. The test responses captured at the scan flip-flops in the first stage corresponding to the previous test are shifted out simultaneously if the test is not the first one. X_1 and X_2 are set to 0 and 1, respectively after the test has been shifted into the multiple scan chains. Scan flip-flops in the first stage are disabled, and scan flip-flops in the second stage are activated at this point. The test shifted into the multiple scan chains in the first stage is propagated to the scan flip-flops in the second stage. The part of the test corresponding to the primary inputs are applied when the *test* pin is set to 0 and turn the circuit into functional mode. X_1 and X_2 are both set to 1 in order to activate clocks of all scan flip-flops. All scan flip-flops receive test responses of the test. The test application time TAP' is

$$\mathrm{TAP}' = (l_1 + 2) \cdot \#\mathrm{vectors}' + l_1. \quad (1)$$

In (1), l_1 is the length of the multiple scan chains, and $\#\mathrm{vectors}'$ is the number of test vectors for the circuit with the two-stage scan architecture. The second term in (1) represents the number of clock cycles required to shift out the test responses of the last test vector.

The proposed two-stage scan architecture can control clock tree test energy very well. As for full scan design with a single scan chain, the number of transitions #ctt at the clock tree is

$$\#\mathrm{ctt} = 2 \cdot \#\mathrm{vectors} \cdot (\mathrm{nff} + 1) \cdot \mathrm{nff} + 2 \cdot \mathrm{nff} \cdot \mathrm{nff}. \quad (2)$$

In (2), nff is the number of scan flip-flops, and #vectors is the number of test vectors for the fully scanned circuit with a single scan chain. The second term $2 \cdot \mathrm{nff} \cdot \mathrm{nff}$ in the right hand of (2) is the number of transitions at the clock signals when shifting out the test responses of the last test vector. Transitions at the clock tree include two parts: 1) transitions at the clocks of the scan flip-flops in the multiple scan chains in the first stage; and 2) transitions at the clocks of the scan flip-flops in the second stage

$$\begin{aligned} \#\mathrm{ctt}' &= [2 \cdot \mathrm{nff}_1 \cdot (l_1 + 1) + 2 \cdot \mathrm{nff}_2 \cdot 2] \cdot \#\mathrm{vectors}' \\ &\quad + 2 \cdot \mathrm{nff}_1 \cdot l_1 \\ \mathrm{nff} &= \mathrm{nff}_1 + \mathrm{nff}_2. \end{aligned} \quad (3)$$

In (3), nff_1 is the number of scan flip-flops in the multiple scan chains in the first stage nff_2 is the number of scan flip-flops in the second stage, l_1 is the length of the multiple scan chains in the first stage, and $\#\mathrm{vectors}'$ is the number of test vectors for the circuits with the proposed scan architecture. Similarly, the last term in (3) represents the number of transitions at clock signals when shifting out the test responses of the last test vector. The number of scan flip-flops in the multiple scan chains in the first stage is much smaller than the number of scan flip-flops in the circuit. The number of transitions at the clock signals for the scan forest designed circuit is

$$\#\mathrm{ctt}'' = 2 \cdot \mathrm{nff} \cdot (l_1 + 1) \cdot \#\mathrm{vectors}'' + 2 \cdot \mathrm{nff} \cdot l_1 \quad (4)$$

where l_1 and $\#\mathrm{vectors}''$ in (4) are the height of the scan forest and the number of test vectors for the scan forest designed circuit, respectively.

IV. Experimental Results

The test generator ATALANTA [9] is used to generate tests, and the HOPE [9] fault simulator is utilized to do fault simulation in the experimental results. All results are obtained with a Sun Blade 2000 workstation using C language in the UNIX environment. Test application cost reduction ratio (TA) and the clock tree test energy reduction ratio (CTE) are obtained as follows:

$$\mathrm{CTE} = \#\mathrm{ctt}'/\#\mathrm{ctt}, \mathrm{CTP}' = \#\mathrm{ctt}'/\#\mathrm{ctt}''.$$
$$\mathrm{TA} = \frac{\mathrm{TAP}'}{(\mathrm{nff} + 1) \cdot \#\mathrm{vectors} + \mathrm{nff}}$$

where $\mathrm{TAP}', \#\mathrm{ctt}, \#\mathrm{ctt}'$, and $\#\mathrm{ctt}''$ are obtained by (1), (2), (3), and (4), respectively. And $\mathrm{nff}, \#\mathrm{vectors}$, and CTP' are the

TABLE I
COMPARISON WITH PREVIOUS METHODS ON TEST POWER CONSUMPTION AND TEST APPLICATION COST

circuit	full scan	two−stage scan							multiple		MCD[5]	
	CPU (s)	CPU (s)	CPU' (s)	TA (%)	TE (%)	CTE (%)	TE' (%)	area (%)	TA* (%)	TE* (%)	TA (%)	TE (%)
s13207	5	5	0.63	1.19	0.51	0.50	45.0	14.0	34.7	16.25	6.1	4.2
s15850	6	7	0.6	1.64	0.56	0.52	24.3	11.5	22.3	7.15	20.2	15.1
s38417	40	42	5.0	0.29	0.08	0.12	36.5	14.9	7.91	2.70	38.3	22.9
s38584	20	17	2.48	0.68	0.14	0.17	14.7	13.2	8.10	1.57	20.0	16.0
b17	578	556	11.8	0.78	0.20	0.28	9.85	9.85	27.6	7.14	—	—
b18	9093	9472	127	0.35	0.12	0.08	10.4	10.4	12.8	6.13	—	—

TABLE II
COMPARISON WITH PREVIOUS METHODS ON TEST DATA VOLUME AND TEST APPLICATION REDUCTION

circuits	two−stage scan		BO[1]		RBO[11]		FDR[3]
	TA(%)	TDR(%)	TA(%)	TDR(%)	TA(%)	TDR(%)	TDR(%)
s13207	1.19	27.80	16.20	13.77	8.4	10.6	12.33
s15850	1.64	18.42	21.54	18.29	15.0	17.8	28.05
s35932	0.08	1.34	17.60	16.34	15.8	19.2	—
s38417	0.29	4.88	20.51	19.07	17.2	20.8	34.65
s38584	0.68	6.58	16.02	14.48	10..4	12.8	35.33

TABLE III
TRANSITIONS OF THE SCAN ARCHITECTURES

circuits	full scan design			multiple scan chain		scan forest [14]		two−stage scan			
	seq.	comb.	#ctt	seq.	comb.	seq.	comb.	seq.	comb.	#ctt	CTE'(%)
s13207	99042003	425311556	418645482	3258171	14112830	1080558	5021317	460908	2840240	2116008	44.1
s15850	65983889	219601263	312022050	5564286	16668704	1665260	5011005	332400	1652287	1694960	24.5
s38417	1407554468	4536885318	4820634328	42153446	122984831	2598289	7929674	836199	2590618	5876024	49.2
s38584	681048871	1516282647	2751118920	58156262	128936713	5074014	11400145	743048	3028356	4661952	17.5
b17	3023349665	2234607033	9224755730	60755323	69239364	13815272	14100451	4572511	3330794	25509142	38.8
b18	10686544507	3148662388	64941484160	436834762	36441303	44045121	3639576	9400933	9333606	57414660	27.3

number of scan flip-flops in the circuit, the number of test vectors for the fully scanned circuit with a single scan chain, and the CTE of the two-stage scan corresponding to the original scan forest. The node transition count (NTC) is reported as quantitative measure for test energy in the brief. Let load capacitance C_{load} for each unit be the number of fanouts. The node transition count (N_G) in scan flip-flops is 2 for $1 \rightarrow 1$ and $0 \rightarrow 0$ transitions, and 6 for $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions for all node G. We have

$$\text{NTC} = \sum_{G} N_G \cdot C_{\text{load}}.$$

A transition occurs at a scan flip-flop when a scan flip-flop held a value 0 (or 1) at the previous cycle and it gets a value 1 (or 0) at the current cycle. The transition is propagated to the combinational successors until the transition disappears or a scan flip-flop reaches.

The two-stage scan architecture has been implemented. Results and comparison with the multiple clock disabling (MCD) [5] are also presented, where the MCD is also used a clock disabling scheme. The proposed method is also compared with the multiple scan chains whose number of scan chains is equal to the number of primary inputs in the circuit. TA and test energy reduction ratio (TE) of the proposed two-stage scan architecture corresponding to the multiple scan chains are also presented in Table I. As shown in Table I, TA, TE, TE′, CPU, CPU′, and area represent the test application cost, TEs with respect to full scan with a single scan chain, TE corresponding to the original scan forest, CPU time to generate tests, CPU time to construct the two-stage scan architecture, and the area overhead, respectively. The number of scan chains in the first stage is equal to the number of primary inputs in the circuit. The area overhead

is calculated based on the cell library *class.lib* in the Synopsys system.

$$\text{area} = \frac{\text{additional area of the DFT logic}}{\text{total area of the original circuit}}.$$

As shown in Table I, all circuits designed by the two-stage scan architecture and full scan with a single-scan chain obtain complete fault coverage.

Table II presents comparison of the proposed method with three most recent methods BO [1], RBO [11], and FDR [3] on test data compression and TAs. Table III presents the numbers of sequential transitions, combinational transitions, and the clock tree transitions. The advantage of the proposed method is apparent.

V. Conclusion

A two-stage scan architecture is proposed for scan testing with compressed test data, low test energy and test application cost by localizing test power consumption during test application. The first stage of the new scan architecture consists of multiple scan chains, and the second stage of it is a number of scan flip-flop groups. Each scan flip-flop group in the second stage is driven by a scan flip-flop in the first stage. Transitions at scan flip-flops in the first stage are prevented propagating to the scan flip-flops in the second stage during scan shift cycles. Experimental results are presented to compare with the previous methods.

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