Using Weighted Scan Enable Signals to Improve Test Effectiveness of Scan-Based BIST

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Abstract—The conventional *test-per-scan* built-in self-test (BIST) scheme needs a number of shift cycles followed by one capture cycle. Fault effects received by the scan flip-flops are shifted out while shifting in the next test vector, like scan testing. Unlike deterministic testing, it is unnecessary to apply a complete test vector to the scan chains. A new scan-based BIST scheme is proposed by properly controlling the scan enable signals of the scan chains. Different weighted values are assigned to the scan enable signals of scan flip-flops in separate scan chains. Capture cycles can be inserted at any clock cycle if necessary. A new testability estimation procedure according to the proposed testing scheme is presented. A greedy procedure is proposed to select a weight for each scan chain. Experimental results show that the proposed method can improve test effectiveness of scan-based BIST greatly and most circuits can obtain complete fault coverage or very close to complete fault coverage.

Index Terms—Random testability, scan-based BIST, scan enable signal, weighted random testing.

1 Introduction

SCAN-BASED BIST can be simply classified into two types: *test-per-scan* and *test-per-clock* [1], [2], [5] test schemes. In *test-per-clock* BIST, a test vector is applied and its test responses are captured and compressed every clock cycle [11]. This test scheme needs fewer test vectors to reach the same fault coverage as that for the test-per-scan test scheme, but the area overhead and timing overhead can be unacceptable.

In the *test-per-scan* BIST scheme, a test vector is first shifted into the scan chains and then a functional cycle is adopted to capture test responses. The test responses captured in the scan flip-flops are shifted out when the next test vector is scanned in. Test responses at the data inputs of scan flip-flops are unobservable during the shift cycles in the *test-per-scan* BIST scheme.

Test length is usually determined by the hard-to-detect faults. Test length reduction of the hard-to-detect faults is an important issue. Various techniques are adopted to handle the problem. The most popular techniques include 1) weighted random testing [10], [13], [14], [18], [21], [22] and 2) test point insertion [8], [23], [24]. Other methods include designing a more effective test generator [6], [12], [23]. Complete fault coverage can be obtained when the pseudorandom test generator is modified [7]. A combination of a pseudorandom test generator and a combinational mapping logic was constructed by Chatterjee and Pradhan to [7] produce a given target pattern set of the hard-to-detect faults.

Weighted random testing refers to applying test patterns that have different signal probabilities instead of 0.5 to primary inputs in order to reduce test length or test application time to reach the given fault coverage. However, most weighted random testing methods need to store multiple weight sets on-chip and multiple session testing is usually necessary, which can make the control logic very complex.

Tsai et al. [19] proposed a novel BIST scheme that inserts multiple capture cycles after the scan shift cycles during a test cycle. Thus, the fault coverage of the scan-based BIST can be greatly improved. An improved method of the above paper, presented recently in [9], selects different numbers of capture cycles after the shift cycles during one test cycle, which increases the proportion of at-speed test and enhances the test quality of scan-based BIST. Wang et al. [20] presents a multiple capture cycle test scheme for circuits with multiple clock domains. Scan chain partitioning was presented in [23] to improve the effectiveness of scan BIST based on structural analysis. The recently proposed reconfigured scan forest architecture [25], [26] can further improve the effectiveness of scan-based BIST. The weighted scan enable signal test scheme has been used for deterministic BIST based on a reconfigurable scan forest architecture. Lai et al. [12] proposed a new scan segmentation approach to get more effective BIST.

A *scan cycle* is the period in which a test pattern is shifted into (or test responses are shifted out of) the scan chains. The length of a scan cycle is equal to the number of scan flip-flops in the longest scan chain. A *capture cycle* is the period between two adjacent scan cycles. The circuit is set to

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the functional mode during the period when the test pattern is applied to the circuit, and the test responses are captured in the scan flip-flops. A *test cycle* consists of a scan cycle followed by a capture cycle. The i-controllability $C_i(l)$ $(i \in \{0,1\})$ measure of a node l is defined as the probability of a randomly selected input vector setting l to value i. The observability $O(l)$ is defined as the probability of a randomly selected input vector propagating the value of l to a primary output or the scan-out signal of a scan chain.

A weighted random testing scheme is proposed by using weighted scan enable (scan enable) signals. Unlike the conventional *test-per-scan* scheme, our method can insert capture cycles at any time if necessary. The proposed method does not need to use a more complicated test generator or modify the scan flip-flops. Our method only needs to assign different weights on the scan enable signals of the scan chains.

In the rest of this paper, testability of the *test-per-scan* test scheme is studied in Section 2. Testability features of the proposed BIST scheme based on weighted scan enable signals is introduced in Section 3. Testability estimation for the proposed test scheme is presented in Section 4. Selection of weights for the new scan-based BIST scheme is introduced in Section 5. Experimental results are given in Section 6. Section 7 concludes the paper.

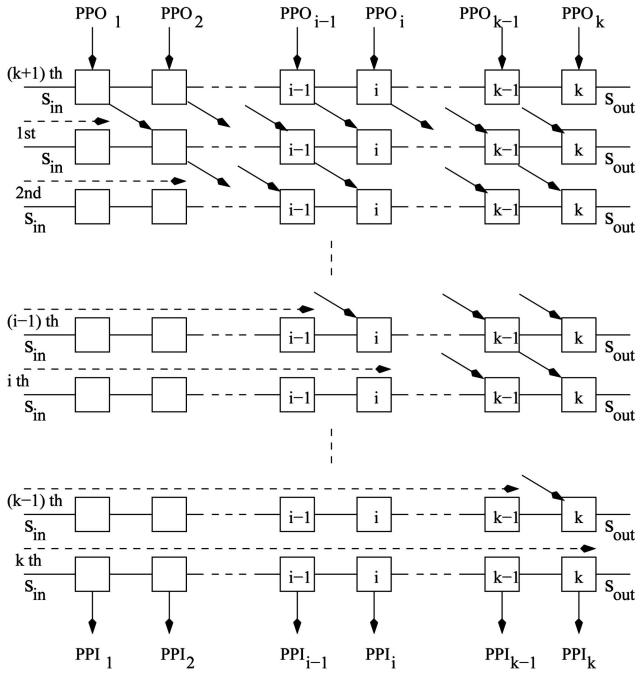


Fig. 1. A test cycle of the *test-per-scan* BIST scheme.

2 Testability of the Test-per-Scan BIST Scheme

Most of the previous conventional *test-per-scan* schemes used the BIST architecture by sharing the same scan enable signal *test*. The outputs of the linear feedback shift register (LFSR) are connected to the phase shifter (PS). The primary inputs are connected to the outputs of the PS. Scan-in signals of the scan chains are also driven by the PS. The scan-out signals of the scan chains and the primary are connected to the multiple input signature register (MISR). The MISR can be compressed by using a compactor. A new testability estimation technique for the test-per-scan BIST test scheme is presented first.

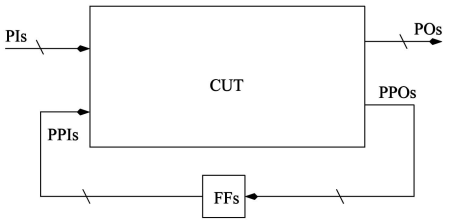
Fig. 1 presents a test cycle for a scan chain of the *test-per-scan* BIST scheme, which consists of a capture cycle of the previous test cycle and k shift cycles of the current test cycle, where k is the length of the longest scan chain. As shown in Fig. 1, test responses at the pseudoprimary outputs (PPOs) are captured in the corresponding scan flip-flops at the capture cycle of the previous test cycle, which is followed by k shift cycles. The random signals are shifted in from the scan-in signal, whereas the captured test responses of the scan flip-flops are shifted out from the scan-out signal sequentially. Consider the ith scan flip-flop; it receives the test response captured at the $(i-1)$th scan flip-flop for the first-shift cycle. It receives the test response captured by the $(i-2)$th scan flip-flip at the second shift cycle. Finally, the ith scan flip-flop receives the test response captured by scan flip-flop 1 at the $(i-1)$th shift cycle. The ith scan flip-flop begins to receive random signals shifted from the scan-in from the ith clock cycle to the kth clock cycle. As for the scan flip-flop k, it does not receive random signals until the kth shift cycle. The scan flip-flops without arrows in Fig. 1 receive random signals and apply them to the circuit.

All primary outputs receive test responses at all clock cycles, whereas the pseudoprimary inputs (PPIs) receive test responses only at the capture cycles. Signal probabilities of the PPIs cannot be thought of as 0.5 during the shift cycles. We want to estimate controllability of the PPIs and observability of the PPOs. The location of a scan flip-flop in a scan chain does have impact on its testability. We consider the ith scan flip-flop in a scan chain. As for the $(k+1)$th clock cycle (capture cycle) of the test cycle t $(t \geq 1)$, its controllability is the controllability of its data input in the kth clock cycle. Testability for all internal nodes can be estimated based on the controllability/observability programs (COP) measure [4].

Let the length of the scan chains be k. As shown in Fig. 2, each test cycle is partitioned into four different phases. A test cycle for the conventional *test-per-scan* test scheme contains: 1) k shift cycles and 2) the capture cycle. The shift cycles of each test cycle are further partitioned into three parts for the ith scan flip-flop: 1) the first $(i-1)$ shift cycles, 2) the shift cycles after the $(i-1)$th clock cycle, except the kth shift cycle, and 3) the kth clock cycle. As shown in Fig. 2, the $(k+1)$th clock cycle is the capture cycle.

Let us consider the controllability of the PPIs of the ith $(i > 1)$ scan flip-flop during test cycle t $(t > 1)$. Its signal probability of the jth clock cycle $(1 \leq j \leq i-1)$ is the signal probability of the $(i-j)$th scan flip-flop at the capture cycle of test cycle $(t-1)$. The signal probability of the ith scan flip-flop after the $(i-1)$th shift cycle is 0.5 because it receives random signals during the remaining shift cycles. Therefore, it is not good to consider controllability of the PPIs as 0.5 for all shift cycles.

The observability of the PPOs (inputs of the scan flip-flops) is 0.0 during the first $(k-1)$ shift cycles, as shown in Fig. 1. It is noted that the observability of the input of a scan flip-flop at the kth clock cycle is the same as the observability of its output at the $(k+1)$th clock cycle because the value of the input of the flip-flop is propagated to its output at the $(k+1)$th clock cycle, which is used as a test at the capture cycle. As for the last phase, which is the



clock cycle classification	clock cycle	C 1(PI)	C 1(PPI) for the i th sff	O(PO)	O(PPO)
shift	$0 < j < i$	0.5	C 1 (PPO) of the $(i-j)$ th sff at the capture cycle of $(t-1)$ test cycle	1.0	0.0
shift	$i-1 < j < k$	0.5	0.5	1.0	0.0
shift	$j=k$	0.5	0.5	1.0	O(PPI) in the next clock cycle
capture	$j = k+1$	0.5	C 1 (PPO) in the k th cycle	1.0	1.0

Fig. 2. Testability estimation of the tth test cycle for the *test-per-scan* BIST scheme.

$(k+1)$th clock cycle, the controllability of the output of the scan flip-flop is the same as its input's controllability at the kth clock cycle. Furthermore, the observability of the input of a scan flip-flop is 1.0, whose value will be captured and shifted out through the scan chain during the shift cycles of the next test cycle. The observability of the primary outputs is 1.0 for all clock cycles. The testability of the circuit during the capture cycles is estimated for the original circuits. However, the testability estimation of the circuit based on the COP measure can converge quickly because the testability of the PPIs of the scan flip-flops has the constraints, as shown in Fig. 2. The observability of the PPIs can be improved if more capture cycles are inserted in the process of scan shift, but not after all scan shift cycles. Weighted test vectors can also be applied to the PPIs in this case. Testability estimation using this test scheme should be similar to the one stated above. Note that all scan chains for the conventional *test-per-scan* test scheme are set to the same mode at any time because they share the same scan enable signal.

3 Testability Features of the Proposed Test Scheme

The proposed test scheme uses different scan enable signals to control different scan chains, as shown in Fig. 3, when the circuit is set to the *test* mode, where weights $w_1, w_2, \ldots, w_k \in \{0.5, 0.625, 0.75, 0.875\}$. Different values are assigned to different scan enable signals of separate scan chains at the same clock cycle. Therefore, testability is studied corresponding to different scan chains. Testing with respect to each scan chain can still be partitioned into test cycles where neither the number of shift cycles nor the number of capture cycles contained in each test cycle is fixed. Let k be the length of the scan chains, and k' and k'' be the number of shift cycles contained in the t and $t+1$ test cycles, as presented in Fig. 4. It should be noted that k' and k'' can be greater than or less than k. The

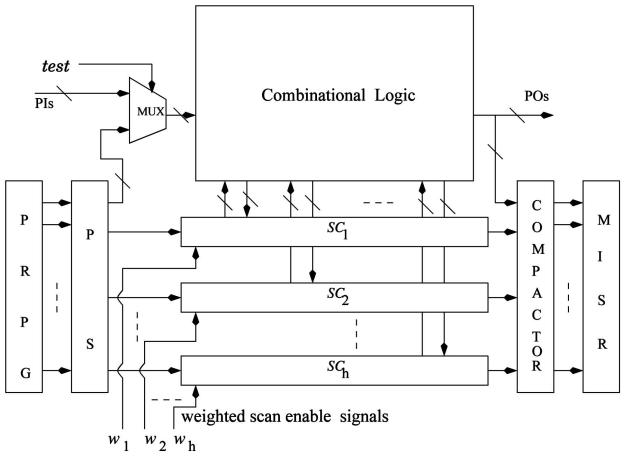


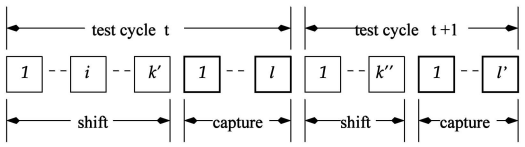
Fig. 3. The new scan-based BIST architecture with weighted scan enable signals.

testability of the scan flip-flops is also closely related to the next test cycle.

As shown in Fig. 4, two consecutive test cycles are presented. The first test cycle contains k' shift cycles and l capture cycles. Moreover, the second test cycle contains k'' shift cycles and l' capture cycles. Testability estimation during a test cycle is partitioned into five phases for the ith scan flip-flop if $i < k'$. Otherwise, the testability estimation of the ith scan flip-flop contains only the first, fourth, and fifth phases, as presented in Fig. 4, if $i > k'$.

The ith scan flip-flop receives the $(i-j)$th scan flip-flop captured at the last test cycle; therefore, the testability measure is the same as that of the $(i-j)$th scan flip-flop's PPO for $1 \le j \le i-1$ clock cycles. Its testability measure is 0.5 from clock cycle i to k'. As for the testability of the scan flip-flops during clock cycles $k'+1$ to $(k'+l-1)$, the signal probability of the PPI is the signal probability of its data input in the last clock cycle and the observability of the PPO is the observability of its output for the next clock cycle.

As for the last clock cycle, the signal probability of the PPI is the same as the previous capture cycles; however, the



feature	clock cycles	C 1(PI)	C 1 (PPI) of the ith sff	O(PO)	O(PPO)
shift	$0 < j < i$	0.5	C 1 (PPO) of the $(i-j)$th sff at the last capture cycle of the $(t-1)$th test cycle	1.0	0.0
shift	$i-1<j< k'$	0.5	0.5	1.0	0.0
shift	$j=k'$	0.5	0.5	1.0	O(PPI) in the next clock cycle
capture	$k' < j < k'+l$	0.5	C 1(PPO) in the last clock cycle	1.0	O(PPI) in the next clock cycle
capture	$j = k'+l$	0.5	C 1(PPO) in the last clock cycle	1.0	uncertain

Fig. 4. Testability of the tth test cycle for the two consecutive test cycles.

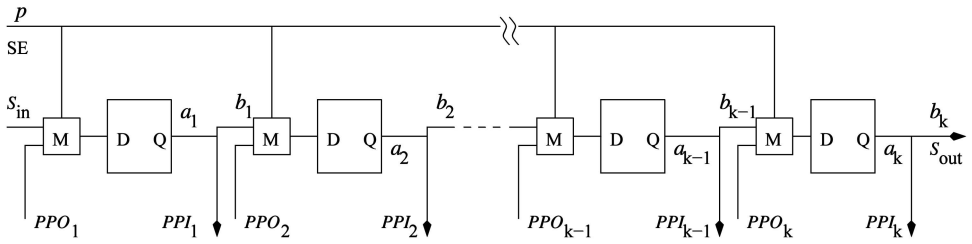


Fig. 5. A scan chain with a weighted scan enable signal.

observability of the PPO is determined by its location and the number of shift cycles contained in the next test cycle. Consider the test schemes in [9], [19], the observability of the PPO must be 1.0 because the number of shift cycles in the next test cycle is equal to the length of the scan chain, that is, the test response captured at the scan flip-flop can always be propagated to the scan-out signal of the scan chain. In our test scheme, the observability of the PPO is 1.0 if the number of shift cycles in the next test cycle is greater than or equal to $k - i$, where i is the location of the scan flip-flop in the scan chain and k is the length of the scan chain. If the number of shift cycles in the next test cycle is less than $k - i$, the observability of the PPO of the scan flip-flop is

$$O(PPO_i) = 1 - (1 - O(PPI_{i+1})) \cdot \ldots \cdot (1 - O(PPI_{i+k''})).$$

That is, the test response captured at the scan flip-flop is propagated to any one of the PPIs $PPI_{i+1}, PPI_{i+2}, \ldots, PPI_{i+k''}$ in this case. Up to now, we can say that the proposed test scheme is actually a generalized test scheme of the ones in [9], [19] with multiple capture cycles. According to our method, neither the number of shift cycles nor the number of capture cycles is fixed. Testability estimation for the $(t+1)$th test cycle is similar, which is still partitioned into five separate phases, as shown in Fig. 4.

4 Testability Estimation for the Proposed Test Scheme

Testability is calculated using the scheme shown in Fig. 3 for the scan chains with weighted scan enable signals. Testability estimation for a scan chain with a weighted scan enable is presented in this section. Controllability estimation based on the test scheme is introduced in Section 4.1 and observability estimation is presented in Section 4.2.

4.1 Controllability Estimation

As shown in Fig. 5, a weight p is assigned to the scan enable signal of the scan chain. The signals PPI_i and PPO_i are the PPIs and PPOs of the ith scan flip-flop for $i = 1, 2, \ldots, k$. The signal probability of the signal PPI_1 can be calculated as follows:

$$C_1(PPI_1) = \frac{1}{2} \cdot p + C_1(PPO_1) \cdot (1 - p), \quad (1)$$

where p is the weight of the scan enable signal. In (1), the first term on the right-hand side indicates the probability of the signal PPI_1 getting a value 1 by the pseudorandom input S_{in} when the scan chain is set to the test mode and the second term represents the probability of assigning value 1 to the signal PPI_1 by its data input PPO_1 when the scan chain is controlled to the functional mode. The signal probability of PPI_2 can be calculated as follows:

$$C_1(PPI_2) = p \cdot C_1(a_1) + C_1(PPO_2) \cdot (1 - p), \quad (2)$$

where $C_1(a_1) = C_1(PPI_1)$. The first term in the right-hand side of (2) represents the probability of the PPI PPI_2 being set to value 1 when the scan chain is set as the test mode and the second term stands for the probability of the signal PPI_2 being assigned a value 1 by its data input when the scan chain is controlled to the functional mode. Similarly, we can obtain the testability measure of signal PPI_k as follows:

$$C_1(PPI_k) = p \cdot C_1(a_{k-1}) + (1 - p) \cdot C_1(PPO_k), \quad (3)$$

where $C_1(a_{k-1}) = C_1(PPI_{k-1})$. Signal probability calculation for other combinational nodes is the same as the conventional *test-per-scan* BIST using the COP [4] measure.

4.2 Observability Estimation

The observability measures of all nodes corresponding to the scan chain with the weighted scan enable signals can be obtained as follows: First, let us consider the last scan flip-flop, as shown in Fig. 5:

$$O(a_{k-1}) = 1 - (1 - O(PPI_{k-1})) \cdot (1 - O(b_{k-1})), \quad (4)$$

$$O(b_{k-1}) = p \cdot O(a_k) = p, \quad (5)$$

$$O(PPO_k) = O(a_k) \cdot (1 - p) = 1 - p. \quad (6)$$

In (4), we think the fault effect on a_{k-1} can be observed if it can be observed from either PPI_{k-1} or b_{k-1}. The fault effect on b_{k-1} can be observed if the node a_k is observable and the scan chain is set as a test mode. The fault effect on the PPO of the kth scan flip-flop is observable if the node a_k is observable and the scan chain is set to the functional mode. The observability corresponding to the second scan flip-flop can be calculated as follows:

$$O(a_2) = 1 - (1 - O(PPI_2)) \cdot (1 - O(b_2)), \quad (7)$$

$$O(b_2) = p \cdot O(a_3), \quad (8)$$

$$O(PPO_2) = O(a_2) \cdot (1 - p). \quad (9)$$

Similarly, the observability of signals corresponding to the first scan flip-flop can be calculated as follows:

$$O(a_1) = 1 - (1 - O(PPI_1)) \cdot (1 - O(b_1)), \quad (10)$$

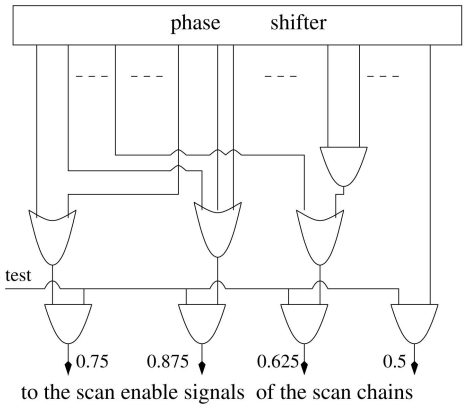


Fig. 6. Logic to generate different weights for the scan enable signals of the scan chains.

$$O(S_{in}) = p \cdot O(a_1), \tag{11}$$

$$O(PPO_1) = O(a_1) \cdot (1 - p). \tag{12}$$

Equations (1)-(12) can be utilized to evaluate the cost function, to be presented later in Section 5, which is used to select weights for all scan chains by minimizing the cost function. Assume that the BIST process is partitioned into multiple test sessions; the weights assigned to the scan enable signals of the scan chains can be updated after each session. This technique can further improve the test effectiveness of the scan-based BIST scheme.

5 Selecting Weights for the Scan Enable Signals of the New Scan-Based BIST Architecture

The architecture of the proposed test scheme is presented in Fig. 3 when the circuit is set to test mode. All weighted signals are assigned to the scan enable signals during test. In the scan-based architecture, as shown in Fig. 3, different weights, $w_1, w_2, \ldots,$ and w_k, are assigned to the scan enable signals of the scan chains $SC_1, SC_2, \ldots,$ and SC_k, respectively, where $w_1, w_2, \ldots, w_k \in \{0.5, 0.625, 0.75, 0.875\}$. The reason why we do not assign any weight less than 0.5 to the scan enable signals is that we do not want to insert more capture cycles than scan shift cycles. An effective method is presented to select weights for the scan enable signals of the scan chains. Selection of the weights on the scan enable signals of the scan chains is determined by the following testability cost function:

$$G = \sum_{l/i \in F} \frac{|C_1(l) - C_0(l)|}{O(l)}, \tag{13}$$

where l/i represents the stuck-at i ($i \in \{0, 1\}$) fault at line l. In (13), F is the random resistant fault set that contains the faults whose detection probability is no more than 10 times that of the hardest fault [3]. Note that (13) does not consider redundant faults according to a deterministic test generator. Our method tries to minimize the cost function, as given in (13).

As shown in Fig. 6, a simple BIST control logic assigns weighted pseudorandom signals to the scan enable signals. The circuit is set to the functional mode when the extra pin *test* is assigned value 0. The circuit is set to the test mode when the extra pin *test* is set to value 1. In this case, the selected weight is assigned to the corresponding scan chain. The scan chain works under the shift mode when the weighted scan enable signal is 1 and works under the capture mode when the scan enable signal is set to value 0. The weighted signals are produced by a phase shifter, as presented in Fig. 6. Only one extra pin is necessary in the scan-based BIST design.

Our method does not need to insert complex hardware into the original circuit in order to generate different weights for the scan enable signals of the scan chains. The weighted signals assigned to the scan enable signals of the scan chains can be generated easily, as in [3]. As shown in Fig. 6, the biased signals of weights 0.625, 0.75, and 0.875 can be generated as follows: The signal of weight 0.625 can be produced by connecting two pseudorandom signals with a 2-input AND gate whose output is connected with a 2-input OR gate. Another input of the OR gate is a pseudorandom signal. The biased signal of weight 0.75 can be obtained from the output of a 2-input OR gate whose inputs are pseudorandom signals. The signal of weight 0.875 can be obtained from the output of the 3-input OR gate whose inputs are pseudorandom signals. The weights for the scan enable signals of the scan chains are determined once and for all. That is, the weights do not need to be updated in the process of testing. The extra logic to generate the weights for the test scheme consists of only the four gates, as presented in Fig. 6, which introduces a trivial area overhead compared to the previous weighted test pattern generators. As shown in Fig. 6, four extra AND gates are connected with different weights, respectively, where the four 2-input AND gates are connected to the *test* signal and the weighted signals. The circuit turns to operational mode when *test* is set to 0 and all weights are assigned to the scan chains when *test* is set to 1. The circuit turns to test mode when *test* is set to 1.

Let all scan chains be assigned separate scan enable signals. We consider assigning one of the following weights, {0.5, 0.625, 0.75, 0.875}, to the scan enable signals of the scan chains. In the weight selection procedure, S is the scan chain set and SC is a specific scan chain. Initially, S contains all scan chains in the circuit and the scan enable signals of all scan chains are assigned those of the regular test-per-scan test scheme. Initially, controllability of the PPI of the ith scan flip-flop is set to $0.5 \cdot (k - i + 1)/(k + 1)$ and the observability of the PPO of the ith scan flip-flop is set to $1/k$, as presented in Section 2. Iterative testability estimation is used for all nodes based on (1)-(12) and the COP measure [4]. It is found that the testability measures for all nodes become stable very quickly.

The procedure to determine weights can be illustrated as follows: First, all scan chains use the common *test-per-scan* scan enable signals. That is, scan enable signals are set to 1 in scan shift cycles and set to 0 in capture cycles. A test cycle for the original scan enable signals contains k scan shift cycles followed by one capture cycle, where k is the length of the longest scan chain. Our method selects a weight for the first scan-chain scan enable signal to minimize the cost function. After the best weight has been selected for the first scan chain, our method selects the best weight for the scan enable signal of the second scan chain that minimizes the cost function, as presented in (13). For each scan chain, if no

select-weight-for-scan-enables()
{
1) Assign the same values to the scan enable signals as the regular test-per-scan BIST scheme to all scan segments.
2) While the scan chain set $S \neq \emptyset$, do
   a) Select a scan chain SC from the scan chain set S, $S = S - \{SC\}$.
   b) For each weight in $\{0.5, 0.625, 0.75, 0.875\}$, testability estimation is adopted to evaluate the cost function as presented in Equation (13).
   c) Select the best weight $w \in \{0.5, 0.625, 0.75, 0.875\}$ that makes the cost function as presented in Equation (13) minimum.
   d) For each scan chain, if no weight can be selected, just leave its scan enable signal as the one in the conventional test-per-scan test scheme.
}

Fig. 7. Procedure to select different weights for the scan enable signals of the scan chains.

weight can be selected, just leave its scan enable signal as the one in the conventional test-per-scan BIST scheme. Continue the above process until proper weights have been chosen for all scan enable signals of the scan chains.

The detailed procedure to determine weights for the scan enable signals is presented in Fig. 7. The details to calculate the testability measure of the circuit have been introduced in Sections 2 and 3. Different weights can be obtained by connecting two or more pseudorandom signals, as presented in Fig. 6.

Our method sets the length of the scan chains as 10 in order to be compatible with [9], [19], therefore, there may be a lot of scan chains. Let the outputs of all scan chains and the primary outputs be connected to the multiple input signature analyzer (MISR) directly. This may make the size of the MISR very large. Multiple scan chains or primary outputs can be connected with XOR gates, whose outputs are connected with the MISR in order to reduce the size of the MISR [23]. The following principle is adopted to merge two primary outputs to a single stage for the MISR: Two primary outputs can be connected with an XOR gate and they are merged into the same stage if two primary outputs have no common combinational predecessor. This causes no degradation in the fault coverage.

The principle to merge two scan chains into a single stage of the MISR is similar to primary output merging, which can be stated as follows: Let $(v_{1,1}, v_{1,2}, \ldots, v_{1,k})$ and $(v_{2,1}, v_{2,2}, \ldots, v_{2,k})$ be two scan chains, where k is the scan-chain length and $v_{i,j}$ is a scan flip-flop. Scan-out signals of two scan chains can be connected with an XOR if scan flip-flops in each of the pairs $(v_{1,1}, v_{2,1}), (v_{1,2}, v_{2,2}), \ldots, (v_{1,k}, v_{2,k})$ do not have any common combinational predecessor, respectively. This technique is similar to the one presented in [23]. However, no degradation in fault coverage incurs using the above technique to merge multiple scan chains into the same stage. The scan-chain length is set to 10 for most results to be presented in this paper. We shall also present the results of our method compared with previous methods when the scan-chain length is set to other values in Section 6.

TABLE 1
Comparison with Previous Methods

circuits	FC	CPU	TPC	without test points				with test points			
				WTS	MTS	TTS	STS	ntp	WTS	MTS	STS
s1269	100	0.1	100	99.87	98.99	99.31	98.99	—	—	—	—
s1423	99.1	0.2	99.08	99.25	98.95	99.25	98.30	5	99.3	99.2	98.9
s1512	100	0.2	96.02	96.92	96.86	96.28	96.28	5	98.3	97.9	97.3
s3271	100	1.0	100	99.95	99.57	99.91	98.25	—	—	—	—
s3330	100	0.8	92.68	97.58	94.33	94.41	91.51	5	99.6	98.4	97.7
s3384	100	1.1	96.54	97.65	97.62	97.87	96.36	5	98.3	97.7	97.5
s4863	100	1.0	99.94	100	99.25	99.29	97.54	—	—	—	—
s5378	99.1	1.5	98.98	99.30	98.93	98.89	98.18	6	99.3	99.2	98.8
s9234	93.7	12.7	90.43	91.88	90.70	89.71	88.02	20	93.7	93.6	92.5
s13207.1	98.5	53.9	97.76	98.55	97.31	98.10	97.31	20	98.8	98.1	98.1
s15850	96.7	59.3	94.56	95.01	93.86	93.85	93.64	15	97.3	96.5	96.2
s15850.1	96.7	61.4	94.71	95.42	94.12	94.01	93.48	15	97.5	96.6	96.3
s38417	99.5	683	96.72	98.24	97.06	97.26	95.85	15	99.3	98.9	98.1
s38584	95.9	536	96.31	96.33	95.91	95.88	95.46	13	97.3	97.1	96.8
b14	99.3	51.4	92.05	92.12	91.49	91.62	89.93	15	94.7	94.2	92.7
b20	99.2	243	93.36	95.41	94.00	94.70	93.28	20	96.6	95.5	94.2
b21	99.1	247	92.06	93.39	93.01	94.26	91.83	20	96.4	95.6	94.8
b22	99.4	633	93.62	94.99	94.37	94.80	93.54	20	96.9	95.7	94.7

6 Experimental Results

The proposed weighted-test-signal-based (WTS) method has been implemented with a Sun Blade 2000 workstation. A pseudorandom test pattern generator (PRTG) of 24 stages is used to generate test patterns for all circuits. The PS is implemented according to Rajski et al. [16]. All experimental results are collected after 500k clock cycles. All extra faults of the design for testability (DFT) logic are excluded and all methods use the same PS and PRTG in order to present a fair comparison.

The PROOFS fault simulator [15] is used for all fault simulation work in this paper. Our method needs sequential fault simulation in many cases. This can increase the CPU time to do fault simulation. However, test stimuli are assigned to the primary inputs and PPIs for any clock cycle instead of only primary inputs, like fault simulation for synchronous sequential circuits. Therefore, CPU time to do fault simulation for the proposed test scheme is still close to the conventional test-per-scan scheme (STS) and other two multiple capture cycle test schemes. The two multiple capture test schemes [9], [19] also need to do sequential fault simulation.

Comparison of our method with the MTS [19], TTS [9], and the STS schemes is presented in Table 1. The MTS [19] method is implemented and the test vector sets for different circuits are generated based on the obtained test schemes. The MTS, TTS, and STS test schemes still use the PS in [16] to generate tests. The TTS is implemented completely. The results of TTS are quite compatible with those presented in [9], while the results of MTS are much better than those given in [19] for most circuits.

The parameters CPU, FC, and TPC in Table 1 stand for the CPU time (seconds) to select the weights for the scan enable signals, fault coverage for the fully scanned circuit, and the fault coverage of the test-per-clock (TPC) test scheme with 500k clock cycles. That is, the fault coverage of the TPC scheme for all circuits is obtained after running

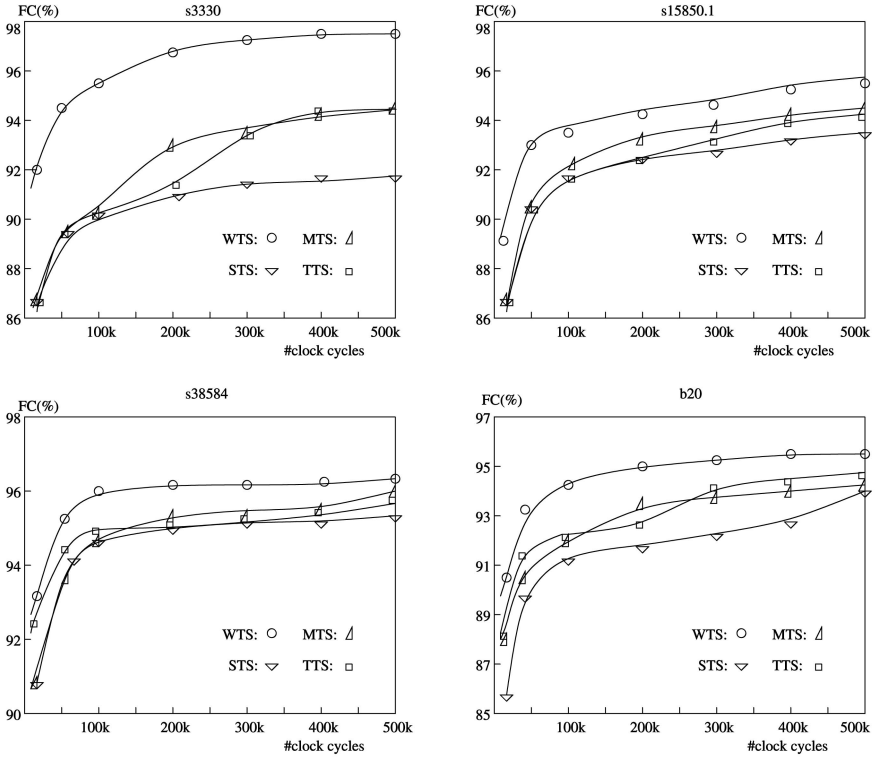


Fig. 8. Fault coverage curves of the four BIST schemes.

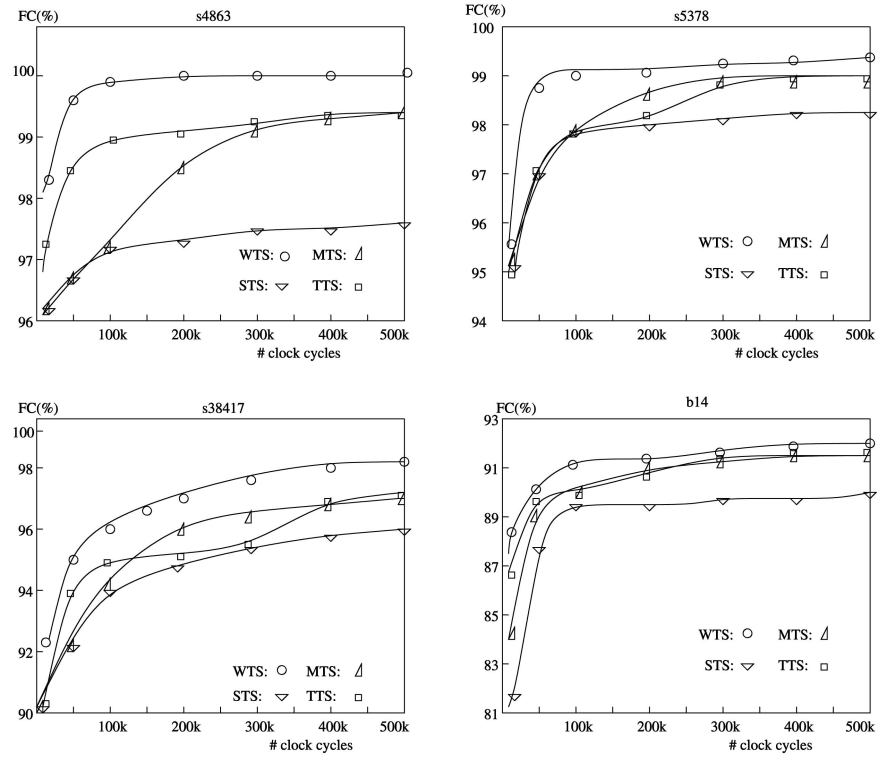


Fig. 9. Fault coverage comparison of the four BIST schemes.

500,000 random test patterns. Each stage of the PPIs of the circuit is connected to the phase shifter [5] and the PPOs of the circuit are completely observable for the TPC test scheme for all clock cycles. Therefore, 500k random patterns are used for the TPC test scheme. It is shown that the fault coverage of the TPC test scheme is a little better than the STS test scheme for all circuits except s1512 and worse than that of the WTS scheme for all circuits except s3271. The conventional STUMPS [3], [5] test scheme is the same as the STS scheme presented in Table 1. The results of the STUMPS scheme can be much worse when no PS is combined.

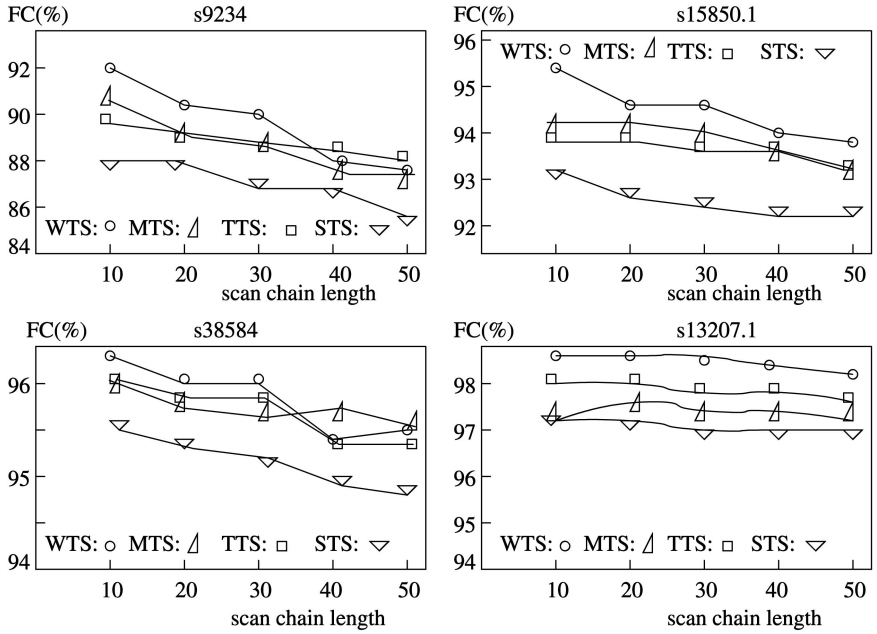


Fig. 10. Fault coverage comparison with variable scan-chain lengths.

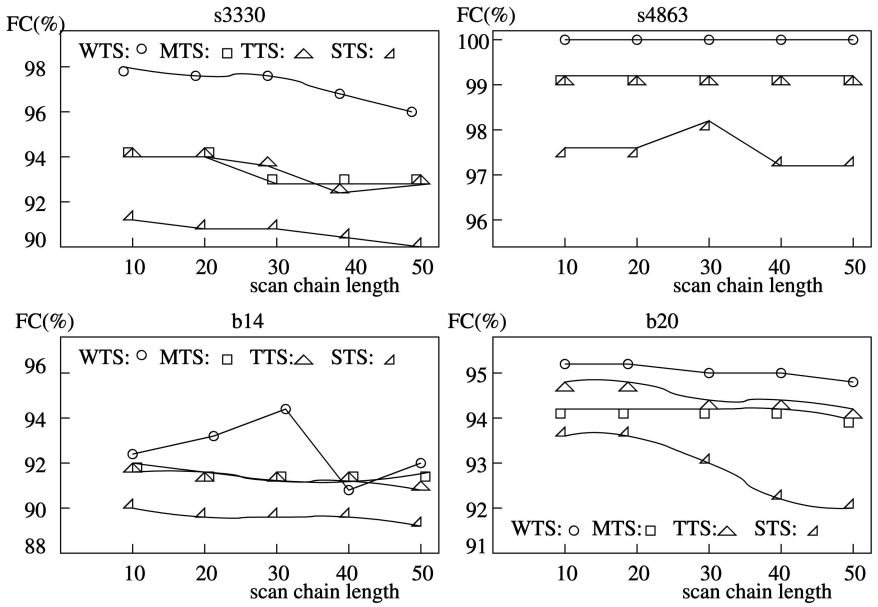


Fig. 11. Comparison of the four test schemes with variable scan-chain lengths.

WTS, MTS, and TTS get better fault coverage for all circuits than the STS when no test point is inserted. WTS apparently gets better results than STS and MTS for all circuits. Compared to the TTS test scheme, our method gets better fault coverage for all circuits except circuits s3384 and b21. Comparison of WTS with MTS and STS is also presented in Table 1 after a number of test points have been inserted. The WTS works better than MTS and STS for all circuits with test points.

Fig. 8 presents a fault coverage comparison of four BIST schemes with the number of clock cycles from 50k to 500k. The results for circuits s3330, s15850.1, s38584, and b20 are presented. The curves show that the proposed method consistently gets better fault coverage than all other methods. Fault coverage of MTS and TTS changes quickly when they turn to different test sessions. As for circuit s3330, the fault coverage difference reaches up to 6 percent when the number of clock cycles is set to 150k. The MTS and TTS schemes use the same test set as the STS scheme in the earlier stage for the circuit s15850.1. This is mainly because the MTS and TTS schemes use three and two separate test sessions for both circuits, respectively. The MTS scheme is partitioned into four different test sessions for circuit b20. However, the fault coverage with MTS on b20 changes sharply when it turns from the first test session to the second.

Fig. 9 presents a fault coverage comparison of four BIST schemes with the number of clock cycles ranging from 50k to 500k for circuits s4863, s5378, s38417, and b14. The curves

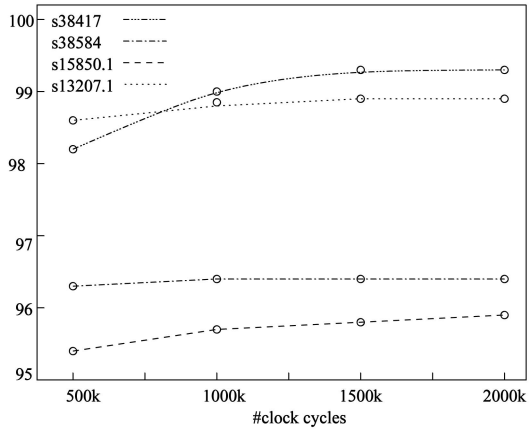


Fig. 12. Fault coverage of the WTS scheme for variable test lengths.

show that the proposed method consistently obtains better fault coverage than the previous methods for all four circuits.

Figs. 10 and 11 present performance comparison among WTS, STS, MTS, and TTS when the length of the scan chains varies from 10 to 50. For circuits s15850.1 and s13207.1, WTS always gets better fault coverage than all of the other three methods for any scan-chain length. The WTS method obtains a little worse fault coverage for circuit s38584 than MTS when the scan-chain length is set to 40 or 50. As for circuit s9234, WTS obtains slightly worse results than TTS when the scan-chain length is set to 40 or 50. WTS always gets better fault coverage than all of the other three methods for any scan-chain length except circuit b14 when the scan chain length is 40.

Fig. 12 presents the performance of the proposed WTS scheme for circuits s13207.1, s15850.1, s38417, and s38584 when test length varies from 500k clock cycles to 2,000k clock cycles. Circuit s38417 consistently gets better fault coverage when the test length increases. The fault coverage for s38417 has been up to 99.3 percent when the test length is 2,000k clock cycles, which has been very close to the complete coverage 99.47 percent for this random resistant ISCAS89 circuit. It seems that all four circuits have reached complete coverage or close to complete coverage when the test length is set to 2,000k clock cycles.

Table 2 presents the required test length for the STS, MTS, and TTS test schemes to reach the same fault coverage as the WTS scheme. In Table 2, parameter #cyc represents the number of clock cycles. Parameter WTS represents the fault coverage of the WTS scheme when the test length is set to 500k clock cycles. The fault simulator stops at 1,500k clock cycles when the fault coverage for all three test schemes, STS, MTS, and TTS, still cannot reach the same fault coverage as that of the WTS scheme.

TABLE 2
Test Length Comparison with Previous Methods

circuits	WTS	STS		MTS		TTS	
		FC(%)	#cyc	FC(%)	#cyc	FC(%)	#cyc
s5378	99.30	99.30	1256k	99.30	825k	99.30	988k
s9234	91.88	90.58	1500k	91.79	1500k	91.08	1500k
s13207.1	98.55	98.55	758k	98.55	851k	98.55	665k
s15850.1	95.42	94.32	1500k	95.42	1280k	95.13	1500k
s38417	98.24	96.29	1500k	97.47	1500k	98.03	1500k
s38584	96.33	96.27	1500k	96.33	1230k	96.33	1350k
s3330	97.58	94.27	1500k	96.67	1500k	96.89	1500k
s4863	100	99.52	1500k	100	928k	100	872k

TABLE 3
Test Length Comparison with the Conventional Test-per-Scan Scheme

circuits	PIs	POs	FFs	STS		WTS		red.
				FC(%)	#cyc	FC(%)	#cyc	(%)
s1269	18	10	37	98.99	28063	98.99	754	97.31
s1423	17	5	74	98.30	238515	98.30	9599	95.98
s1512	29	21	57	96.28	340722	96.28	80361	76.41
s3271	26	14	116	98.25	249470	98.27	3749	98.50
s3330	40	73	132	91.51	468605	91.52	7998	98.29
s3384	43	26	183	96.36	422008	96.38	1145	99.73
s4863	49	16	104	97.54	473761	97.56	3810	99.20
s5378	35	49	179	98.18	398035	98.18	32478	91.84
s9234	19	22	228	88.02	489947	88.04	39215	92.00
s13207.1	62	152	638	97.31	497372	97.31	77713	84.38
s15850	14	87	597	93.64	451733	93.64	58902	86.96
s15850.1	77	150	534	93.48	412391	93.48	89263	78.35
s38417	28	106	1636	95.85	492938	95.88	84809	83.2
s38584	12	278	1452	95.46	476061	95.46	40375	91.52
b14	32	54	—	89.93	471393	89.93	18122	96.16
b20	32	22	490	93.28	495103	93.28	63025	87.27
b21	32	22	490	91.83	428009	91.83	54201	87.34
b22	32	22	735	93.54	481618	93.55	129216	73.17
average	—	—	—	94.88	—	94.88	—	89.87

Table 3 presents the test length comparison of the proposed method with the conventional STUMPS (also the STS scheme) test scheme. The number of clock cycles (#cyc) for the STS scheme to reach the final fault coverage of the 500k clock cycles is recorded and the number of clock cycles for the WTS scheme to reach the same fault coverage is also presented. The greatest test length reduction (red.) reaches up to 99.7 percent and the least test length reduction is also more than 73 percent.

7 Conclusions

A method to generate weighted pseudorandom vectors for the PPIs was proposed by assigning different weights to the scan enable signals of the scan chains. The proposed method does not need to design a complex weighted test generator, modify the scan flip-flops, or store multiple weight sets on-chip. Neither the number of shift cycles nor the number of capture cycles for each test cycle is fixed based on the new test generation method. The proposed method needs only one test session, which makes the control logic and control scheme very simple. Experimental results showed that the method works better than two recent scan-based BIST schemes using multiple capture cycles for each test cycle and the conventional *test-per-scan* test scheme with a single capture cycle. The authors would like to express their thanks to Yang Zhao for his presentation of a part of the experimental results in this paper.

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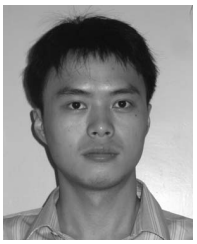

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