PAPER

NoC-Compatible Wrapper Design and Optimization under Channel-Bandwidth and Test-Time Constraints

Fawnizu Azmadi HUSSIN[†a)], *Nonmember*, Tomokazu YONEDA[†b)], *Member*, *and* Hideo FUJIWARA[†c)], *Fellow*

SUMMARY The IEEE 1500 standard wrapper requires that its inputs and outputs be interfaced directly to the chip's primary inputs and outputs for controllability and observability. This is typically achieved by providing a dedicated Test Access Mechanism (TAM) between the wrapper and the primary inputs and outputs. However, when reusing the embedded Network-on-Chip (NoC) interconnect instead of the dedicated TAM, the standard wrapper cannot be used as is because of the packet-based transfer mechanism and other functional requirements by the NoC. In this paper, we describe two NoC-compatible wrappers, which overcome these limitations of the 1500 wrapper. The wrappers (Type 1 and Type 2) complement each other to optimize NoC bandwidth utilization while minimizing the area overhead. The Type 2 wrapper uses larger area overhead to increase bandwidth efficiency, while Type 1 takes advantage of some special configurations which may not require a complex and high-cost wrapper. Two wrapper optimization algorithms are applied to both wrapper designs under channel-bandwidth and test-time constraints, resulting in very little or no increase in the test application time compared to conventional dedicated TAM approaches.

key words: *SoC testing, NoC testing, test wrapper design, NoC-compatible wrapper*

1. Introduction

The rapid increase in design complexity of System-on-Chip (SoC) devices and the short time-to-market pressure accelerate SoC adoption. Manufacturing tests are also becoming increasingly complex and expensive. The best-adopted test technology for SoCs is based on the use of a Test Access Mechanism (TAM) [1]–[3] to connect all the embedded Cores-Under-Test (CUT) to the external Automatic Test Equipment (ATE). Core-based tests require that the CUTs be isolated; this is typically achieved by wrapping the cores with IEEE 1500 [4] compatible wrappers. Various core test scheduling methodologies based on the dedicated TAM have been proposed [1], [3].

Success of a design relies on the use of appropriate design and process technology, as well as the ability to efficiently interconnect all the components. As design complexity has increased, the interconnects have evolved from a single bus to multiple hierarchical buses, and recently to Networks-on-Chip (NoC) [5]. The effectiveness of the Internet Protocol networks inspired the birth of the NoC, since it can provide large on-chip bandwidth for inter-core communications; its modular infrastructure eases the transition effort from the traditional bus-based architecture. In [5], the authors highlighted several pioneer NoC architectures as well as the test-related challenges that must be overcome to promote the adoption of NoC as an SoC interconnect.

In this paper, we analyze two types of NoC-compatible wrappers, based on the guaranteed bandwidth and latency of the NoC. The first wrapper, Type 1, is based on the NoC-compatible wrapper proposed in [6], [7]. Depending on the number of wrapper scan chains, the test application time (TAT) of the Type 1 wrapper could be shorter or longer than that of the IEEE 1500 standard wrapper; however, for most cases some NoC bandwidth is wasted. We then propose a second NoC-compatible wrapper, Type 2, that is 100% bandwidth efficient—i.e. no wasted bandwidth; Type 2's TAT is the same as that of the 1500 wrapper. For a given bandwidth or test application time constraint, the proposed wrapper optimization algorithm finds the best configuration using a fast binary search algorithm. Compared to [6], [7], our proposed test wrapper with the optimization scheme is more efficient in terms of both reducing the test application time and NoC bandwidth utilization; this is demonstrated by the experimental results reported in this paper.

We begin with a review of some related work in Sect. 2. The NoC model and the IP core model are described in Sects. 3 and 4, respectively. In Sect. 5, a detailed description of the proposed NoC-compatible wrapper architecture is given. The wrapper optimization methodology is explained in Sect. 6. Some experimental results on selected benchmark circuits are given in Sect. 7. Finally, concluding remarks are offered in Sect. 8

2. Related Work

In this paper, we will consider the Æthereal [8], [9] NoC, as an example, which provides abundant communication resources. Therefore, the use of a dedicated TAM for testing of an NoC-based chip is expensive. As a result, the reuse of functional on-chip resources for test purposes is becoming more practical and more economical. Several research groups have published work on NoC test scheduling [10]–[12] utilizing the NoC as the delivery path for the transport of the test data from external tester to the CUTs. Test scheduling for the NoC router [12], [13] and crosstalk test

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[†] The authors are with the Graduate School of Information Science, Nara Institute of Science and Technology, Ikoma-shi, 630–0192 Japan.
a) E-mail: fawniz-h@is.naist.jp
b) E-mail: yoneda@is.naist.jp
c) E-mail: fujiwara@is.naist.jp

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of the interconnects [14] have also been discussed. In these approaches, each CUT is wrapped by an IEEE 1500 compatible wrapper in order to provide isolation and access during the test application.

IEEE 1500 standard wrapper relies on the use of a dedicated TAM, which merely provides an electrical connection between the wrapper and an external tester. When reusing the Networks-on-Chip (NoC) as TAM, the 1500 wrapper cannot be used as is because of three main reasons. (*i*) The packet-based data transfer through the NoC cannot guarantee the precise timing required by the 1500 wrapper. (*ii*) The wrapper does not provide the necessary control signals for both protocol inputs and outputs for successful packet transfer through the NoC. (*iii*) The test data are transferred through a fixed-width data channel, which may result in wasted bandwidth and increased test application time.

In order to overcome these limitations, Amory et al. [6], [7] propose an NoC-compatible wrapper and controller that takes advantage of the guaranteed bandwidth and latency provided by the NoC to ensure test data integrity; this is achieved by using an input interface architecture that interfaces the NoC with the core. Their experimental results showed that in terms of core test time, the proposed NoC-compatible wrapper is comparable to the dedicated TAM-based IEEE 1500 wrapper, while having the advantage of being NoC-reuse [10]–[14] capable. However, due to the constraint of the parallel-serial conversion at the input port, the proposed wrapper requires much higher guaranteed bandwidth on the NoC than the actual rate of the test data loaded into the wrapper scan chains. This is further explained in Sect. 5.2.

3. NoC Model

The proposed wrapper utilizes the functional communication channel between a tester and a CUT. The delivery channel can be a dedicated path or a transparent virtual channel. The wrapper is topology independent; it can be used for any NoC architecture as long as minimum sustainable bandwidth and latency are guaranteed during the test application of the target CUT. The quality-of-service guarantees ensure that the test data are available at the CUT at the right time. In this paper, the Æthereal [8], [9] NoC is used to explain the wrapper design and optimization.

The Æthereal NoC routers [8] provide both guaranteed and best-effort services. The guaranteed throughput (GT) router guarantees uncorrupted, lossless, and ordered data transfer, and both guaranteed latency and throughput over a finite time interval. The GT router uses a slot table to avoid contention on a link, to divide bandwidth per link between connections, and to switch data to the correct outputs. There is a logical notion of synchronicity; all routers on the network are in the same fixed-duration slot. Therefore, in order to guarantee throughput, the connections (i.e. virtual circuits) are allocated time slots; more allocated time slots means more guaranteed bandwidth.

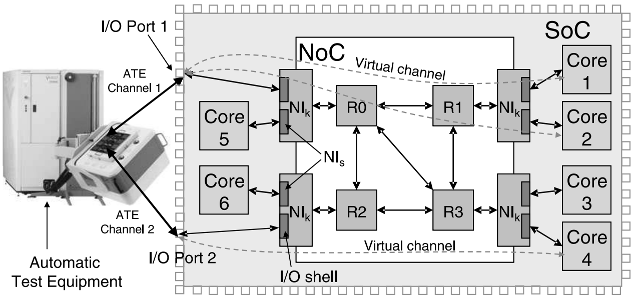


Fig. 1 SoC model based on the Æthereal NoC.

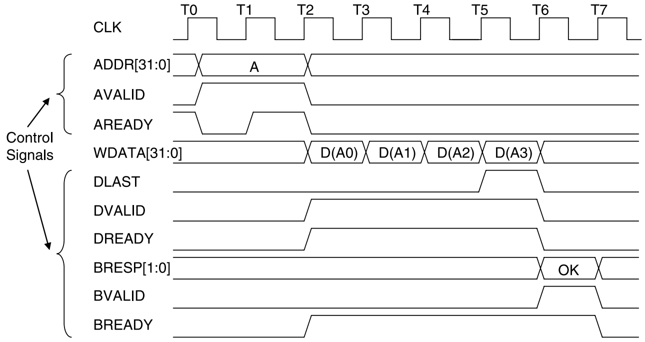


Fig. 2 Transaction-based on-chip communication (Simplified AXI burst-write transaction).

Figure 1 shows an SoC based on the Æthereal NoC, which implements a network interface (NI) [9] between the network routers to the IP cores by means of *shared-memory abstraction.* A transaction-based protocol is implemented in order to provide backward compatibility to existing on-chip communication protocols such as AXI [15] and OCP [16], and allow efficient implementation of future NoC protocols. The NI is split into two components in order to optimize its implementation. The *NI kernel* (NI_k) implements the channel, packetizes messages and schedules them to the routers, implements the end-to-end flow control and clock domain crossings. The *NI shells* (NI_s) implement the specific connections for various on-chip protocols, transaction ordering for connections, and other higher-level issues specific to the protocol offered to the IP.

Figure 1 shows an NoC model based on the Æthereal architecture consisting of four GT routers $R0 - R3$. The NI supports multiple communication protocols required by the IP cores. Two of the NI shells are labeled *I/O port 1* and *I/O port 2*, which can be used to interface the external ATE ports to the NoC. Two virtual channels (VC) are shown connecting the ATE on port 1 to Core 1 and Core 2, respectively. Another VC connects the ATE on port 2 to Core 4. Each VC k is guaranteed a minimum bandwidth, B_{vc_k}, where $\sum_k B^{i,j}_{vc_k} \leq B^{i,j}_{max}$. The term $B^{i,j}_{max}$ represents the maximum link bandwidth between each pair of GT routers R_i and R_j along the VC path. If $B^{i,j}_{vc_k} < B^{i,j}_{max}$ for some link $R_i \rightarrow R_j$, the remaining $B^{i,j}_{max} - B^{i,j}_{vc_k}$ can be allocated to other VCs in order to allow simultaneous test applications of multiple CUTs.

Figure 2 shows a simplified timing diagram of an AXI

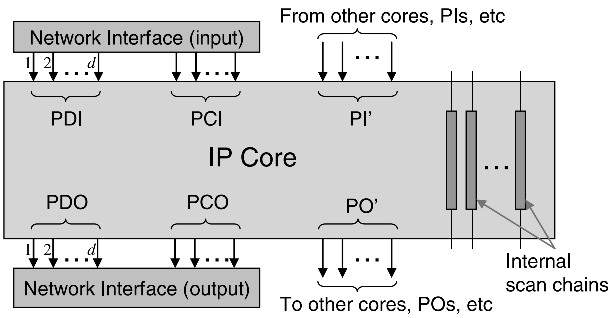


Fig. 3 IP core model with an interface to the NoC's network interface and to other SoC cores and interconnects.

burst write transaction [15]. In order to reuse the NoC during test, the ATE needs to communicate with the CUT using the read/write transactions. The write transaction variables and the IP core model considered in this paper are explained in the next section.

4. IP Core Model

The I/O ports of an IP core under test consist of primary inputs (PI), primary outputs (PO), scan chain inputs (SI) and scan chain outputs (SO). The PIs can be categorized into *primary data input* (PDI) and *primary control input* (PCI). Assuming that the CUT communicates with the NoC by means of the AXI protocol [15] described in Fig. 2, the PDI consists of WDATA[31:0] signals, while PCI consists of ADDR[31:0], AVALID, DLAST, DVALID, and BREADY signals. The POs can also be categorized into *primary data output* (PDO) and *primary control output* (PCO). PDO is made up of RDATA[31:0] signals (not included in the write transaction diagram in Fig. 2), while PCO is made up of AREADY, DREADY, BRESP[1:0], and BVALID signals.

With the new classifications, core I/Os can be categorized as PDI, PDO, PCI, PCO, and other PI/POs (PI'/PO') which are not connected to the communication port of the NoC as shown in Fig. 3. The PDIs and PDOs are used to carry the test vectors from the ATE to the CUT, and the test responses from the CUT to the ATE, respectively. The PCIs and PCOs are needed to operate in the functional mode during the test application to ensure that the read/write transactions, by which the test data and responses are transmitted, execute properly. Since the CUT is not operating in the normal mode, the PCO signals must be generated by a wrapper controller. Special wrapper cells proposed in [7] are used for PCOs to make the NoC operate in the normal mode to transfer the test responses. This is further discussed in Sect. 5.1. For all other PI/POs, the standard IEEE 1500 wrapper boundary register cells are used.

5. NoC-Compatible Wrapper Architecture

Core wrapper design for a dedicated TAM-based test architecture has been explained in [1]–[3]. For a CUT, given k internal scan chains (ISC) of length, $l_1, l_2, \ldots, l_k$, i primary inputs, o primary outputs, b bidirectionals, and n_{sc} wrapper scan chains (WSC), the WSCs are formed while minimizing the maximum scan-in and scan-out depths. *Scan-in elements* consist of zero or more inputs, bidirectionals, and ISCs. *Scan-out elements* consist of zero or more outputs, bidirectionals, and ISCs.

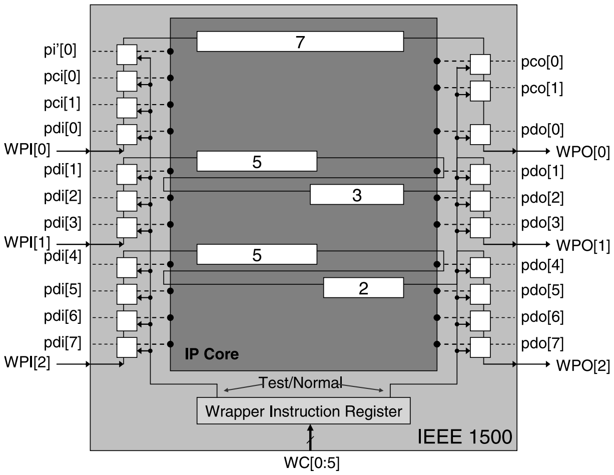


Fig. 4 IEEE 1500 based wrapper with scan chains made up of PI/PO wrapper cells (squares) and internal scan chains (rectangles).

Figure 4 shows $n_{sc} = 3$ for a CUT with $l_k \in [7, 5, 5, 3, 2]$ flip-flops, $i = 11$ ($n_{pdi} = 8$, $n_{pci} = 2$, $n_{pi'} = 1$), $o = 10$ ($n_{pdo} = 8$, $n_{pco} = 2$), and $b = 0$; in this paper, n_x denotes the number of "x" elements. The scan elements are partitioned to form scan chains with *maximum scan-in depth*, $s_i = 11$, and *maximum scan-out depth*, $s_o = 11$, respectively. The wrapper scan chain formation treats the wrapper cells, regardless whether they are data or control I/Os, as identical. The scan chains are formed by cascading input cells, internal scan chains, and output cells together, in the specified order. As a result, the total test application time (TAT) can be calculated by Eq. (1) [2], where n_v is the number of test vectors. For Fig. 4, the TAT is, $T_{TAM} = 12n_v + 11$ clock cycles.

$$T_{TAM} = (max\{s_i, s_o\} + 1) \times n_v + min\{s_i, s_o\} \qquad (1)$$

When using dedicated TAMs as the delivery channel, the wrapper scan chain inputs (WPI) and outputs (WPO) are connected directly to the ATE input and output channels through the dedicated TAM wires. The functional I/O connections (dotted lines in Fig. 4) are not used during testing. The wrapper instruction register is used to enable test mode (solid lines) or the normal functional mode (dotted lines).

In order to reuse the NoC as the delivery channel, the scan chains are connected to the existing functional connections. Therefore, the test control and synchronization are no longer at the hand of the ATE, rendering the IEEE 1500 wrapper inadequate. This is partly due to the inherent delay in packet-based data transfer used by the NoC. Sections 5.1–5.3 explain these problems and how they are addressed in the proposed NoC-compatible wrappers.

5.1 Type 1 NoC-Compatible Wrapper: Interfacing the PDI/PDO Ports to the Scan Chains

The proposed Type 1 wrapper is the same as the wrapper in [7] in terms of wrapper boundary cells and scan chain structure. However, their operations are slightly different when loading the test stimuli into the wrapper scan chains. As a result the wrapper controllers are slightly different. We will discuss the effect of this characteristic on the test application time at the end of this section. The Type 1 wrapper uses the same approach as in [1], [3] when forming the wrapper scan chains which minimizes $max\{s_i, s_o\}$, except that most of the PDI and PDO cells are excluded from the scan chain formation.

For a given number of wrapper scan chains, n_{sc}, and the PDI bit-width, n_{pdi}, the number of PDI bits that can be used to carry the test data for each wrapper scan chain, n_{idwc}, is given by Eq. (2), assuming that $n_{pdi} \geq n_{sc}$. To differentiate these PDI bits, those that can carry the test data are called *input data wrapper cells*, IDWC (shaded black in Fig. 5). If $\hat{n}_{idwc} \neq 0$ (Eq. (3)), some PDI bits cannot be used to carry the test data; these will become part of the wrapper scan chains, and not the IDWC. A similar analysis can be done for the *output data wrapper cells* (ODWC), resulting in Eqs. (4) and (5).

$$n_{idwc} = \lfloor n_{pdi}/n_{sc} \rfloor \tag{2}$$

$$\hat{n}_{idwc} = n_{pdi}\ mod\ n_{sc} \tag{3}$$

$$n_{odwc} = \lfloor n_{pdo}/n_{sc} \rfloor \tag{4}$$

$$\hat{n}_{odwc} = n_{pdo}\ mod\ n_{sc} \tag{5}$$

The Type 1 NoC-compatible wrapper is illustrated in Fig. 5 for the CUT with 8-bit PDI/PDOs, 2-bit PCI/PCOs, 1-bit PI', and three wrapper scan chains (refer to the notation in Fig. 3). From Eq. (2), $n_{idwc} = n_{odwc} = \lfloor 8/3 \rfloor = 2$ means that each wrapper scan chain is interfaced to two IDWC/ODWC cells. In addition, $\hat{n}_{idwc} = \hat{n}_{odwc} = (8\ mod\ 3) = 2$ means that the remaining two PDI/PDO bits cannot be used to carry the test data (illustrated by the dotted lines for `pdi[0]*` and `pdi[5]*`); these unused PDI/PDO bits become part of the wrapper scan chain, with no extra functionality. In the figure, dotted lines represent the functional paths which are not used during the scan operation. Solid lines represent the test data (stimuli and responses) transportation paths during the scan-in/out operations.

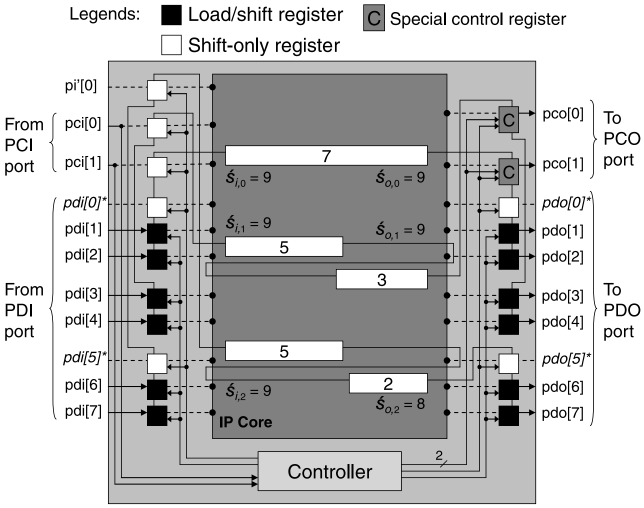


Fig. 5 Type 1 NoC-compatible wrapper architecture with scan chains made up of internal scan chains and normal (shift-only) wrapper cells in Fig. 6.

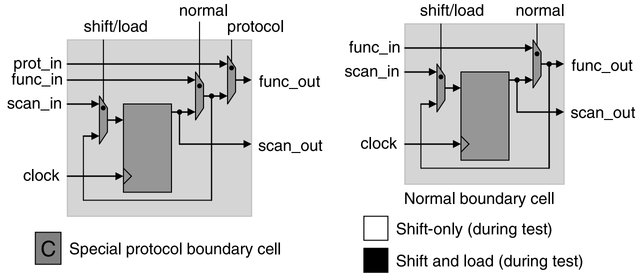


Fig. 6 Two types of wrapper cells used in [7]. The same normal wrapper cell is used under different control sequences for data-capturing from the NoC (black), and as part of the wrapper scan chains (white). The special wrapper cell has an extra *prot_in* input signal that bypasses the memory cell to supply the functional (i.e. bus protocol) control signals to return the test response data through the NoC.

The 2-bit input control signals (PCI) coming from the NoC are used by the controller to synchronize the load and shift control signals required in order to capture the test data from the PDI inputs into the corresponding IDWC cells and scan chain elements. Since the wrapper cells for PCI inputs are always in scan mode during the test application, the incoming signals are ignored by the CUT. Similarly, the control signals coming from the CUT (PCO) are ignored by the wrapper cells because the generated signals are invalid during the test operation. Instead, similar to the scheme proposed in [7], the controller must generate the necessary control signals (Fig. 2) and feed them to the NoC through the special wrapper cell at each PCO output, which is illustrated in Fig. 6. These functional control signals are necessary to ensure successful data transfer through the NoC in the functional mode.

Since n_{pdi} equals n_{pdo} for a typical NoC core, the following discussion on the PDI on the input port also applies to the PDO on the output port. During the test application, IDWC cells are loaded with the test data in one clock cycle, in the normal operation mode (refer to Fig. 5). The IDWC cells change into the test mode, during which the test data are serially shifted for two clock cycles to empty the contents into the scan chains. After completion, the IDWC cells change again into the normal mode to capture the next incoming data from the PDI port. This operation is controlled by a test controller which keeps track of the number of loads and shifts using counters [17].

For the NoC-compatible wrapper with a scan-in depth of nine (Fig. 5), after four repetitions of loads and shifts, the first eight bits of each scan chains are loaded with the test data. To load the last bit, the IDWC cells are loaded with new test data and a single shift clock is applied. However, before applying the capture cycle, the IDWC must also be loaded with valid test data. After the last single shift, only part of the IDWC cells contains valid test data. Reloading the IDWC data from the PDI port can corrupt the valid data currently in the IDWC cells. The wrapper control scheme in [6], [7] does not take into account this possible data corruption during the scan operation.

To overcome this problem, the first ($s_i \; mod \; n_{idwc}$) shift cycles of every test pattern must shift in dummy bits into the scan chains followed by the load-shift cycles until all scan chain elements are filled with test vector data. After the scan chains are completely loaded, another clock cycle is required to load the IDWC cells with valid test data before applying the capture cycle. Since the IDWC and ODWC wrapper cells are not considered part of the wrapper scan chains, the effective scan-in elements for the proposed wrapper scan chain design can be formally defined as follows.

Definition 1: The *scan-in (scan-out) elements for the Type 1 NoC-compatible wrapper* consist of the unused IDWC (ODWC) cells, bidirectional cells, and internal scan chains (i.e. excluding all the IDWC/ODWC cells). The maximum scan-in and scan-out depths are denoted by $\acute{s}_i$ and $\acute{s}_o$, respectively (Fig. 5). ■

As a result of the new test scheme, the number of shift-in and shift-out cycles required for the Type 1 NoC-compatible wrapper is summarized by Eqs. (6) and (7), respectively. Equation (8) gives the total TAT, where the additional "+1" represents the final load of the IDWC data prior to the capture cycle. For the NoC-compatible wrapper in Fig. 5, $T_{Type1} = 11n_v + 9$ clock cycles, which is smaller than T_{TAM} based on Eq. (1). The reduction in TAT is due to the IDWC and ODWC cells that are not part of the wrapper scan chains. The IDWC cells are loaded in parallel instead of through serial shifting.

$$\widehat{s_i} = \acute{s}_i + (\acute{s}_i \; mod \; n_{idwc}) \tag{6}$$

$$\widehat{s_o} = \acute{s}_o + (\acute{s}_o \; mod \; n_{odwc}) \tag{7}$$

$$T_{Type1} = (max\{\widehat{s_i}, \widehat{s_o}\} + 1 + 1) \times n_v + min\{\widehat{s_i}, \widehat{s_o}\} \tag{8}$$

5.2 Type 1 NoC-Compatible Wrapper: Inefficient NoC Bandwidth Utilization

For a CUT with n_{sc} wrapper scan chains and f_m scan frequency, its scan rate (or scan bandwidth) is given by $B^{scan}_{Type1} = n_{sc} \times f_m$. As shown in the previous example (Fig. 5), some PDI bits cannot be used to carry the test data due to the Type 1 wrapper's input architecture constraint. In order to supply the test data to the CUT at B^{scan}_{Type1} rate, the required channel bandwidth on the NoC is given in Eq. (9). For the NoC-compatible wrapper in Fig. 5, the scan and required bandwidths are $3f_m$ bits-per-second (bps) and $4f_m \; bps$, respectively.

$$B^{req}_{Type1} = B^{scan}_{Type1} \times \frac{n_{pdi}}{n_{pdi} - \hat{n}_{idwc}} \tag{9}$$

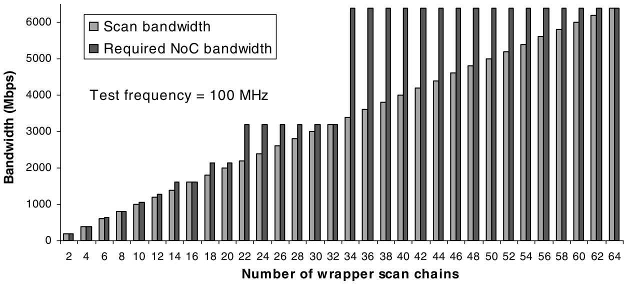


Fig. 7 Scan rate and required bandwidth of a Type 1 NoC-compatible wrapper for p93791's Core 6 [19] with $n_{pdi} = 64$.

Figure 7 shows the required bandwidth of the proposed Type 1 NoC-compatible wrapper (Fig. 5) compared to the actual scan bandwidth for an ITC'02 benchmark circuit for $n_{sc} = 2$ to 64 and $n_{pdi} = 64$. For some number of wrapper scan chains, the required bandwidth is almost twice that of the scan bandwidth. For these cases (i.e. $\hat{n}_{idwc} \neq 0$), the Type 1 NoC-compatible wrapper is inefficient in terms of NoC bandwidth utilization, similar to the NoC-compatible wrapper in [7]. For other cases, it is as efficient as the dedicated TAM-based wrapper while having the advantage of NoC reuse support capability with minimal area overhead. In the next section, an alternate wrapper architecture is proposed to overcome this limitation.

5.3 Type 2 NoC-Compatible Wrapper: Optimizing the NoC Bandwidth Utilization

Section 5.2 has shown that the Type 1 wrapper is inefficient in terms of bandwidth utilization because of the restricted input/output wrapper cells architecture. The Type 2 NoC-compatible wrapper in Fig. 8 is designed to complement the Type 1 wrapper in this aspect. Extra load/shift registers and shift-only registers are added to the PDI/PDO ports, similar to the buffer architecture in [17] for the reuse of the SoC's functional bus, and the bandwidth matching registers in [18]. On the input side, the load/shift registers translate the PDI bit-width into the number of wrapper scan chains using parallel-serial shift registers.

In this paper, we distinguish the terms *load, shift* and *scan* as follows. *Load* operation captures data into the wrapper boundary register (WBR) from its data input while shift and scan operation takes data from the shift input. Furthermore, *shift* operation takes place along the bandwidth-matching WBR chain consisting of the load/shift registers and the additional shift-only registers that are not part of the wrapper scan chains. *Scan* operation takes place along the wrapper scan chains as in Fig. 4.

Control signals on pci[0:1] indicate new data availability at the pdi[0:7] port, which triggers the Controller to assert a load signal to capture the data into the load/shift registers. Subsequently, the Controller asserts a shift signal on the load/shift registers and the 3-bit shift-only registers for $n_{sc} = 3$ cycles. This is followed by a scan signal on the wrapper scan chain (Fig. 9). This process is repeated until

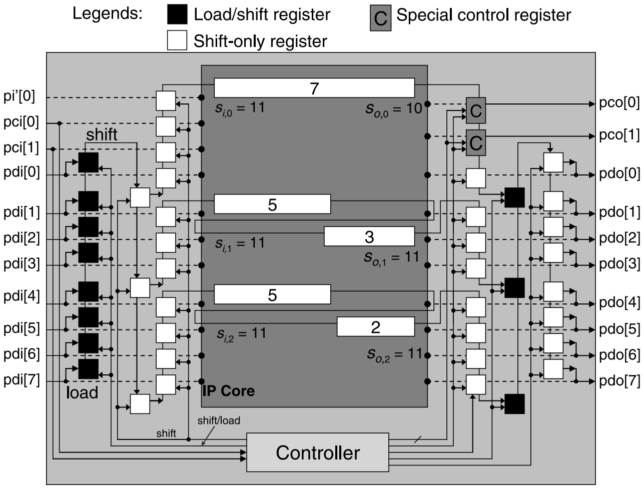
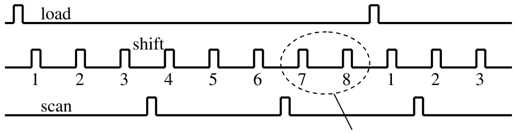


Fig. 8 Type 2 NoC-compatible wrapper with an I/O interface which performs parallel-serial shifting to match the NI bit width with the number of wrapper scan chains. The same wrapper cells in Fig. 6 are used.



Two bits are temporarily stored in the register while the next 8-bit data is loaded.

Fig. 9 Control signals sequence of the Type 2 wrapper to perform the bit width translation. Bits 7 and 8 from the first load are temporarily stored in the shift-only buffer while waiting for the first bit of the next load.

all the data in the pdi[0:7] register is shifted out. As explained in Fig. 9, bits 7 and 8 need to be scanned together with bit 1 of the next load cycle. The 3-bit shift-only register is necessary to store bits 7 and 8 while new data is loaded. Therefore, no NoC bandwidth is wasted. When the capture clock is asserted, the 3-bit shift-only registers contain the data for the first scan cycle of the next test pattern. Therefore, they are not considered part of the wrapper scan chains.

As a result, all the PDI wires can be used to carry the test data; therefore, the required NoC bandwidth matches the scan bandwidth for any wrapper configuration. The TAT for the Type 2 NoC-compatible wrapper is also the same as the dedicated TAM-based wrappers, given in Eq. (10). This is achieved at the cost of area overhead of load/shift registers and a more complex control scheme to realize the bit-width conversion. Therefore, it is important that the Type 2 wrapper is used only when necessary. Section 6 looks at two proposed optimization schemes for both of these NoC-compatible wrappers.

$$T_{Type2} = (max\{s_i, s_o\} + 1) \times n + min\{s_i, s_o\} \qquad (10)$$

6. Optimization of the NoC-Compatible Wrappers

Parallel core tests are performed according to a test schedule under given constraints. Figure 10 shows an example test scheduling scheme based on the bin-packing optimization [1], [3], where a rectangle represents the required NoC bandwidth (vertical axis) and the TAT (horizontal axis) of a CUT under a specific wrapper configuration. The figure illustrates the state of the test schedule after four cores are scheduled (i.e. the starting test times and the amount of allocated bandwidths are assigned). When scheduling the subsequent core, there are several possible starting times and amount of bandwidths that can be assigned to the core. B_1 and B_2 are the maximum amount of bandwidths that can be allocated if the test were to begin after the test of Core 2 and Core 3, respectively, complete. Using B_1 and B_2 as inputs to the wrapper optimization algorithm Ψ_B, we can determine the length of the test application by maximizing the bandwidth utilization. Based on these information, we can decide how to schedule the subsequent core test. Similarly, we could also consider the available test time instead of bandwidth during the test scheduling.

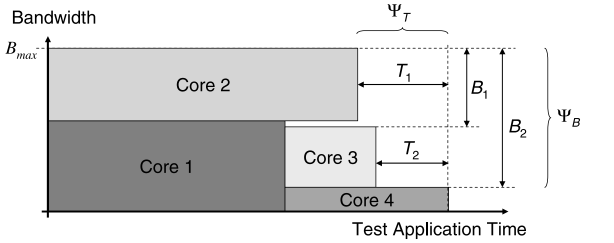


Fig. 10 A typical test schedule optimization scheme based on 2D-bin packing algorithm.

Based on the above scheduling objectives, the problems of optimizing the number of wrapper scan chains (n_{sc}) for a core, under a given bandwidth (Ψ_B) or a given test application time (Ψ_T), respectively, can be formally defined as follows.

Ψ_B: Given a core with i functional inputs, o functional outputs, b bidirectionals, k internal scan chains of length $l_1, l_2, \ldots, l_k$, scan frequency, f_m, and a maximum bandwidth for the virtual channel between the core and the ATE, B_{max}, find the number of wrapper scan chains, n_{sc}, such that (i) the TAT is minimized, (ii) the required bandwidth, $B_{req} \leq B_{max}$, and (iii) n_{sc} is minimum subject to priority (i).

Ψ_T: Given a core as in Ψ_B, and a maximum TAT, T_{max}, find the number of wrapper scan chains, n_{sc}, such that (i) the required bandwidth, B_{req}, is minimized, (ii) TAT $\leq T_{max}$, and (iii) n_{sc} is minimum subject to priority (i).

A similar problem for a dedicated TAM-based wrapper design has been proved NP-hard in [1]. Therefore, heuristic algorithms are proposed to solve both Ψ_B and Ψ_T. Figure 11 illustrates graphically the search steps for Ψ_B (when B_{max} = 5600 Mbps) for Core 17 of the p93791 [19] benchmark circuit. Since the TAT and the required bandwidth are monotonic decreasing and increasing with respect to n_{sc}, respectively, binary search algorithms can be used to find the

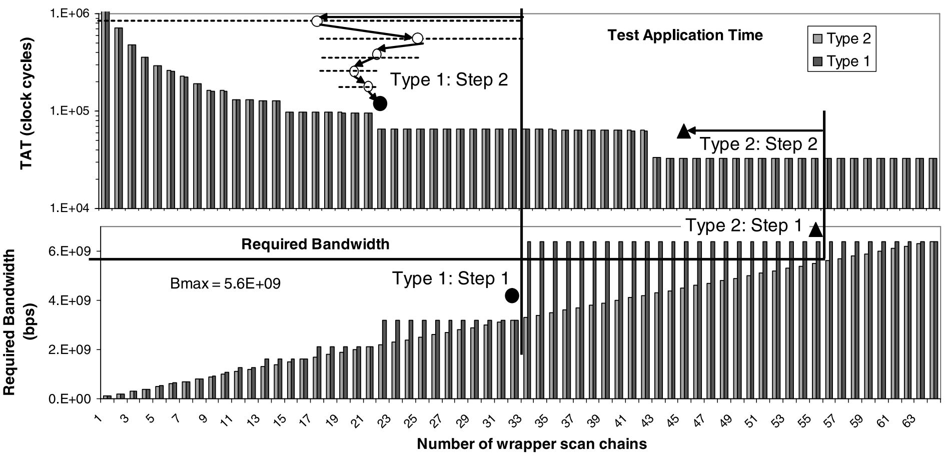


Fig. 11 Optimization of NoC-compatible wrapper design for a given B_{max}. In Step 2 (Type 1), the dotted lines represent the search space which halves in every progression of the binary search.

solution for n_{sc}. At each search step, wrapper scan chains which minimize $max\{s_i, s_o\}$ are formed using the algorithm proposed in [1], described in Sect. 5. For the Type 1 wrapper, binary search takes place in steps 1 and 2 (refer to Fig. 11). In Step 1, the maximum number of scan chains, n_{sc}^{max}, such that $B_{Type1}^{req} \leq B_{max}$ is located (objective (*ii*) of Ψ_B). In Step 2, the search is restricted to $n_{sc} = [1, n_{sc}^{max}]$ to find the solution(s) for n_{sc} that minimizes the TAT (objective (*i*) of Ψ_B). Because of the staircase decreasing TAT vs. n_{sc} (top half of Fig. 11), multiple solutions to n_{sc} may exist. The smallest value is chosen as the solution (objective (*iii*) of Ψ_B) without affecting objective (*i*). Progression of the binary search is graphically illustrated in Fig. 11. As a result, $n_{sc} = 22$ (Type 1) with a TAT of 65,098 clock cycles.

For the Type 2 wrapper, n_{sc}^{max} is directly calculated since B_{Type2}^{req} is a linear function of n_{sc}. Binary search in Step 2 (similar to the Type 1 wrapper) results in $n_{sc} = 45$ with a TAT of 32,766 clock cycles. Clearly a better result for the Type 2 wrapper when $B_{max} = 5600$ Mbps. In this case, the Type 1 wrapper is unable to utilize efficiently the allocated bandwidth because of the constraint in its I/O architecture. A similar heuristic is implemented for Ψ_T and some selected cases for both algorithms are presented in Sect. 7.

7. Experimental Results

In order to evaluate the effectiveness of the proposed methodology, we have conducted experiments on several benchmark IP cores. Core 17 and Core 6 (the largest of p93791 circuit) from the ITC'02 benchmark [19] are selected in order to offer comparisons with the IEEE 1500-based approaches reported in [1], [2]. Another IP core—an example core from [6]—allows some comparison with an NoC-compatible wrapper to be offered. Finally, we offer an extensive comparison with [7] using 42 different cores from ITC'02 circuits. The scan frequency is fixed to $f_m = 100$ MHz; the TAT reported in this paper is in number of scan clock cycles, where each cycle is equivalent to $1/f_m$ or $0.01\mu s$.

Table 1 Core 6 of p93791 [19] with 64-bit PDI/PDOs.

n_{sc}	TAT (clock cycles)		%
	[1, 2]	Type 1 NoC	increase
1	5,317,007	5,312,372	-0.09%
2	2,658,613	2,656,404	-0.08%
3	1,809,815	1,812,442	0.15%
4	1,358,456	1,359,988	0.11%
5	1,126,316	1,127,848	0.14%
6	907,097	909,286	0.24%
7	793,217	794,749	0.19%
8	679,337	680,212	0.13%
9	674,957	676,489	0.23%
10	565,457	566,770	0.23%
11	561,077	562,171	0.19%
12	455,738	455,956	0.05%
13	451,577	452,452	0.19%
14	451,358	451,576	0.05%
15	447,197	448,072	0.20%
16-19	341,858	342,076	0.06%
20-21	337,478	338,134	0.19%
22	333,317	333,754	0.13%
23	231,478	231,258	-0.10%
24-38	227,978	228,196	0.10%
39-42	223,598	223,816	0.10%
43-45	219,218	219,436	0.10%
46	115,848	115,847	0.00%
47-64	114,317	114,535	0.19%

A TAT comparison between the proposed Type 1 NoC-compatible wrapper and dedicated TAM-based IEEE 1500 wrapper is given in Table 1, for Core 6 with $n_{pdi} = 64$ bits. In all cases, the differences are always less than 0.2%; the proposed Type 1 NoC-compatible wrapper does not incur noticeable penalty on the TAT. In fact, some reductions are achieved for $n_{sc} = 1$ and 2 scan chains. For the Type 2 NoC-compatible wrapper, the TAT is the same as the dedicated TAM-based approach because the added interface between the CUT and the NoC port does not constrain the scan chain design. The Type 2 wrapper's required bandwidth matches the scan bandwidth—an improvement due to the extra load/shift registers. Table 2 reports similar experimental results for Core 17 of the same benchmark circuit. The TAT of the proposed NoC reuse wrapper is at most 0.66% larger than the standard wrapper.

For the circuit from [6], the TAT is given in Table 3. Compared to the dedicated TAM-based wrapper, the proposed Type 1 NoC-compatible wrapper is better for smaller number of wrapper scan chains. For wider scan chains, the TAT's are about 3% longer. However, compared to the NoC-compatible wrapper design in [6] [†], the Type 1 wrapper is always superior.

[†] Based on the corrected results obtained from the paper author because of reporting error in the original published literature.

Table 2 Core 17 of p93791 [19] with 64-bit PDI/PDOs.

n_{sc}	TAT (clock cycles)		%
	[1, 2]	Type 1 NoC	increase
1	1,433,858	1,430,832	-0.21%
2	717,148	715,648	-0.21%
3	483,258	484,342	0.22%
4	358,682	358,040	-0.18%
5	290,128	290,778	0.22%
6	257,361	257,577	0.08%
7	225,028	225,244	0.10%
8	192,912	193,128	0.11%
9	161,664	161,880	0.13%
10	160,579	161,229	0.40%
11	130,628	130,196	-0.33%
12	129,331	129,764	0.33%
13	128,680	128,896	0.17%
14	128,029	128,462	0.34%
15-16	97,215	97,648	0.45%
17	97,215	97,431	0.22%
18	96,998	97,214	0.22%
19	96,347	96,563	0.22%
20	95,913	96,129	0.23%
21	95,696	95,912	0.23%
22	65,530	65,314	-0.33%
23-34	64,882	65,098	0.33%
35	64,665	64,881	0.33%
36	64,448	64,664	0.34%
37-38	64,014	64,230	0.34%
39	63,797	64,013	0.34%
40	63,363	63,579	0.34%
41-42	63,146	63,362	0.34%
43	33,632	33,632	0.00%
44	32,982	32,982	0.00%
45-64	32,766	32,982	0.66%

Table 3 TAT comparison for the circuit defined in [6].

n_{sc}	1500	Amory	Proposed		% increase	
	[1, 2]	[6]	Type 1	Type 2	Type 1 / TAM	Type 1 / Amory
1	5,532	5,532	5,300	5,532	-4.19%	-4.19%
2	2,771	2,771	2,660	2,771	-4.01%	-4.01%
3	1,858	1,858	1,780	1,858	-4.20%	-4.20%
4	1,396	1,451	1,428	1,396	2.29%	-1.59%
5	1,363	1,429	1,406	1,363	3.15%	-1.61%
6	1,363	1,418	1,395	1,363	2.35%	-1.62%

Table 4 TAT comparison with [6] for Core 6 of p93791, with 64-bit PDI/PDO port.

Amory [6]			Proposed (Type 2)					
n_{sc}	TAT	B_{req}	B_{max}	n_{sc}	B_{req}	TAT	% increase	
							B_{req}	TAT
11	562,172	1,280	1,280	12	1,200	455,738	-6.3%	-18.9%
15	448,073	1,600	1,600	16	1,600	341,858	0.0%	-23.7%
22	333,755	3,200	3,200	24	2,400	227,978	-25.0%	-31.7%
24	228,416	3,200	3,200	24	2,400	227,978	-25.0%	-0.2%

Table 5 TAT comparison with [6] for Core 17 of p93791, with 64-bit PDI/PDO port.

Amory [6]			Proposed (Type 2)					
n_{sc}	TAT	B_{req}	B_{max}	n_{sc}	B_{req}	TAT	% increase	
							B_{req}	TAT
6	259,531	640	640	6	600	257,361	-6.3%	-0.8%
13	129,548	1,600	1,600	15	1,500	97,215	-6.3%	-25.0%
23	65,316	3,200	3,200	23	2,300	64,882	-28.1%	-0.7%
33	65,099	6,400	6,400	45	4,500	32,766	-29.7%	-49.7%

Table 4 and Table 5 give further comparisons for Core 6 and Core 17, respectively, of the p93791 benchmark circuit. The TAT (column 2) and the required bandwidth, B^{req}_{Amory}, (column 3) are obtained for selected n_{sc} (column 1). Using $B_{max} = B^{req}_{Amory}$ (column 4) as input to Ψ_B, the corresponding n_{sc}, B^{req}_{Type2}, and TAT for the proposed Type 2 wrapper are obtained. Using at most the bandwidth required by [6], the proposed wrapper gives shorter TATs.

In Table 4, for n_{sc} = 11 scan chains (first row), the proposed wrapper requires 6.3% less bandwidth to obtain 18.9% smaller TAT, than the given wrapper configuration by the method in [6]. For the selected cases in the tables, the proposed approach either requires less bandwidth to achieve comparable TAT, or achieves smaller TAT while requiring similar amount of bandwidth.

Table 6 Optimization results for selected values of B_{max} and T_{max} (Core 17 of p93791).

	Given:	Type 1			Type 2		
Ψ_B	B_{max} (Mbps)	n_{sc}	B_{req} (Mbps)	TAT	n_{sc}	B_{req} (Mbps)	TAT
	1,700	15	1,600	97,648	15	1,500	97,215
	3,000	21	2,133	96,129	23	2,300	64,882
Ψ_T	T_{max}	n_{sc}	B_{req} (Mbps)	TAT	n_{sc}	B_{req} (Mbps)	TAT
	70,000	22	3,200	65,098	22	2,200	65,530
	200,000	8	800	193,128	8	800	192,912

Table 7 List of considered ITC'02 benchmark cores.

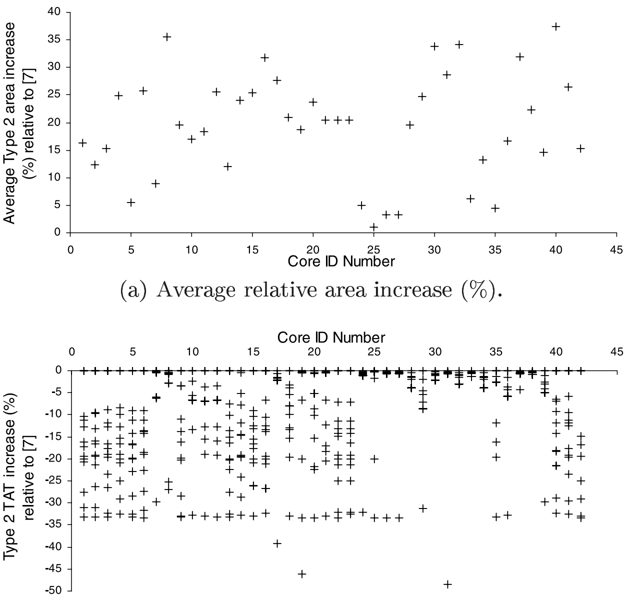
SoC	Cores considered	SoC	Cores considered
a586710	2, 3, 4, 7	p22810	27
d281	7	p34392	2, 10, 18
d695	2	p93791	10, 32
f2126	1, 2	q12710	1, 2, 3, 4
g1023	1, 2, 3, 4, 10, 11, 12, 14	t512505	1, 2, 4, 8, 9, 14, 15, 16, 17, 23, 24, 25, 26, 29, 31
h953	1		

Table 6 compares the Type 1 and Type 2 wrappers when Ψ_B and Ψ_T are applied. For B_{max} = 1700 Mbps, both wrappers result in similar performance—a slight advantage for Type 1 in terms of area overhead. At B_{max} = 3000 Mbps, Type 2 is clearly the winner, with only 0.8% bandwidth overhead to achieve 32.5% TAT reduction. For T_{max} = 70000, Type 2 requires 31% smaller bandwidth with less than 0.7% TAT overhead. On the other hand, at T_{max} = 200000, Type 1 wrapper is superior due to its minimal wrapper hardware overhead. The results illustrate the tradeoffs between the two types of NoC-compatible wrappers for a given constraint, which can be explored during the test schedule optimization.

An extensive comparison on area overhead and test application time between the proposed Type 2 wrapper and the wrapper in [7] is offered using 42 selected cores from the ITC'02 benchmark circuits shown in Table 7. Sixteen unique channel bandwidth values, $B_{max} \in [1 \times f_m, 2 \times f_m, \ldots, 16 \times f_m]$, in bits-per-second are considered. For every B_{max}, the wrapper configurations for both the Type 2 wrapper and the wrapper proposed in [7] are determined. The corresponding TAT and area costs in terms of wrapper boundary cells are given in Fig. 12. Figure 12 (a) shows the area increase of the Type 2 wrapper, relative to that of the wrapper in [7]. The horizontal axis is the core ID number in the order listed in Table 7. The average relative area increase for the 672 wrapper configurations is 19.3%. Figure 12 (b) gives the corresponding test time comparison, for the 16 different B_{max} values for each core. The proposed wrapper achieved up to 48.6% reduction and an average of 7.8% shorter test application time. For any given maximum channel bandwidth, B_{max}, Type 2's TAT is always shorter than that of [7].

8. Conclusion

We have proposed two versions of a NoC-compatible wrapper that requires minimal overhead on the test application time and area overhead. The previously proposed wrapper design did not handle the problem of inefficient bandwidth utilization. In this paper, we have proposed two heuristics that find the best wrapper design for a given maximum bandwidth or maximum test application time, which is important



(a) Average relative area increase (%).

(b) Relative TAT increase (%).

Fig. 12 Comparison between the Type 2 wrapper and the wrapper in [7]. The wrapper configurations are determined for 16 unique values of maximum bandwidth, $B_{max} \in [1 \times f_m, 2 \times f_m, \ldots, 16 \times f_m]$ bps and $n_{pdi} = n_{pdo} = 32$ for the 42 selected cores in Table 7.

for test schedule optimization.

The proposed wrapper does not incur large test time overhead (against the IEEE 1500 standard) for the same number of wrapper scan chains (about 3% for a very small circuit, and less than 0.25% for larger circuits). The wrappers scale well for large circuits. The advantage of the proposed wrapper is that NoC reuse is possible with only small test time overhead. With additional allowances on the area overhead, the proposed wrapper (Type 2) can efficiently utilize the NoC bandwidth with zero overhead on the test application time.

Compared to the NoC-compatible wrapper in [7], the enhanced Type 2 wrapper gives an average of 7.8% test time reduction for 42 selected SoC benchmark cores under various NoC bandwidth constraints.

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Fawnizu Azmadi Hussin is a Ph.D. student in the Computer Design & Test Laboratory at Nara Institute of Science and Technology. He obtained his Bachelor of Electrical Engineering from the University of Minnesota, U.S.A. and subsequently his M.Eng.Sc. in Systems and Control from the University of New South Wales, Australia. His research interest is in VLSI design and testing.

Tomokazu Yoneda received the B.E. degree in information systems engineering from Osaka University, Osaka, Japan, in 1998, and M.E. and Ph.D. degree in information science from Nara Institute of Science and Technology, Nara, Japan, in 2001 and 2002, respectively. Presently he is an assistant professor in Graduate School of Information Science, Nara Institute of Science and Technology. His research interests are VLSI CAD, design for testability, and SoC test scheduling. He is a senior member of the IEEE.

Hideo Fujiwara received the B.E., M.E., and Ph.D. degrees in electronic engineering from Osaka University, Osaka, Japan, in 1969, 1971, and 1974, respectively. He was with Osaka University from 1974 to 1985 and Meiji University from 1985 to 1993, and joined Nara Institute of Science and Technology in 1993. Presently he is a Professor at the Graduate School of Information Science, Nara Institute of Science and Technology, Nara, Japan. His research interests are logic design, digital systems design and test, VLSI CAD and fault tolerant computing, including high-level/logic synthesis for testability, test synthesis, design for testability, built-in self-test, test pattern generation, parallel processing, and computational complexity. He is the author of Logic Testing and Design for Testability (MIT Press, 1985). He received many awards including Okawa Prize for Publication, IEEE CS (Computer Society) Meritorious Service Awards, IEEE CS Continuing Service Award, and IEEE CS Outstanding Contribution Award. He served as an Editor and Associate Editors of several journals, including the IEEE Trans. on Computers, and Journal of Electronic Testing: Theory and Application, and several guest editors of special issues of IEICE Transactions of Information and Systems. Dr. Fujiwara is a fellow of the IEEE, a Golden Core member of the IEEE Computer Society, and a fellow of the IPSJ.