A Design of Programmable Logic Arrays with Universal Tests

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***Abstract*—In this paper the problem of fault detection in easily testable programmable logic arrays (PLA's) is discussed. The easily testable PLA's will be designed by adding extra logic. These augmented PLA's have the following features: 1) for a PLA with n inputs and m columns (product terms), there exists a "universal" test set such that the test patterns and responses do not depend on the function of the PLA, but depend only on the size of the PLA (the values n and m); 2) the number of tests is of order $n + m$. For the augmented PLA's, universal test sets to detect faults in PLA's are presented. The types of faults considered here are single and multiple stuck faults and crosspoint faults in PLA's. Fault location and repair of PLA's are also considered.**

***Index Terms*—Easily testable design, fault detection, fault location, logic circuits, programmable logic arrays (PLA's), universal test sets.**

I. INTRODUCTION

WITH the increasing circuit density in a single large-scale integrated (LSI) circuit chip, the difficulty of testing the circuits is becoming apparent. In order to overcome this problem, methods have been suggested in which test points and additional logic are used for the purpose of easing the test generation problem [1]-[6]. Designing easily testable circuits, one should pay attention to the following features: 1) the cost of generating test patterns is low, that is, the computation time for test generation is short; and 2) the cost of testing the circuits is low, that is, the length of test sequence is short.

This paper is concerned with the problem of fault detection and location in the easily testable programmable logic arrays (PLA's) which have the above mentioned features. The PLA, which is conceptually a two-level AND-OR, is attractive in LSI due to its memory-like array structure. A method is presented to augment PLA's by adding extra logic so that the augmented PLA's have the following easily testable features: 1) for a PLA with n inputs and m columns (product terms), there exists a "universal" test set such that the test patterns and responses do not depend on the function of the PLA, but depend only on the size of the PLA (the values n and m); 2) the number of tests is of order $n + m$. Since the augmented PLA's have the universal test set, the test generation of PLA's is no more necessary, and the cost of test generation is considerably reduced to almost zero. The augmented PLA's introduced in this paper are similar to the PLA which was independently obtained by Hong and Ostapko [3]. However, since the augmented PLA's considered in this paper need less additional hardware than [3] and also since no test sequence for multiple faults appears in [3], we will present universal test sequence for single and multiple faults in the PLA's. First, single-stuck faults and single crosspoint faults are considered, and the universal test sets to detect these faults in PLA's are presented. Then the type of faults are extended to multiple faults. Fault location and repair of PLA's are also considered where the faults are assumed to be multiple crosspoint faults.

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II. PROGRAMMABLE LOGIC ARRAYS

A programmable logic array (PLA) consists of three main parts. These are the decoders, the AND, and the OR arrays. The decoders are usually implemented by single-bit decoders or double-bit decoders, as shown in Figs. 1 and 2. Both the AND array and the OR array are used to implement multioutput combinational logic with sum-of-products forms. Fig. 3 shows an example of a 4-input, 2-output PLA with single-bit decoders, which realizes two functions in the following:

$$f_1 = x_1 \vee x_4 \vee \bar{x}_2\bar{x}_3 \vee \bar{x}_1x_2x_3$$

$$f_2 = \bar{x}_2 \vee x_4 \vee x_1\bar{x}_3 \vee \bar{x}_1x_2x_3.$$

Fig. 4 shows another realization using a PLA with double-bit decoders.

In the following Sections III and IV, we present a method to augment PLA's with single-bit decoders or double-bit decoders by adding extra logic so that the augmented PLA's are easily testable PLA's with short "universal" test sequences. The types of faults considered in Sections III and IV are single faults in the PLA which are the stuck faults and the crosspoint faults. A crosspoint fault in a PLA is a fault such that the presence (absence) of a contact between a row and column of the PLA becomes the absence (presence) of the contact.

III. AUGMENTED PLA'S WITH SINGLE-BIT DECODERS

In order to design an easily testable PLA with single-bit decoders, we augment a given PLA by adding extra logic, that is, a shift register, two cascades of EOR's (EXCLUSIVE-OR's), and one column and one row to AND and OR arrays, respectively, as shown in Fig. 5. The connections of the added column in the AND array is arranged so that each row of the AND array has an odd number of connections. Similarly, the connections of the added row in the OR array is arranged so that each column has an odd number of connections. In the augmented

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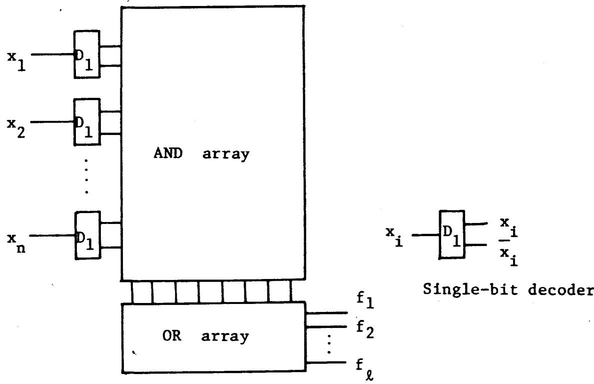

Fig. 1. PLA with single-bit decoders.

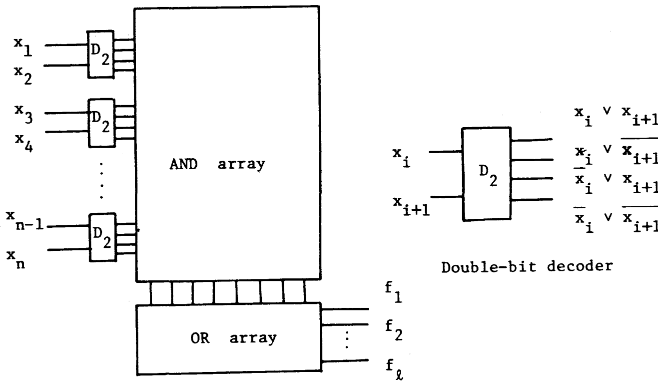

Fig. 2. PLA with double-bit decoders.

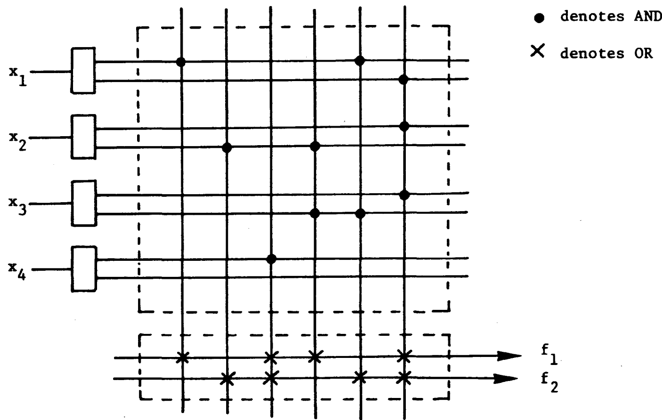

Fig. 3. Example of PLA with single-bit decoders.

PLA each column (product term) b_i is ANDed by each variable S_i of the shift register as follows:

$$b_i = p_i \cdot S_i \qquad \text{for } i = 1, 2, \cdots, m$$

where p_i is a product term generated by the ith column of the AND array without the shift register and m is the number of columns. Fig. 5 shows a PLA augmented from the PLA shown in Fig. 3.

The augmented PLA has the following properties.

1) The shift register can be used to select an arbitrary column of the AND array by setting 1 to the selected column and 0 to all other columns. [See Fig. 6(a).]

2) The augmented decoders with control inputs y_1 and y_2 can be used to sensitize an arbitrary row of the AND array by setting 0 or 1 to the selected row and 1 to all other rows. [See Fig. 6(b).]

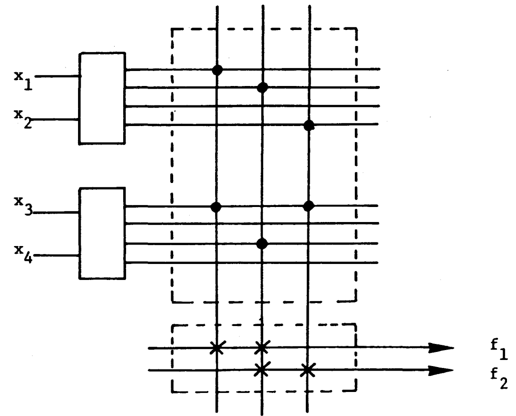

Fig. 4. Example of PLA with double-bit decoders.

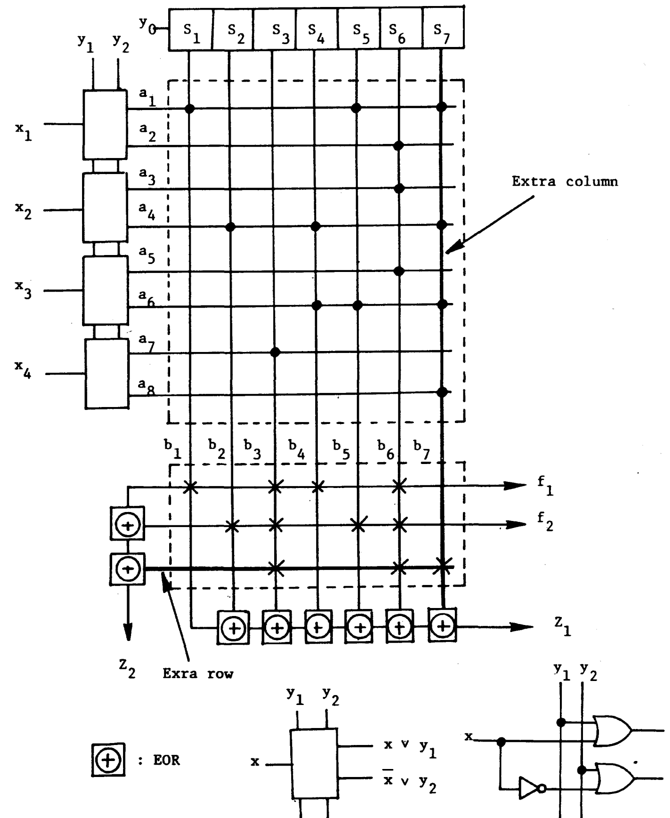

Fig. 5. Augmented PLA with single-bit decoders.

3) The cascade of EOR's below the OR array can be used as a parity checker to detect single errors in the sensitized row of the AND array. [See Fig. 6(c).]

4) The cascade of EOR's on the left of the OR array can be used as a parity checker to detect single errors in the sensitized column of the OR array. [See Fig. 6(d).]

Utilizing the above properties of the augmented PLA we can present a universal test set to detect single faults in the following:

1) stuck faults on the input or output lines of gates within the decoders, the AND array, and the OR array,

2) crosspoint faults in the AND and OR arrays.

Table I shows the test set $A_{n,m}$ to detect the above types of faults, where n is the number of inputs, m is the number of columns in the AND array, and

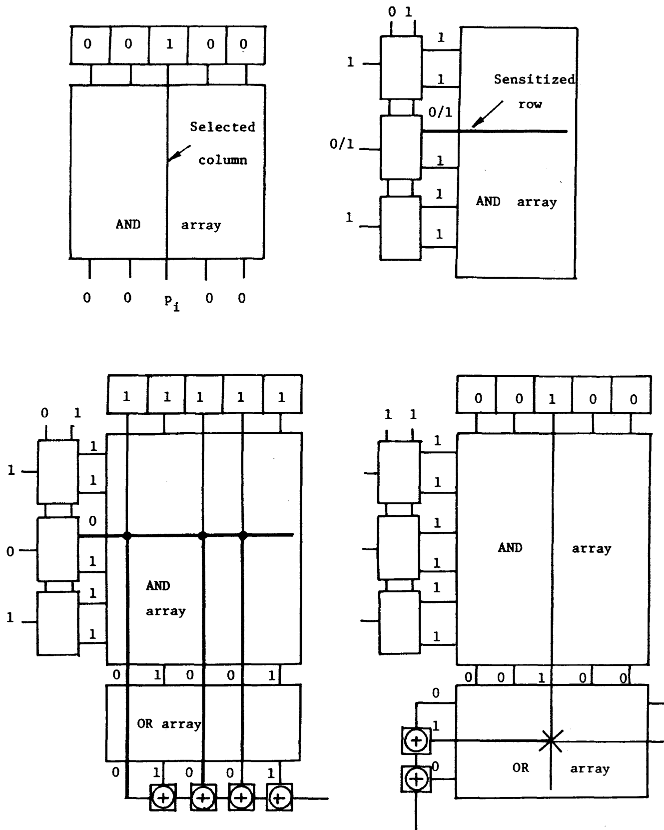

Fig. 6. Features of the augmented PLA.

TABLE I
UNIVERSAL TEST SET $A_{n,m}$

	x_1 ...... x_i ...... x_n y_1 y_2 S_1 .... S_j ..... S_m	Z_1 Z_2
I_1	- .... - ...... - - - 0 .... 0 0	0 0
For j=1,2,...,m		
I_{2j}^0	0 .... 0 ...... 0 1 0 0 ...0 1 0 0	1 1
I_{2j}^1	1 .... 1 ...... 1 0 1 0 ... 0 1 0 0	1 1
For i=1,2,...,n		
I_{3i}^0	1 ..... 1 0 1 ..... 1 0 1 1 ..... 1 1	ε_m -
I_{3i}^1	0 ..... 0 1 0 ..... 0 1 0 1 ..... 1 1	ε_m -

$$\epsilon_m = \begin{cases} 0 & \text{if } m \text{ is odd} \\ 1 & \text{if } m \text{ is even} \end{cases}$$

and " – " represents DON'T CARE.

For this test set $A_{n,m}$ we have the following theorem.

Theorem 1: Let $M_{n,m}$ be an augmented PLA with single-bit decoders which has n inputs and m columns in the AND array. For any $M_{n,m}$ the test set $A_{n,m}$ can detect all single stuck and crosspoint faults in the decoders, and AND array and the OR array.

Proof: When we apply test inputs I_{2j}^0 and I_{2j}^1, the jth column is set to 1 and other columns are all set to 0. Therefore, both I_{2j}^0 and I_{2j}^1 can detect any crosspoint fault on the jth column of the OR array by observing the output Z_2, and a stuck-at-0 fault on the jth column, stuck-at-1 faults on the other columns, and stuck-at-0 faults on the rows of the AND array by observing the output Z_1. Any stuck fault on the row of the OR array can be detected by some I_{2j}^0 and I_{2j}^1 $(1 \leq j \leq m)$.

By applying test I_{3i}^0 (I_{3i}^1), the $(2i-1)$th $(2i$th$)$ row of the AND array is set to 0 and other rows are all set to 1. Therefore, test I_{3i}^0 (I_{3i}^1) can detect all crosspoint faults and a stuck-at-1 fault on the $2i$-1th ($2i$th) row in the AND array by observing the output Z_1.

Tests I_{2j}^0, I_{2j}^1 $(j = 1, 2, \cdots, m)$ and I_{3i}^0, I_{3i}^1 $(i = 1, 2, \cdots, n)$ can also detect all stuck faults in the decoders. The stuck-at-0 faults on the input lines of OR gates can be detected by I_{2j}^0 and $I_{2j}^1 (j = 1, 2, \cdots, m)$. The stuck-at-1 faults on the input lines of OR gates can be detected by I_{3i}^0 and I_{3i}^1 $(i = 1, 2, \cdots, n)$. The stuck-at-0 faults on the input lines x_i $(i = 1, 2, \cdots, n)$, y_1, and y_2 can be detected by I_{2j}^0 and I_{2j}^1 $(j = 1, 2, \cdots, m)$. The stuck-at-1 faults on the input lines x_i $(i = 1, 2, \cdots, n)$, y_1, and y_2 can be detected by I_{3i}^0 and $I_{3i}^1 (i = 1, 2, \cdots, n)$. Q.E.D.

Next, we will show that the test set $A_{n,m}$ can also detect any multiple stuck fault in the EXCLUSIVE-OR cascades under the fault assumption that permits only stuck-type faults on the external input and output lines of EOR gates, that is, no fault within EOR gates is considered.

We have the following lemma. Similar results appear in [12].

Lemma 1: For an EXCLUSIVE-OR cascade realization of a k-input linear function, all multiple stuck faults on the external lines of EOR gates can be detected by the following $k + 1$ tests:

$$t_0 = (0, 0, \cdots, 0)$$
$$t_1 = (1, 0, \cdots, 0)$$
$$t_2 = (0, 1, 0, \cdots, 0)$$
$$\ddots$$
$$t_k = (0, 0, \cdots, 0, 1).$$

Proof: Any linear function of k or fewer variables can be expressed in the form

$$l_A(x_1, x_2, \cdots, x_k) = a_0 \oplus a_1x_1 \oplus a_2x_2 \oplus \cdots \oplus a_kx_k$$

where $a_i = 0$ or 1 for $i = 1, 2, \cdots, k$ and $A = (a_0, a_1, a_2, \cdots, a_k)$.

It can easily be shown that even if one or more stuck-at-0 or stuck-at-1 faults are introduced into the EXCLUSIVE-OR cascade, the resulting circuit still realizes a linear function. So, any faulty function of the EXCLUSIVE-OR cascade can be expressed in the above form. When $A = (0, 1, \cdots, 1)$, the linear function l_A represents the fault-free linear function l_k.

Let $l_B = b_0 \oplus b_1x_1 \oplus \cdots \oplus b_kx_k$ be a linear function realized by a circuit under test where $b_i = 0$ or 1 for $i = 1, 2, \cdots, k$. Applying the vectors $t_0, t_1, \cdots, t_k$ to the equation

$$l_A(x_1, x_2, \cdots, x_k) = l_B(x_1, x_2, \cdots, x_k)$$

we obtain

$$a_0 = b_0$$
$$a_0 \oplus a_1 = b_0 \oplus b_1$$
$$\vdots$$
$$a_0 \oplus a_k = b_0 \oplus b_k$$

which implies

$$a_i = b_i \qquad \text{for } i = 0, 1, 2, \cdots, k.$$

Therefore, we can uniquely determine the values a_i's, and thus distinguish whether l_B equals to the fault-free linear function or not. Q.E.D.

In Lemma 1 $k + 1$ tests $t_0, t_1, \cdots, t_k$ can easily be extended to k linearly independent vectors plus zero vector. Then we have the following lemma.

Lemma 2: If k input vectors are linearly independent, then these k vectors plus zero vector are sufficient to detect any multiple stuck fault on the external lines of EOR gates in a k-input EXCLUSIVE-OR cascade.

Let $M_{n,m}$ be an augmented PLA, and let C_1 and C_2 be the cascades of EOR's having the output Z_1 and Z_2, respectively, in the augmented PLA shown in Fig. 5. Let $M_{\text{OR}} = [a_{ij}]$ be a matrix of l rows and m columns where

$$a_{ij} = \begin{cases} 1 & \text{if there exists a link at the } (i,j)\text{th position of the OR array, and} \\ 0 & \text{otherwise.} \end{cases}$$

By Lemmas 1 and 2 we have the following theorem for the multiple faults in two cascades of EOR's, C_1 and C_2.

Theorem 2: The tests I_1, I_{2j}^0 ($j = 1, 2, \cdots, m$) in $A_{n,m}$ are sufficient to detect all multiple stuck faults in C_1. If the column rank of matrix M_{OR} is equal to the number of inputs of the EXCLUSIVE-OR cascade C_2, then all the multiple stuck faults in C_2 can be detected by tests I_1, and I_{2j}^0 ($j = 1, 2, \cdots, m$) in $A_{n,m}$.

Note that if the column rank of matrix M_{OR} is not equal to the number of inputs of the cascade C_2 although it hardly occurs, then it is not guaranteed that all multiple stuck faults in the cascade C_2 can be detected by the tests mentioned above. To overcome this problem, it might be necessary to add extra OR array so that the rank of M_{OR} is equal to the number of inputs of the EXCLUSIVE-OR cascade C_2. Note also that we permit only stuck-type faults on the external input and output lines of EOR gates. However, by adding extra array it is possible to generate all test patterns for the cascade C_1 and C_2. This technique was reported by Hong and Ostapko [3].

Using the test set $A_{n,m}$, we can construct a test sequence for the augmented PLA's as follows:

$$\alpha_{n,m} = I_1 I_{21}^0 I_{22}^0 \cdots I_{2m}^0 I_{21}^1 I_{22}^1 \cdots I_{2m}^1 \\ U_1 U_2 \cdots U_{m-1} I_{31}^0 I_{32}^0 \cdots I_{3n}^0 I_{31}^1 I_{32}^1 \cdots I_{3n}^1$$

where the test pattern U_i ($i = 1, 2, \cdots, m - 1$) is defined as

$$\begin{matrix} x_1 \cdots x_n y_1 y_2 S_1 S_2 \cdots S_i S_{i+1} \cdots S_m Z_1 Z_2 \\ U_i = - \cdots - 1\,1\,1\,1 \cdots 1\,0 \cdots 0\,\bar{\epsilon}_i. \end{matrix}$$

The test sequence $\alpha_{\text{n,m}}$ can also detect the shift function of the shift register, as well as all single stuck and crosspoint faults in the PLA. The length of the test sequence is $2n + 3m$.

Now we have presented the test set and the test sequence for the augmented PLA's. Both the test set $A_{n,m}$ and the test sequence $\alpha_{n,m}$ have the following advantages of easy testability. The test set $A_{n,m}$ does not depend on the connection pattern of the PLA, but depends only on the values n and m, that is, the test patterns and responses are uniquely determined only by the size of the PLA. Therefore, the test set $A_{n,m}$ is "universal." We can also see that the test sequence $\alpha_{n,m}$ is universal. Hence, the test generation of the augmented PLA's is not more necessary. Moreover, the universal test sequence is a very short test sequence whose length is $2n + 3m$. In this way we can see that the augmented PLA's are very easily testable PLA's having a universal test sequence.

IV. Augmented PLA's with Double-Bit Decoders

The PLA's with double-bit decoders can be similarly augmented by adding extra logic, that is, a shift register, two cascades of EOR's, and one column and one row to the AND and OR arrays, respectively, as shown in Fig. 7. Fig. 7 shows a PLA augmented from the PLA shown in Fig. 4. The augmented double-bit decoders have four control inputs y_1, y_2, y_3, and y_4, as shown in Fig. 7.

For the augmented PLA with double-bit decoders, we can similarly construct a universal test set $B_{n,m}$, as shown in Table II, and the following theorem holds.

Theorem 3: Let $N_{n,m}$ be an augmented PLA with double-bit decoders which has n inputs and m columns in the AND array. For any $N_{n,m}$, the test set $B_{n,m}$ can detect all single stuck and crosspoint faults in the decoders, the AND array, and the OR array.

Theorem 4: $B_{n,m}$ can detect all multiple stuck faults in the cascade C_1. If the column rank of M_{OR} is equal to the number of rows in the OR array, then all multiple stuck faults in the cascade C_2 can also be detected by $B_{n,m}$.

Using the test set $B_{n,m}$, we can construct the universal test sequence $\beta_{\text{n,m}}$ for the augmented PLA's as follows:

$$\beta_{n,m} = I_1 I_{21}^0 I_{22}^0 \cdots I_{2m}^0 I_{21}^1 I_{22}^1 \cdots I_{2m}^1 I_{21}^2 I_{22}^2 \cdots I_{2m}^2 \\ I_{21}^3 I_{22}^3 \cdots I_{2m}^3 U_1 U_2 \cdots U_{m-1} I_{31}^0 I_{32}^0 \cdots I_{3\frac{n}{2}}^0 \\ I_{31}^1 I_{32}^1 \cdots I_{3\frac{n}{2}}^1 I_{31}^2 I_{32}^2 \cdots I_{3\frac{n}{2}}^2 I_{31}^3 I_{32}^3 \cdots I_{3\frac{n}{2}}^3$$

where the test pattern U_i ($i = 1, 2, \cdots, m - 1$) is defined as

$$\begin{matrix} x_1 \cdots x_n y_1 y_2 y_3 y_4 S_1 \cdots S_i S_{i+1} \cdots S_m \quad Z_1 Z_2 \\ U_i = - \cdots - 1\,1\,1\,1\,1 \cdots 1\,0 \cdots 0 \quad \bar{\epsilon}_i\, -. \end{matrix}$$

The length of the test sequence is $2n + 5m$.

Note that we also state more general results for PLA with k-bit decoders. The universal test sequence might be constructed as follows:

$$I_1 I_{21}^0 \cdots I_{2m}^0 I_{21}^1 \cdots I_{2m}^1 \cdots I_{21}^{2k-1} \cdots I_{2m}^{2k-1} \\ U_1 U_2 \cdots U_{m-1} I_{31}^0 \cdots I_{3n/k}^0 I_{31}^1 \cdots I_{3nk}^1 \cdots I_{31}^{2k-1} \\ \cdots I_{3n/k}^{2k-1}$$

where I_{2j}^i's and I_{3j}^i's are the test patterns for k-bit decoders extended from 2-bit decoders. The total test length is $(2^k + 1)m + (n/k)2^k$.

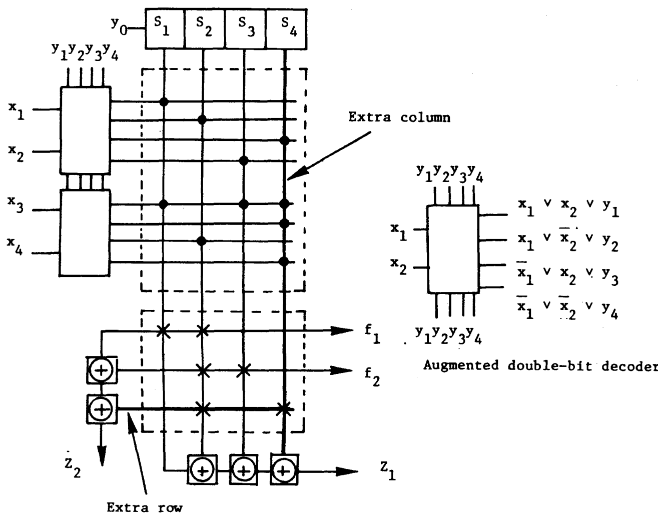

Fig. 7. Augmented PLA with double-bit decoders.

TABLE II
UNIVERSAL TEST SET $B_{n,m}$

	x_1	x_2	...	x_{2i-1}	x_{2i}	...	x_{n-1}	x_n	y_1	y_2	y_3	y_4	S_1	...	S_j	...	S_m	Z_1	Z_2
I_1	-	-	...	-	-	...	-	-	-	-	-	-	0	...	0	....	0	0	0
For j=1,2,...,m																			
I_{2j}^0	0	0	....	0	0	......	0	0	1	0	0	0	0	....	1	....	0	1	1
I_{2j}^1	0	1	....	0	1	......	0	1	0	1	0	0	0	....	1	....	0	1	1
I_{2j}^2	1	0	....	1	0	......	1	0	0	0	1	0	0	....	1	....	0	1	1
I_{2j}^3	1	1	....	1	1	......	1	1	0	0	0	1	0	....	1	....	0	1	1
For $i=1,2,\ldots,\frac{n}{2}$																			
I_{3i}^0	1	1	....	0	0	......	1	1	0	1	1	1	1	....	1	....	1	ε_m	-
I_{3i}^1	1	0	....	0	1	......	1	0	1	0	1	1	1	....	1	....	1	ε_m	-
I_{3i}^2	0	1	....	1	0	......	0	1	1	1	0	1	1	....	1	....	1	ε_m	-
I_{3i}^3	0	0	....	1	1	......	0	0	1	1	1	0	1	....	1	....	1	ε_m	-

V. MULTIPLE FAULT DETECTION

So far we have discussed the single fault detection problem for the augmented PLA's. In this section we extend the single fault model to the types of multiple faults in the following, and present the universal test set for them. Note that no more than one of the following multiple faults occurs simultaneously.

1) Multiple stuck faults on the primary outputs x_i ($i = 1, 2, \cdots, n$).

2) Multiple stuck faults on the control inputs y_i ($i = 1, 2, 3, 4$).

3) Multiple stuck faults on the rows in the AND array.

4) Multiple stuck faults on the columns in the AND and OR arrays.

5) Multiple stuck faults on the rows in the OR array.

6) Multiple stuck faults on the input and output lines of the EOR cascade C_1.

7) Multiple stuck faults on the input and output lines of the EOR cascade C_2 provided that the column rank of M_{OR} is equal to the number of rows in OR array.

8) Odd number of crosspoint faults on the columns of the OR array.

9) Odd number of crosspoint faults on the rows of the AND array.

For the class of the above mentioned multiple faults, we can show that the test sets $A_{n,m}$ and $B_{n,m}$ are also universal test sets for the augmented PLA's with single-bit decoders and double-bit decoders, respectively.

Now, the cascade of EOR's in the PLA is used as a parity checker to detect odd number of errors on the rows and columns of the AND and OR arrays, respectively. In the same way this approach can be extended to other multiple fault model by applying error detecting codes such as linear codes [10], where the augmented PLA's will be designed to have more than two cascades of EOR's.

VI. FAULT LOCATION AND REPAIR

In this section we consider the fault detection and repair of the augmented PLA's. For the augmented PLA's there exists a universal test sequence of fault location. The types of faults considered here are the multiple crosspoint faults in the AND and/or OR arrays.

Fault location test can be performed by identifying the configuration of the AND and OR arrays, that is, whether there exists a link between each row i and column j of the arrays. By applying the test pattern shown in Fig. 8, we can identify whether there exists a link or contact between row i and column j and the AND array. If the value of output Z_1 is 0 (1), then there exists a link (correspondingly, no link) at the (i,j)th position of the AND array.

For the OR array, the test pattern shown in Fig. 9 can detect the presence or absence of a link between row i and column j of the OR array. If the value of output f_i is 1(0), then there exists a link (no link) at the (i,j)th position of the OR array. Note that the last row of the OR array does not have a direct output, however it is observable from the additional output Z_2.

Using these test patterns, we can completely determine the configuration of the AND and OR arrays. Therefore, all the multiple crosspoint faults can be found by observing the responses. The number of tests for the AND array is $2nm$, and the number of tests for the OR array is m. Hence, the total length of the fault location test sequence for the augmented PLA's is $2nm + m$.

Now after the fault location test the faulty PLA can be repaired as follows. For a field programmable logic array (FPLA), it is known that an arbitrary product term can be both logically and physically deleted and a new product term can be generated by using spare columns of the PLA, and thus the faulty PLA can be repaired using spare rows and/or columns [11]. If the PLA is a mask programmable logic array (MPLA), it is difficult to repair the PLA for itself. In this case we can repair the faulty PLA by using the well-known memory

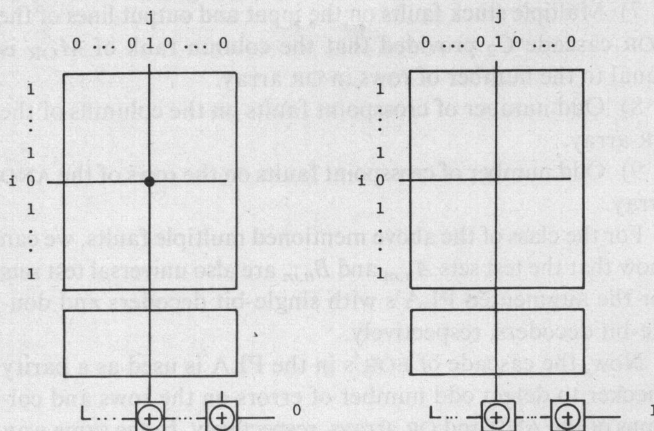
Fig. 8. Fault location test for AND array.

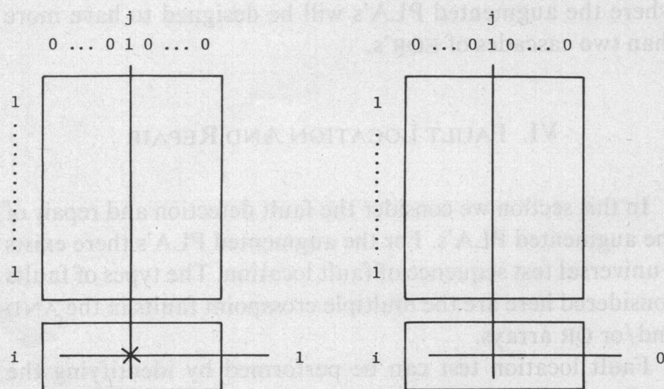
Fig. 9. Fault location test for OR array.

patch technique. This is a method to recover the function of the faulty MPLA by switching it to a spare FPLA when some errors occur.

VII. Conclusion

In this paper we have introduced a design of easily testable PLA's by adding extra logic and presented universal test sequences for them. These augmented PLA's have the very short universal test sequences such that the test patterns and responses are uniquely determined only by the size of the PLA's independently of the function of them. The length of the universal test sequences to detect single and multiple faults is of order $n + m$, and the length of the universal test sequences to locate multiple faults is of order nm, where n is the number of inputs and m is the number of columns of the AND array.

The augmented PLA in this paper, however, has a weak point such that there exist some stuck faults inside of EXCLUSIVE-OR gates which cannot be detected by the universal tests. This problem can be resolved by adding extra OR array such as Hong and Ostapko [3] to generate the test patterns for such faults.

Although we have not considered PLA's with flip-flops in this paper, we can augment them to have the universal test sets. This can be done by applying a scan-in and scan-out technique such as LSSD [5], [6].

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References

[1] R. G. Bennetts and R. V. Scott, "Recent developments in the theory and practice of testable logic design," *Computer*, pp. 47–63, June 1976.

[2] S. M. Reddy, "Easily testable realizations for logic functions," *IEEE Trans. Comput.*, vol. C-21, pp. 1183–1188, Nov. 1974.

[3] S. J. Hong and D. L. Ostapko, "FITPLA: A programmable logic array for function independent testing," in *Dig. 10th Int. Symp. Fault-Tolerant Comput.*, Kyoto, Japan, June 1980, pp. 131–136.

[4] H. Fujiwara, K. Kinoshita, and H. Ozaki, "Universal test sets for programmable logic arrays," in *Dig. 10th Int. Symp. Fault-Tolerant Comput.*, Kyoto, Japan, June 1980, pp. 137–142.

[5] M. J. Williams and J. B. Angell, "Enhancing testability of large-scale integrated circuits via test points and additional logic," *IEEE Trans. Comput.*, vol. C-22, pp. 46–60, Jan. 1973.

[6] E.B. Eichelberger and T. W. Williams, "A logic design structure for LSI testability," in *Proc. 14th Des. Automat. Conf.*, June 1977, pp. 462–468.

[7] H. Fleisher and L. I. Maissel, "An introduction to array logic," *IBM J. Res. Develop.*, vol. 19, pp. 98–109, Mar. 1975.

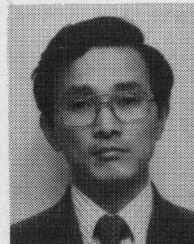
[8] D. L. Ostapko and S. J. Hong, "Fault analysis and test generation for programmable logic arrays (PLA's)," in *Dig. 8th Int. Symp. Fault-Tolerant Comput.*, Toulouse, France, June 1978, pp. 83–89.

[9] V. K. Agarwal, "Multiple fault detection in programmable logic arrays," in *Dig. 9th Int. Symp. Fault-Tolerant Comput.*, Madison, WI, June 1979, pp. 227–234.

[10] W. W. Peterson and E. J. Weldon, Jr., *Error-Correcting Codes*. Cambridge, MA: MIT Press, 1972.

[11] *Signetics Field Programmable Logic Arrays*, Signetics, CA, Oct. 1977.

[12] K. K. Saluja and S. M. Reddy, "Fault detecting test sets for Reed-Muller canonic networks," *IEEE Trans. Comput.*, vol. C-24, pp. 995–998, Oct. 1975.



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