A New PLA Design for Universal Testability

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Abstract — **A new design of universally testable PLA's is presented in which all multiple faults can be detected by a universal test set which is independent of the function being realized by the PLA. The proposed design has the following properties. 1) It can be tested with function-independent test patterns; hence, no test pattern generation is required. 2) The amount of extra hardware is significantly decreased compared to the previous designs of universally testable PLA's. 3) Very high fault coverage is achieved, i.e., all single and multiple stuck faults, crosspoint faults, and adjacent line bridging faults are detected. 4) It is appropriate for built-in testing approaches. 5) It can be applied to the high-density PLA's using array folding techniques.**

Index Terms — **Built-in test, design for testability, fault detection, function-independent test, PLA folding, programmable logic array (PLA), testing, universal test.**

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I. Introduction

Because of the rapidly increasing circuit density in LSI/VLSI technology, the testing problem is getting much more difficult and worse. One approach to alleviate this problem is embodied in design for testability techniques [1]. With these techniques, sufficient extra circuitry is added to a circuit or chip so as to reduce the complexity of testing or the cost of testing. The complexity or cost of testing can be classified into two categories: one is the ease of test generation and the other is the ease of test application. For the first category, the optimum design to minimize the test generation cost is achieved by eliminating the expensive stage of test generation. Such a design can be accomplished by universal testing or function-independent testing such that test patterns are predetermined independently of the function being realized. Various designs for universal testability have been reported successfully for the circuits with regular structures such as Reed–Muller canonic circuits [2], [3] and programmable logic arrays (PLA's) [4]–[7]. The PLA, which is conceptually a two-level AND–OR, is especially attractive in LSI/VLSI due to its memory-like array structure, and has become a popular and effective tool for implementing logic functions [12]–[16].

The first contributions to the design of universally testable PLA's are Fujiwara *et al.* [4], [5] and Hong and Ostapko [6]. They have independently proposed designs of PLA's which can be tested easily by function-independent test patterns. Although the designs of Fujiwara [4], [5] and Hong [6] differ in implementation, the essential idea is almost the same. They both have extra circuitry to select one row line of AND array, a shift register to select one product line, and two EXCLUSIVE OR cascades or trees to check the parity of the row and column in the array. While these designs have succeeded in reducing the cost of test generation, there still remain some problems. Both designs use two EXCLUSIVE OR cascades or trees which occupy a large extra area of the chip in most technology. Moreover, only single faults for stuck and crosspoint faults are considered in these designs [4]–[6], although most of the multiple faults are also detected.

In order to solve these problems of hardware cost and limited fault coverage, Saluja *et al.* [7] presented a design of PLA's with universal tests. The design of Saluja [7] notably excludes the two EXCLUSIVE OR cascades or trees that existed in the previous designs, and has a universal test set which detects multiple stuck and crosspoint faults. However, the design of Saluja [7] still has the following drawbacks. Although it decreases the amount of extra hardware by excluding EXCLUSIVE OR cascades or trees, the reduction is not sufficient since another shift register is appended. Also, the circuitry to select one row line of the AND array adds two gate delays to the normal operation of the PLA; that is, the speed degradation is worse than the PLA's of Fujiwara [4], [5] and Hong [6]. Furthermore, fault coverage is not complete since the bridging faults, which are important in PLA's, are not considered. Although the input test patterns are function independent, the output test responses in the design of Saluja [7] are not function independent. This makes its incorporation with built-in testing difficult.

In this correspondence, a new design of universally testable PLA's is presented. The proposed design has the following properties.

1) It can be tested with function-independent test patterns. For the design of PLA's under the single-fault assumption, both the input test patterns and output test responses are function independent. However, under multiple-fault assumption the output test responses are not function independent.

2) The amount of extra hardware is significantly decreased compared to the previous designs of universally testable PLA's [4]–[7]. The ratio of additional hardware to original hardware can be reasonably small for LSI and VLSI chips. For example, for a PLA with 60 inputs, 60 outputs, and 200 product terms, the ratio is less than 5 percent.

3) Very high fault coverage is achieved, i.e., any combination of stuck faults, crosspoint faults, and adjacent line bridging faults in the PLA are detected.

4) It is appropriate for built-in testing approaches since input test patterns and output test responses are both function independent under single-fault assumption.

5) The design can be applied to the high-density PLA's using array folding techniques.

II. Augmented PLA's for Multiple Faults

A PLA consists of three main sections: the decoder, the AND array, and the OR array. The decoder section usually consists of a collection of one-input decoders or two-input decoders. A PLA can be implemented both in bipolar and MOS technology. In this correspondence, we assume that the PLA's are NOR–NOR implemented in NMOS technology and consist of one-input decoders. These assumptions do not affect our argument. The results given here can easily be modified to be applicable to PLA's implemented in other technology, or with two or more input decoders. A PLA consists of n inputs, $2n$ rows in AND array, m columns (product lines), and ℓ rows (outputs) in OR array.

Consider the augmented PLA shown in Fig. 1. It is augmented by adding a shift register, two columns between the decoder and the AND array, and one column and one row to AND and OR arrays, respectively. The extra connections shown in Fig. 2 are for an implementation in NMOS technology. The augmented PLA can be obtained by excluding two EXCLUSIVE OR cascades from the PLA of Fujiwara [4], [5], although the connections of the added column/row in the AND/OR array are different. Therefore, the amount of extra hardware is significantly decreased compared to the previous designs of universally testable PLA's [4]–[7].

A shift register is added to select a column (product line) in the AND array. Each column P_i is ANDed by the complement of each variable S_i of the shift register as follows:

$$P_i = p_i \cdot \overline{S}_i \qquad \text{for } i = 1, 2, \cdots, m$$

where p_i is a product term generated by the ith column of the original AND array. An extra product line P_{m+1} is added which has devices on all crosspoints in the AND array, i.e.,

$$P_{m+1} = \overline{Q}_1 \cdot \overline{Q}_2 \cdots \overline{Q}_{2n} \cdot \overline{S}_{m+1}$$

where Q_i is the ith row of the AND array. An extra output line Z is added which has devices on all product lines, i.e.,

$$Z = P_1 + P_2 + \cdots + P_m + P_{m+1}.$$

Two extra control lines C_1 and C_2 are added to disable all $\overline{X}_i$'s and X_i's, respectively, as follows:

$$Q_{2i-1} = \overline{X}_i \cdot \overline{C}_1$$

$$Q_{2i} = X_i \cdot \overline{C}_2 \qquad \text{for } i = 1, 2, \cdots, n$$

where X_i is the ith input line and Q_j is the jth row of the AND array. The section composed of $2 \times 2n$ crosspoints on two control lines is called the control array of the augmented PLA.

The augmented PLA has the following properties.

1) The shift register can be used to select an arbitrary column of the AND array by setting 0 to the selected column and 1 to all other columns. Note that since NOR logic is assumed, to select a column or product line P_i, S_i should be 0 and all other S_j's should be 1.

2) The control array can be used to select any row of the AND array, i.e., to sensitize any output line of the decoder. To select Q_{2i-1}, set X_i to 0, all other X_j's to 1, C_1 to 0, and C_2 to 1. To select Q_{2i}, set X_i to 1, all other X_j's to 0, C_1 to 1, and C_2 to 0. Note that in NOR logic selecting a row is equivalent to setting the row to 1 and all other rows to 0.

3) The extra column P_{m+1} in the AND array can be used to test stuck, crosspoint, and bridging faults in the decoder and the control array, and also to test stuck and bridging faults on the rows of the AND array.

4) The extra row and output line Z of the OR array can be used

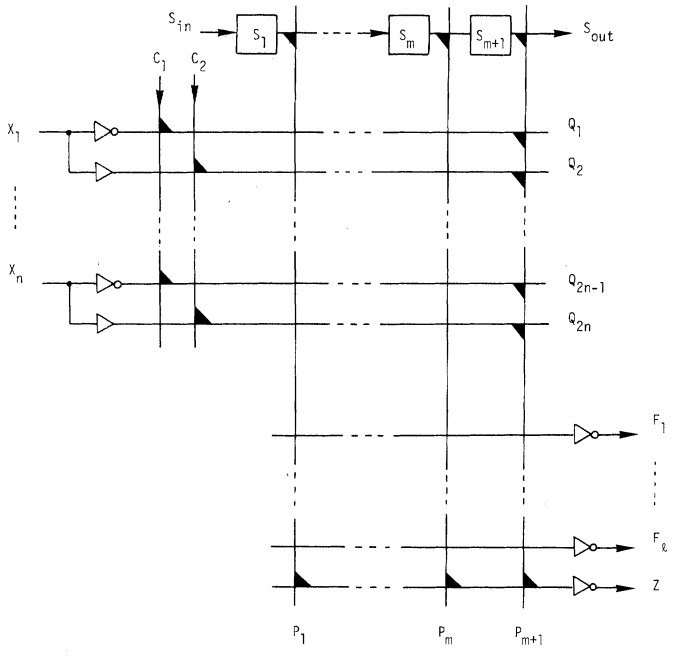
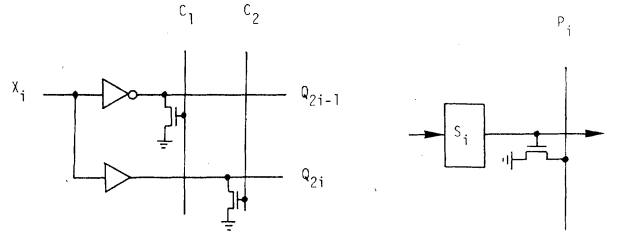


Fig. 1. Augmented PLA for multiple faults.



(a) (b)

Fig. 2. Extra device in NMOS technology.

to test stuck and bridging faults on the columns or product lines and crosspoint faults in the AND array in cooperation with other extra hardware.

The types of faults considered in this section are the multiple faults such that any combination of the following types of faults occurs simultaneously.

1) Stuck faults in the augmented PLA, i.e., stuck-at-0/1 faults on the lines, X_i's, C_i's, Q_i's, P_i's, F_i's, Z, and S_i's.

2) Crosspoint faults in the control array, the AND array, and the OR array. A crosspoint fault is an extra or a missing device fault at the corresponding crosspoint.

3) Adjacent line bridging faults in the control array, the AND array, and the OR array, i.e., bridging faults between C_1 and C_2, Q_i and Q_{i+1}, P_i and P_{i+1}, F_i and F_{i+1}, and F_ℓ and Z. The technology used will determine what effect the bridging will have. In this correspondence, the PLA is assumed to be NOR–NOR implemented in NMOS technology. Hence, a bridging fault between two lines can be assumed to produce an AND function between the lines since low will dominate in NMOS technology. However, the results given here can easily be modified to OR-type bridging faults.

Table I shows the test set $T_{n,m+1}$ to detect all multiple faults mentioned above, where n and m are the numbers of inputs and product lines, respectively, in the original PLA before augmentation. We can show that $T_{n,m+1}$ is the multiple fault test set for the PLA's of Fig. 1 in the following theorem. The proof is omitted due to limitation of space. For the detailed proof, see [20].

Theorem 1: The augmented PLA of Fig. 1 can be tested for all multiple faults, i.e., any combination of stuck faults, crosspoint faults, and bridging faults in the PLA, by the test set $T_{n,m+1}$ shown in Table I.

TABLE I
UNIVERSAL TEST SET $T_{n,m+1}$

	X_1 ... X_i ... X_n	C_1 C_2	S_1 ... S_j ... S_m S_{m+1}
I^1	0 0	1 0	1 1
I^2_j $(j=1,\ldots,m+1)$	0 0	1 0	1 ... 0 1
I^3	1 1	0 1	1 ..... 1 0
I^4_{ij} $(i=1,\ldots,n;\ j=1,\ldots,m+1)$	1 ... 0 ... 1	0 1	1 ... 0 1
I^5_{ij} $(i=1,\ldots,n;\ j=1,\ldots,m+1)$	0 ... 1 ... 0	1 0	1 ... 0 1

By Theorem 1, the test set $T_{n,m+1}$ is shown to be the multiple fault test set for the augmented PLA's of Fig. 1. Furthermore, the test patterns of $T_{n,m+1}$ are function independent, but their responses are not function independent. However, the responses of test patterns can be easily derived from the personality matrix of the PLA.

Using the test set $T_{n,m+1}$, we can construct a test sequence for the augmented PLA's as follows:

$$\tau_{n,m+1} = I^1 I^2_1 I^2_2 \cdots I^2_{m+1} I^3 I^4_{11} I^4_{21} \cdots I^4_{n1} \cdots I^4_{ij} \cdots I^4_{1m+1} \cdots I^4_{nm+1} \cdot I^5_{11} I^5_{21} \cdots I^5_{n1} \cdots I^5_{ij} \cdots I^5_{1m+1} \cdots I^5_{nm+1}.$$

The length of the test sequence is $2nm + 2n + m + 3$.

Finally, we will estimate the area of increase in the augmented PLA's of Fig. 4. Let A_1 be an area of a transistor, let A_2 be an area of a pull-up, and let A_3 be an area of a cell of a shift register. Then the ratio of extra hardware to original hardware is

$$\theta = \frac{A_1(6n + m + \ell + 1) + A_3(m + 1)}{(A_1 + A_2)(3n + \ell) + A_1(2n + \ell)m + A_2(m + \ell)} \times 100 \quad \text{(percent)}.$$

Assuming that $A_1 = A_2$ and $A_3 = 6 \times A_1$, we have

$$\theta = \frac{6n + 7m + \ell + 7}{6n + 2nm + \ell m + m + 3\ell} \times 100 \quad \text{(percent)}.$$

In some of the more recent VLSI chips, PLA's take a large part of the chips. For example, the BELLMAC-32A, a 32 bit single chip microprocessor [16], has eight PLA's. The sizes of these PLA's range from 25 inputs, 12 outputs, and 42 product terms to 50 inputs, 67 outputs, and 190 product terms as shown in Table II. Table II shows the ratio of hardware increase for the BELLMAC-32A if we redesign the eight PLA's with the universally testable PLA's of Fig. 1. The ratio is very small, and for larger PLA's the increase will become much smaller. For example, for a PLA with 60 inputs, 60 outputs, and 200 product terms, the ratio is less than 5 percent.

III. AUGMENTED PLA'S FOR SINGLE FAULTS

In Section II, we have presented a design of universally testable PLA's for multiple faults. The test set $T_{n,m+1}$ of Fig. 1 is universal since the test patterns are independent of the function implemented by the PLA, but their responses are not function independent. However, if we assume the single fault model, we can design an augmented PLA for which both the input test patterns and their

TABLE II
RATIO OF AUGMENTATION FOR BELLMAC-32A

PLA	Inputs	Outputs	Product Terms	Ratio of Increase (%)
1	50	67	190	5.3
2	30	27	120	9.7
3	27	54	181	7.4
4	54	61	134	5.7
5	30	37	153	8.5
6	24	13	44	16.2
7	12	21	58	18.1
8	25	12	42	16.3
Total				7.5

responses are independent of the function. In this section, we will present the PLA design under single fault assumption.

The PLA's for single faults can be similarly augmented as shown in Fig. 3. On the whole, the structure of augmented PLA is the same as that of Fig. 1, except the connections of devices on the extra columns and rows in the AND and the OR arrays. The augmented PLA of Fig. 3 has two extra columns in the AND array and two extra rows in the OR array which satisfy the following conditions.

1) An extra product line P_{m+2} is added which has devices on all crosspoints in the AND array, i.e.,

$$P_{m+2} = \overline{Q}_1 \cdot \overline{Q}_2 \cdots \overline{Q}_{2n} \cdot \overline{S}_{m+2}$$

where Q_i is the ith row of the AND array.

2) An extra product line P_{m+1} is added which has devices at the two crosspoints of Q_1 and Q_2, so that P_{m+1} is always set to 0 during normal operation of the PLA.

3) The existence of a device at the crosspoint of P_{m+1} and Q_3 is arranged so that the total number of absence of devices at the crosspoints of P_j and Q_{2i-1} for all $i = 1, \cdots, n$ and $j = 1, \cdots, m+1$ is odd.

4) Similarly, the existence of a device at the crosspoint of P_{m+1} and Q_4 is arranged so that the total number of absence of devices at the crosspoints of P_j and Q_{2i} for all $i = 1, \cdots, n$, and $j = 1, \cdots, m+1$ is odd.

5) An extra output line Z_1 is added which has devices on alternate crosspoints in the OR array.

6) An extra output line Z_2 is added which has devices on all crosspoints in the OR array.

7) The column P_{m+2} has devices on alternate crosspoints in the OR array.

8) For each row F_i in the OR array, the existence of a device at the crosspoint of P_{m+1} and F_i is arranged so that the number of presence of devices on the crosspoints of $P_1, P_2, \cdots, P_{m+1}$ is odd.

The types of faults considered in this section are the single faults as follows.

1) Single stuck faults in the augmented PLA, i.e., stuck-at-0/1 faults on the lines, X_i's, C_i's, Q_i's, P_i's, Z_1, Z_2, and S_i's.

2) Single crosspoint faults in the control array, the AND array, and the OR array.

3) Single bridging faults between adjacent lines in the control array, the AND array, and the OR array.

The test sequence to detect all single faults mentioned above is the same as that described in Section II. It is constructed by the test set $T_{n,m+2}$ as follows, where n and m are the numbers of inputs and product terms of the original PLA before augmentation, respectively.

$$\tau_{n,m+2} = I^1 I_1^2 I_2^2 \cdots I_{m+2}^2 I^3 I_{11}^4 I_{21}^4 \cdots I_{n1}^4 \cdots I_{ij}^4 \cdots I_{1,m+2}^4 \cdots I_{n,m+2}^4 \cdot I_{11}^5 I_{21}^5 \cdots I_{n1}^5 \cdots I_{ij}^5 \cdots I_{1,m+2}^5 \cdots I_{n,m+2}^5 .$$

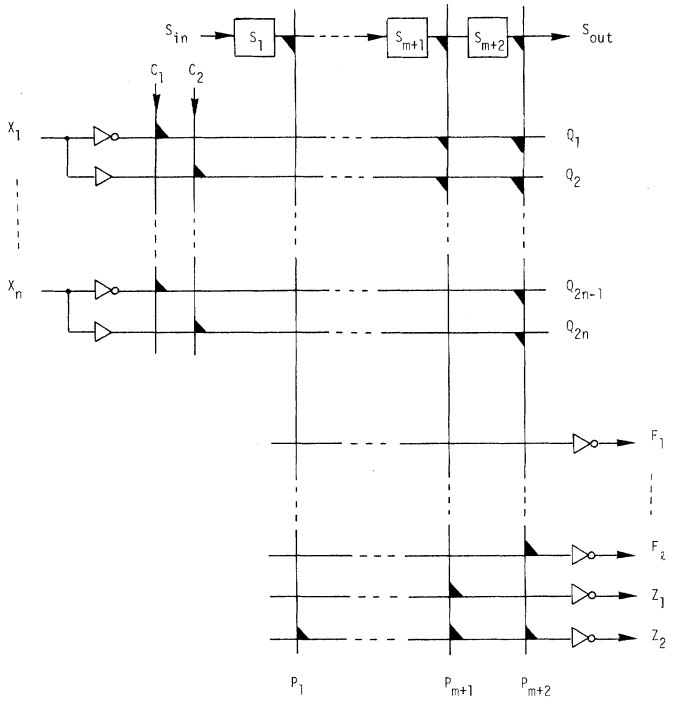


Fig. 3. Augmented PLA for single faults.

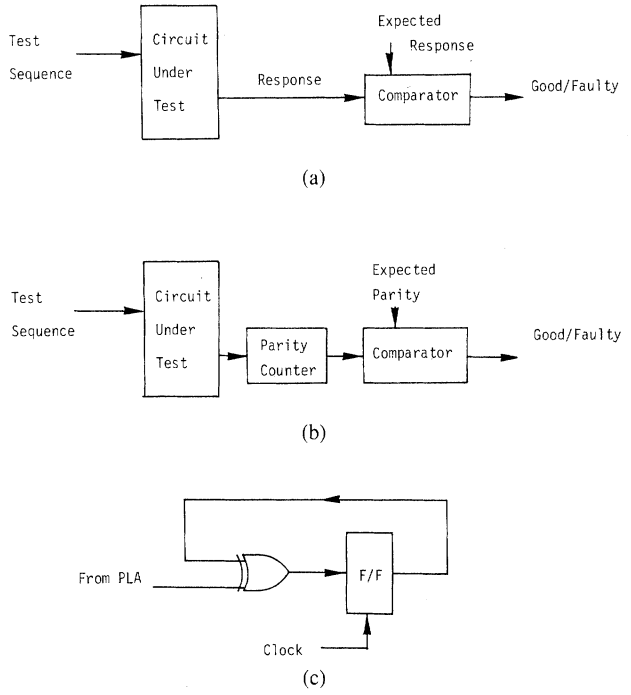


Fig. 4. Testing schemes. (a) Conventional testing scheme. (b) Parity compression testing scheme. (c) Parity counter.

We can show that $\tau_{n,m+2}$ detects all single faults in the PLA's of Fig. 3 in the following theorem.

In the ordinary testing scheme, a sequence of test patterns is applied to the circuit under test and the response of the circuit is compared against the previously obtained correct response one by one as shown in Fig. 4(a). In this section, we consider a different testing scheme using parity counters as shown in Fig. 4(b). The response is compressed by a parity counter and then compared against a reference value only at a predetermined time. The timing of parity checking and the expected parity of the response for the test sequence $\tau_{n,m+2}$ are shown in Table III, where

TABLE III
UNIVERSAL TEST SEQUENCE

Test Sequence	$I^1\ I_1^2 \cdots I_{m+1}^2{}^*\ I_{m+2}^2{}^*\ I^3{}^*\ I_{11}^4 \cdots I_{n,m+1}^4{}^*\ I_{1,m+2}^4{}^* \cdots I_{n,m+2}^4{}^*\ I_{11}^5 \cdots I_{n,m+1}^5{}^*\ I_{1,m+2}^5{}^* \cdots I_{n,m+2}^5{}^*$								
Parity Check Time	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9
Expected Parity F_1	1	:	X	X	X	X	X	X	X
Expected Parity	:	1	:	:	:	:	:	:	:
Expected Parity	:	0	:	:	:	:	:	:	:
Expected Parity F_ℓ	1	1	:	:	:	:	:	:	:
Z_1	Π_1	Π_1	X	X	X	X	X	X	X
Z_2	Π_2	Π_3	Π_2	Π_3	Π_3	Π_3	Π_2	Π_2	Π_2

$\Pi_1=\Pi(\lceil\frac{m+1}{2}\rceil)$ $\Pi_2=\Pi(m+1)$ $\Pi_3=\Pi(m)$

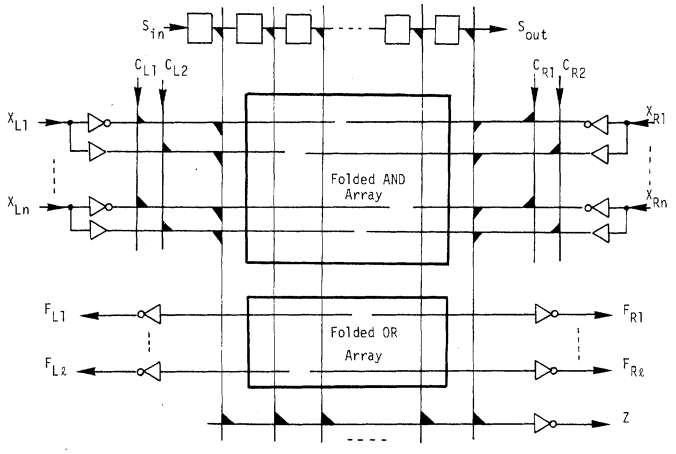


Fig. 5. Augmentation for folded PLA.

$$\Pi(\alpha) = \begin{cases} 0 & \text{if } \alpha \text{ is even} \\ 1 & \text{if } \alpha \text{ is odd} \end{cases}$$

and $\lceil\beta\rceil$ is the smallest integer greater than or equal to β, and X means not to check at the time.

Theorem 2: The augmented PLA of Fig. 3 can be tested for all single stuck faults, crosspoint faults, and bridging faults in the PLA by applying test sequence $\tau_{n,m+2}$ and comparing the compressed parity of the response against the reference values at the predetermined time as shown in Table III.

The test sequence $\tau_{n,m+2}$ and its parity sequence shown in Table III are both function independent. Moreover, the length of the parity sequence is 9, and hence, the cost of storing the correct response is very low. The test sequence $\tau_{n,m+2}$ can be easily generated by a shift register. Hence, it is concluded that the PLA design of Fig. 3 and the testing scheme of Fig. 4(b) are suitable to built-in testing.

IV. CONCLUSIONS

The new design of universally testable PLA's presented in this paper has the following merits. 1) It can be tested with function-independent test patterns. 2) The amount of extra hardware is significantly decreased compared to the previous designs of universally testable PLA's. 3) Very high fault coverage is achieved. 4) It is suitable to built-in testing. 5) It can be applied to the high density PLA's using folding techniques. Fig. 5 shows an augmented folded PLA for multiple faults.

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