A Design of Programmable Logic Arrays with Random Pattern-Testability

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Abstract—**Programmable logic arrays (PLA's) are very suitable to VLSI and have become a popular and effective tool for implementing logic functions, because of their regular structure like memory. On the other hand, built-in self-test approach using linear feedback shift registers (LFSR's) is currently being widely investigated as one of the attractive testing techniques for VLSI circuits. However, random testing using random patterns are not always effective for achieving a high fault coverage for the high fan-in circuits such as programmable logic arrays (PLA's).**

This paper presents a new testable design of PLA's with high fault coverage for random test patterns. The proposed design is realized with low area overhead by adding a mask array between the input-decoder and the AND array of the PLA. Several variations of the proposed approach are also presented. The probability of detection of faults and the test length are discussed for both stuck-type and crosspoint-type faults in order to estimate the fault coverage achievable with the random patterns for those PLA's.

I. Introduction

SCAN design techniques such as Level Sensitive Scan Design (LSSD) have been used mainly in mainframes [1]. Although those approaches have indeed succeeded in reducing the difficulty of testing sequential logic, this type of testing still has some drawbacks: Storage of huge amount of test patterns is still bothersome since special test-generation software for scan design is required, and testing is slow because of the shifting of patterns through the scan path.

Built-in self-test (BIST) based on random testing attracts a good deal of attention as one of the approaches that alleviate such problems [1]. The major difficulty in such random testing with random test patterns is the low fault coverage for very high fan-in circuits such as programmable logic arrays (PLA's). Hence, for BIST PLA's it is necessary either to employ deterministic (not random) test patterns or to augment a PLA to make it random-pattern-testable. The former includes BIST PLA designs with universal test patterns [2], [3]. Although these BIST PLA's can achieve very high fault coverage, the area overhead is still high. For the latter approach, two random-pattern-testable designs of PLA's were proposed by Eicherberger and Lindbloom [4] and Ha and Reddy [5]. However, these methods also have high area overhead due to their extra circuitry for controlling a large number of product lines of PLA's. In this paper, we propose an approach to designing a random-pattern-testable PLA with low area overhead by adding a mask array only between the input-decoder and the AND array. Several variations of the proposed PLA are also presented to discuss the trade-off between fault coverage and area overhead. For those PLA's, we consider the probability of fault detection for stuck-type and crosspoint-type faults and estimate the test length necessary for achieving a given test confidence, say 0.9, to compare the effectiveness of those PLA's.

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II. Fault Detection Probability

There are several works on the analysis of the required test length to achieve a desired level of test confidence using a random model [6]–[8] or a pseudorandom model [9]–[10]. In this paper we consider random testing based on random model for analysis of test quality. First, we analyze detection probabilities of stuck-at and crosspoint faults in PLA's.

Consider the PLA shown in Fig. 1(a). Fig. 1(b) shows the equivalent AND-OR circuit at gate level concerning the jth output Z_j. Let m be the number of inputs (i.e., fan-in) of the OR gate and let k_i be the fan-in of the ith AND gate G_i. For the purpose of probabilistic analysis, a simple tree structure, i.e., a two-level AND-OR circuit without reconvergence is used as a model. It is also assumed that the probabilities of a "0" and "1" occurring at primary inputs are equal, i.e., $1/2$.

Let us now compute the probability of detecting a stuck-at-0 or stuck-at-1 fault f_1 at an input of the AND gate G_i. Since the fan-in of G_i is k_i, the probability of propagating the fault to the output of G_i is $1/2^{ki}$. Further to propagate the fault to the output of the OR gate, the outputs of all the other AND gates should be 0. Hence, the detection probability of the fault f_1 is

$$P_d(f_1) = \frac{1}{2^{ki}} \prod_{j \neq i} \left(1 - \frac{1}{2^{kj}}\right). \tag{1}$$

Next let us consider a crosspoint fault f_2 shown in Fig. 2(a). Since in this case there is a transistor at the crosspoint, the fault f_2 is a missing-device fault. This type of fault is equivalent to an input stuck-at fault. Hence, the probability of detecting the fault f_2, $P_d(f_2)$, is equal to (1).

For extra-device faults which corresponds to the presence of unintended transistor at a crosspoint, there are two cases f_3 and f_4 as shown in Fig. 2(b) and (c). The fault f_3

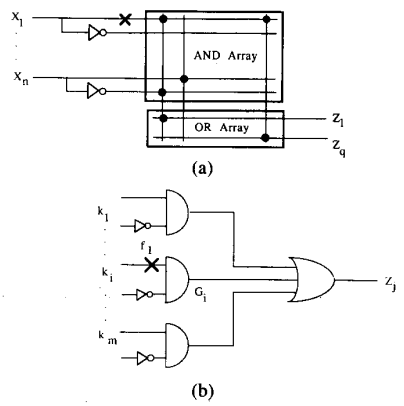

Fig. 1. Equivalent AND-OR circuit of PLA. (a) PLA. (b) Equivalent AND-OR.

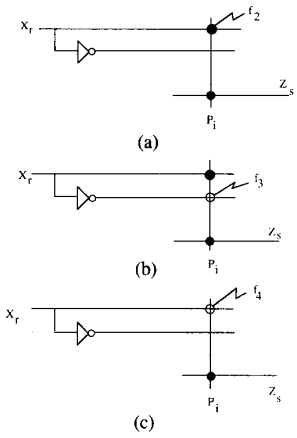

Fig. 2. Crosspoint faults in PLA.

is equivalent to an input stuck-at-0 fault of AND gate, and hence the detection probability of the fault, $P_d(f_3)$, is equal to (1).

To detect the fault f_4 (see Fig. 2(c)), all the inputs of the AND gate G_i should be 1, the input X_r corresponding to f_4 should be 0, and the outputs of all other AND gates should be 0. These probabilities are $1/2^{ki}$, $1/2$, and $1 - 1/2^{kj}$, respectively. Hence the probability of detecting fault f_4 is

$$P_d(f_4) = \frac{1}{2^{ki+1}} \prod_{j \neq i} \left(1 - \frac{1}{2^{kj}}\right) \tag{2}$$

which is half of (1).

Let L be the number of independent random input patterns applied to detect a fault f and let $P_d(f)$ be the probability of detecting the fault f by one input pattern. Then, the probability that the fault f is detected by at least one out of L patterns is given by

$$P_d(f, L) = 1 - \{1 - P_d(f)\}^L. \tag{3}$$

This equation allows us to calculate the required test length for different desired levels of test confidence. To achieve a high level of test confidence, $P_d(f)$ must take a high value. However, as seen in (1) and (2), $P_d(f)$ is very low in general.

Since PLA's are very high fan-in circuits, the values of $1/2^{ki}$ and $1/2^{kj}$ are very low, i.e., $1/2^{ki} \ll 1/2$ and $1/2 \ll (1 - 1/2^{kj})$. Hence, the values of $P_d(f)$ in equations (1) and (2) are influenced much more by the first factor, $1/2^{ki}$, than by the second factor, $1 - 1/2^{kj}$. For example, suppose $k_i = 24$ (2^{24} is approximately 16×10^6). To detect the fault, 16×10^6 random patterns are necessary to be applied in average. However, if those fan-ins are halved, the number of required random patterns is greatly decreased to $2^{12} = 4096$.

III. Random-Pattern-Testable PLA's

PLA's are random-pattern-resistant due to high fan-in of the product lines and output lines. Eichelberger and Lindbloom [4] proposed a modification method that makes a PLA testable with random patterns, as shown in Fig. 3. The additional circuitry consists of two sections called segment selector and product term selector. In the segment selector, control signals u_i ($i = 1, 2, \cdots, s$) are generated from random test variables t_i ($i = 1, 2, \cdots, \log_2 s$) under control of the test signal T so that the test patterns applied at the primary inputs are masked and only one group of inputs are selected randomly at a time. In the product term selector, the random variable inputs t_i ($i = 1 + \log_2 s, 2 + \log_2 s, \cdots, \log_2 s + \log_2 p$) are decoded so that, at most, one product term can be selected at a time, where s and p are the numbers of segments and product terms, respectively.

As shown in (1) and (2), the probability of fault detection is determined by two factors $1/2^{ki}$ and $(1 - 1/2^{kj})$. The above method is intended to increase the first factor by segment selection and the second factor by product term selection. However, the area overhead is very high, especially for the product term selector.

Ha and Reddy [5] have proposed a different design of random-pattern-testable PLA's with less area overhead, as shown in Fig. 4. The decoder of the original PLA is augmented so that all the inverters in the decoder are changed to 2-input NOR gates and the same number of extra control inputs as the original primary inputs are added. Further, a shift register is added to the original PLA. The extra transistors of NOR gates are provided to apply weighted random patterns on the bit lines, i.e., to increase the probability of occurrence of zeros on the decoded input lines. The shift register is used to select a group of product lines. Indeed, the PLA of Ha and Reddy [5] gives a high fault coverage. However, the area overhead would become high due to the extra shift register when the number of product lines grows, and the pin overhead would be severe due to the extra control inputs whose number is the same as the primary inputs.

Since PLA's are very high fan-in circuits, the values of $1/2^{ki}$ and $1/2^{kj}$ are very low, i.e., $1/2^{-ki} \ll 1/2$ and $1/2 \ll (1 - 1/2^{kj})$. Hence, the values of $P_d(f)$ in equations (1) and (2) are much more influenced by the

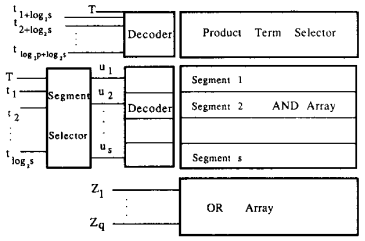

Fig. 3. PLA of Eichelberger and Lindbloom [4].

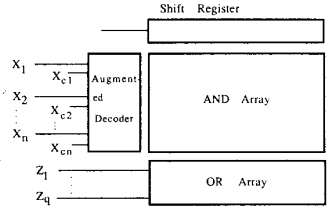

Fig. 4. PLA of Ha and Reddy [5].

first factor, $1/2^{ki}$, compared with the second factor, $1 - 1/2^{kj}$. In order to reduce the area overhead, here we do not append the circuitry for product line selection but adopt a mechanism which increases only the first factor to achieve a high fault coverage.

Fig. 5 shows two designs of random-pattern-testable PLA's proposed in this paper. Both designs have the additional circuitry consisting of a programmable mask array which masks some inputs of the AND array. The second design of Fig. 5(b) has another extra circuitry, a mask decoder, which controls the mask array as follows: When $T = 0$, all mask control signals u_i ($i = 1, 2, \cdots, r$) are disabled, "0," and the PLA works in the normal way. When $T = 1$, exactly one of the mask control signals is enabled, "1," to select one mask in the mask array. In the PLA of Eichelberger and Lindbloom [4], the segmentation of the AND array is fixed independently of the function of the PLA. This is not effective for the purpose of increasing the probability of fault detection of the PLA. We introduce here the mask array which can be programmed to increase effectively the fault detection probability of the PLA. Fig. 6 shows an example of the proposed PLA with a mask decoder implemented in nMOS technology.

The principle of masking is illustrated in Fig. 7 using an AND-OR equivalent circuit. In the figure, by controlling $u_1 = 0$, $u_2 = 1$, a_3 and a_4 are masked and only the inputs of a_1 and a_2 are applied to the AND gate. This effects that the fan-in of the AND gate is decreased from 4 to 2. Here, those control lines such as u_1 and u_2 are called "*mask-control lines*," those masked inputs such as a_3 and a_4 are called "*mask*," and those unmasked inputs such as a_1 and a_2 are called "*window*."

We have presented four schemes of random-pattern-testable PLA's; Eichelberger and Lindbloom's PLA, Ha and Reddy's PLA, and two new PLA's proposed in this

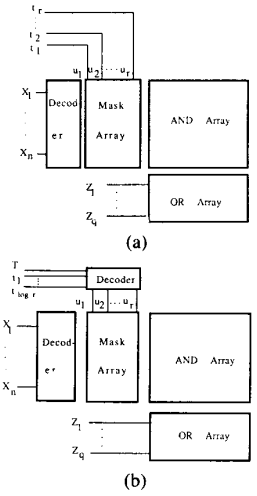

Fig. 5. The proposed PLA.

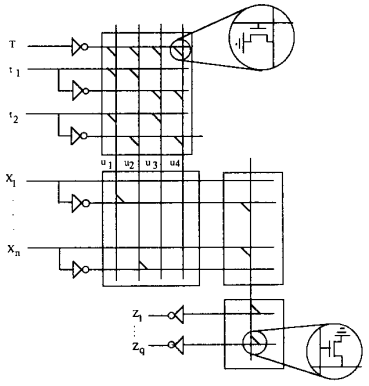

Fig. 6. Realization in nMOS.

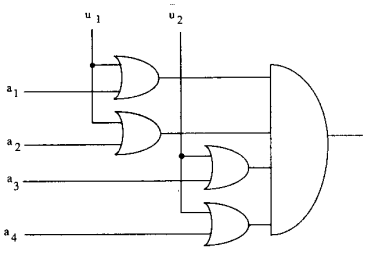

Fig. 7. Masking of AND gate.

paper. To compare the area overhead, let us make a rough estimate in the following. The additional circuitry of Eichelber and Lindbloom's PLA is mainly composed of the segment selector and the product term selector. The segment selector occupies almost the same area as the mask array plus its decoder of the PLA of Fig. 5. Hence the area required for product term selection is purely extra compared with our PLA. Similarly, the additional circuitry of Ha and Reddy's PLA consists of the augmented decoder and the shift register as shown in Fig. 4. The additional area in the augmented decoder is also almost

the same as that of the mask array of Fig. 5. Therefore, the shift register is purely extra area overhead compared with our PLA of Fig. 5. Moreover, the Ha and Reddy's PLA requires extra control inputs whose number is the same as the primary inputs, and thus the pin overhead is also severe.

In most real PLA's, the number of product terms is usually much larger than the number of primary inputs. Therefore, our PLA's proposed here succeed in reducing a huge amount of extra area/pin overhead compared with the previous PLA's. Moreover, it can be shown that the proposed PLA is not worse than the previous PLA's for test quality. We shall consider this in the next section by estimating the probability of fault detection for those PLA's.

IV. Fault Detection Probability of Proposed PLA's

We shall consider the fault detection probabilities of the following four schemes of PLA's as well as Eichelberger–Lindbloom and Ha–Reddy PLA's.

Scheme 0: The normal PLA with no extra circuitry.

Scheme 1: The augmented PLA of Fig. 5(a). Random patterns with equally likely 0 and 1 are assumed to be applied to the mask-control inputs as well as the primary inputs.

Scheme 2: The augmented PLA of Fig. 5(b). Random patterns with equally likely 0 and 1 are assumed to be applied to the mask-control inputs including input T as well as the primary inputs.

Scheme 3: The augmented PLA of Fig. 5(b). Random patterns with equally likely 0 and 1 are assumed to be applied to the primary inputs and the mask-control inputs except input T. While random test patterns are applied, input T is fixed to "1."

The difference between Schemes 2 and 3 is whether random patterns are applied to T or not. In Scheme 2, the augmented PLA can be equivalent to the original PLA when $T = 0$. Hence, all detectable faults in the original PLA are also detectable in the augmented PLA. However, in Scheme 3, some detectable fault in the original PLA may become undetectable in the augmented PLA because T is restricted to be always "1" during testing.

To compare the effectiveness of the above four schemes and Eichelberger–Lindbloom and Ha–Reddy schemes, we shall estimate the probability of detecting faults for them. For the purpose of probabilistic analysis, we shall use the equivalent AND-OR circuit without fanout as a model, as shown in Fig. 8. Fig. 8(a) illustrates the mask patterns for Scheme 1, where no pair of masks overlap each other, and the union of all masks covers the fan-in of all AND gates. Similarly, Figure 8(b) shows the mask patterns for Schemes 2 and 3, where no pair of windows overlap each other, and the union of all windows covers the fan-in of all AND gates.

Let m and r be the fan-in of the OR gate and the number of mask patterns, respectively. Assume that all the AND gates have the same fan-in, say k, and that the number of

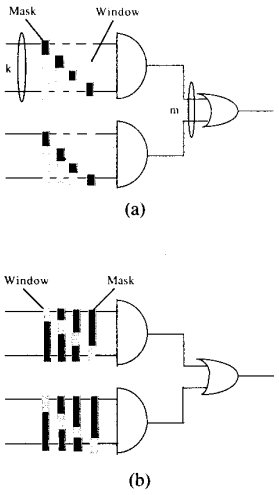

Fig. 8. Masking of PLA.

mask patterns is the power of 2, i.e, $r = 2^N$ for some integer N.

Let us consider an input stuck-at-0 (or -1) fault, say f, of an AND gate.

For Scheme 0, the detection probability of the fault f is

$$P_0(f) = \frac{1}{2^k}\left(1 - \frac{1}{2^k}\right)^{m-1}. \tag{4}$$

For Scheme 1, we assume that all mask patterns have the same size of masks, say s. Since no pair of masks overlap each other and the union of all masks covers the fan-in of the AND gate (see Fig. 8(a)), we have $k = rs$. Also we assume that random patterns with equally likely 0 and 1 are applied to the mask-control lines as well as the primary inputs. Hence, each of 2^r-patterns appears at the mask-control lines equally likely with the probability of $1/2^r$.

The detection probability of fault f when i mask-control lines are enabled simultaneously is

$$\frac{1}{2^{(r-i)s}}\left(1 - \frac{1}{2^{(r-i)s}}\right)^{m-1}.$$

The number of occurrence of this case is ${}_{r-1}C_i$. Hence, the detection probability of fault f is

$$P_1(f) = \frac{1}{2^r}\sum_{i=0}^{r-1} {}_{r-1}C_i \frac{1}{2^{(r-i)s}}\left(1 - \frac{1}{2^{(r-i)s}}\right)^{m-1}. \tag{5}$$

For Scheme 2, we assume that all mask patterns have the same size of windows, way w. Since no pair of windows overlap each other and the union of all windows covers the fan-in of the AND gate (see Fig. 8(b)), we have $k = rw$. Also we assume that random patterns with equally likely 0 and 1 are applied to the mask-control inputs as well as the primary inputs. Hence, each of r one-hot patterns appears at the mask-control lines with the probability of $1/2r$ and all 0 pattern appears with the probability

of $1/2$. Hence, the detection probability of fault f is

$$P_2(f) = \frac{1}{2^{k+1}}\left(1 - \frac{1}{2^k}\right)^{m-1} + \frac{1}{2r}\frac{1}{2^w}\left(1 - \frac{1}{2^w}\right)^{m-1}. \quad (6)$$

For Scheme 3, we assume that all mask patterns have the same size of windows, say w, and hence we have $k = rw$. Also we assume that random patterns are applied to the mask-control inputs except T. Hence, each of r one-hot patterns appears at the mask-control lines with the probability of $1/r$.

The detection probability of fault f is thus

$$P_3(f) = \frac{1}{r}\frac{1}{2^w}\left(1 - \frac{1}{2^w}\right)^{m-1}. \quad (7)$$

Next let us consider the scheme of Eichelberger and Lindbloom [4]. To simplify our comparison, we assume that the mechanism to select a group of inputs in Eichelberger–Lindbloom's scheme is equivalent to that of Scheme 3, i.e., each segment corresponds to a mask pattern (see Fig. 8(b)). Then the probability of propagating the fault f to the output of the AND gate is $1/(r2^w)$. Each single product term is selected at a time by the product term selector with the probability of $1/p$ where p is the number of product terms. In Fig. 8(b), the probability of propagating a faulty signal of an AND gate to the output of the OR gate is $1/m$ where m is the fan-in of the OR gate. The detection probability of fault f is thus

$$P_{\mathrm{EL}}(f) = \frac{1}{r}\frac{1}{2^w}\frac{1}{m}. \quad (8)$$

For the scheme of Ha and Reddy [5] shown in Fig. 4, when random patterns with equally likely 0 and 1 values are applied to the primary inputs X_i and extra inputs X_{ci} ($i = 1, 2, \cdots, n$), the probabilities of the output values of the augmented decoder, which are input values to the AND array, are 0.75 for one and 0.25 for zero. Using the shift register a group of product terms can be selected at a time. When we assume that each product term is selected randomly with the probability of $1/m$, the probability of detecting fault f is

$$P_{\mathrm{HR}}(f) = \frac{0.75^k}{m}. \quad (9)$$

When we optimistically assume that a desired product term always succeeds to be selected or sensitized, then we have

$$P_{\mathrm{HR}}(f) = 0.75^k. \quad (10)$$

Table I shows the detection probabilities of the fault f for six schemes of PLA's when $r = 4$.

To achieve a test confidence of more than C_L with L random patterns, from (3) we have

$$P(f, L) = 1 - \{1 - P(f)\}^L > C_L. \quad (11)$$

TABLE I
COMPARISON OF FAULT DETECTION PROBABILITY WHEN $r = 4$

Fan-In		Fault Detection Probability					
		Scheme					
OR	AND	0	1	2	3	EL	HR
10	20	9.5×10^{-7}	1.6×10^{-3}	2.9×10^{-3}	5.8×10^{-3}	7.8×10^{-4}	3.2×10^{-3} — 3.2×10^{-4}
10	40	9.1×10^{-13}	6.1×10^{-5}	1.2×10^{-4}	2.4×10^{-4}	2.4×10^{-5}	1.0×10^{-5} — 1.0×10^{-6}
50	20	9.5×10^{-7}	5.9×10^{-4}	8.2×10^{-4}	1.6×10^{-3}	1.6×10^{-4}	3.2×10^{-3} — 6.3×10^{-5}
50	40	9.1×10^{-13}	5.8×10^{-5}	1.2×10^{-4}	2.3×10^{-4}	4.9×10^{-6}	1.0×10^{-5} — 2.0×10^{-7}

TABLE II
COMPARISON OF TEST LENGTH WHEN $r = 4$

Fan-In		Test Length for Test Confidence 0.9					
		Scheme					
OR	AND	0	1	2	3	EL	HR
10	20	2.4×10^{6}	1.4×10^{3}	7.8×10^{2}	3.9×10^{2}	2.9×10^{3}	7.3×10^{2} — 7.3×10^{3}
10	40	2.5×10^{12}	3.8×10^{4}	1.9×10^{4}	9.5×10^{3}	9.4×10^{4}	2.9×10^{5} — 2.9×10^{6}
50	20	2.4×10^{6}	3.9×10^{3}	2.8×10^{3}	1.4×10^{3}	1.5×10^{4}	7.2×10^{2} — 3.6×10^{4}
50	40	2.5×10^{12}	3.9×10^{4}	2.0×10^{4}	9.9×10^{3}	4.7×10^{5}	2.3×10^{5} — 1.2×10^{7}

Assuming $P(f) \ll 1$, test length L can be approximated as

$$L \approx \frac{-\log_e(1 - C_L)}{P(f)}. \quad (12)$$

Table I shows the detection probability of the AND input stuck-at fault and Table II shows the test length necessary for achieving a test confidence of more than 0.9 for six schemes of PLA's when $r = 4$.

From the results of these tables, it is shown that both fault detection probability and test length for all schemes except Scheme 0 are greatly improved compared with Scheme 0. Although Scheme 3 is the most effective with respect to the fault detection probability and test length, there is little difference among Schemes 1, 2, 3, EL, and HR. Therefore, when we consider the area overhead of the augmented PLA, Scheme 1 might be the best among them in the sense that the fault detection probability can be greatly improved with very low area overhead.

V. CONCLUSIONS

We have proposed a new design of PLA's that are testable with random patterns. By inserting a programmable mask array between the input decoder and the AND array, a high fault coverage can be achieved with random patterns. The area and/or pin overhead of additional circuitry is much lower than the previous PLA's [4], [5].

We have considered the probabilities of fault detection for both stuck-at faults and crosspoint faults. Although the model used to analyze the probabilities is a simple tree structure, by estimating the number of patterns required to achieve a desired test confidence, we have shown that any PLA can be modifed to be random-pattern-testable with very low area and pin overhead.

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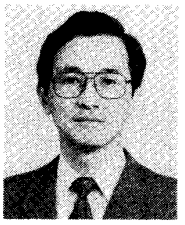

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