

Design of Diagnosable Sequential Machines Utilizing Extra Outputs

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A method is developed to modify a given machine to an output-observable one by adding a minimum number of extra outputs. For the k -output-observable sequential machines, an input-output sequence w_1, w_2, \dots, w_k such that w_1 is an input-output sequence which passes through all transitions of the given state table and w_2 is an arbitrary input-output sequence of length k , can be shown to be a checking sequence; the hence nearly minimum length checking sequences are obtained.

1. Introduction

On the fact that the problem for sequential machines, it is desirable to find an efficient procedure to construct checking sequences of short length. An efficient approach to the design of checking experiments, called the transition checking approach, was first introduced by Heims¹. However, for machines without distinguishing sequences, his procedure yields very long test sequences. Hence, for machines without distinguishing sequences, new approaches are proposed to the problem. One approach is to modify a given machine by adding extra inputs²⁻⁴ or outputs⁵⁻¹⁰ so that the modified machine has a distinguishing sequence. For an n -state, m -input symbol machine, these procedures give a bound on the length of checking sequences that is approximately nm^2 . Therefore, for machines with a large number of states, these procedures yields very long experiments, which make them impractical.

In order to overcome this, Reprinted from the output-observable sequential machines which are not output-observable sequential machines, we can find a shorter checking sequence. For an input-output sequence which passes through all transitions of the given state table and w_2 is an arbitrary input-output sequence of length k , we can show that w_1, w_2 is a checking sequence, and consequently shorter than the

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A method is developed to modify a given machine to an output-observable one by adding a minimum number of extra outputs. For the k -output-observable sequential machines, an input-output sequence $\omega_1\omega_2$, such that ω_1 is an input-output sequence which passes through all transitions of the given state table and ω_2 is an arbitrary input-output sequence of length k , can be shown to be a checking sequence, and hence nearly minimum length checking sequences are obtained.

1. Introduction

On the fault detection problem for sequential machines, it is desirable to find an efficient procedure to construct checking sequences of short length. An efficient approach to the design of checking experiments, called the *transition checking approach*, was first introduced by Hennie¹⁾. However, for machines without distinguishing sequences, his procedure yields very long test sequences. Hence, for machines without distinguishing sequences, new approaches are proposed to this problem. One approach is to modify a given machine by adding extra inputs²⁻⁴⁾ or outputs⁵⁻¹⁰⁾ so that the modified machine has a distinguishing sequence. For an n -state, m -input symbol machine, these procedures give a bound on the length of checking sequences that is approximately mn^2 . Therefore, for machines with a large number of states, these procedures yields very long experiments, which make them impractical.

In order to overcome this, we introduce the *output-observable sequential machines* which have checking sequences of short length. For a k -output-observable sequential machine, we can find a checking sequence $\omega_1\omega_2$, such that ω_1 is an input-output sequence which passes through all transitions of the given state table and ω_2 is an arbitrary input-output sequence of length k . Since a checking sequence must pass through all transitions of the given state table, the input-output sequence ω_1 is shorter than every possible checking sequence, and consequently shorter than the

minimum length checking sequence. Hence, the length of the checking sequence $\omega_1\omega_2$ is nearly minimum. Moreover, it is shown that the procedure of organizing checking sequences is simple and systematic.

In this paper we describe a method for the modification of a given machine to an output-observable one by adding a minimum number of extra outputs, and an efficient procedure for the design of checking experiments of the output-observable sequential machines.

2. Output-Observability and Semi-FSR Realizability

A sequential machine M will be represented by a quintuple $M=(S, I, Z, \delta, \lambda)$ where S is a finite set of states, I is the input alphabet, and Z is the output alphabet, $\delta: S \times I^* \rightarrow S$ is the next-state function, and $\lambda: S \times I^* \rightarrow Z^*$ is the output function. The sequential machines considered in this paper are assumed to be reduced and strongly connected Mealy machines, such that binary codes are already assigned to their output symbols, i.e., the output function λ is represented by a direct product, $z_1 \times \cdots \times z_p$, of binary output functions z_1, \dots, z_p shown in Fig. 1.

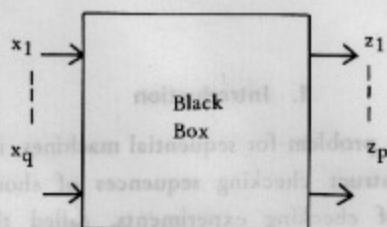


Fig. 1 Sequential machine M

Definition 1: A decomposition over a set of states S is a collection of subsets of S , called blocks, such that their set union is S . A decomposition such that its blocks are pairwise disjoint is called a partition.

Definition 2: We define a relation \sim_{π} corresponding to a decomposition π , such that $S_i \sim_{\pi} S_j$ for $S_i, S_j \in S \iff S_i$ and S_j belong to the same block of π . For $B_i, B_j \in \pi$, $B_i \sim_{\pi} B_j \iff S_i \sim_{\pi} S_j$ for all $S_i \in B_i$ and $S_j \in B_j$.

Definition 3: A reduced form $\tilde{\pi}$ of π is a decomposition satisfying the following conditions:

- (1) $S_i \sim_{\tilde{\pi}} S_j \iff S_i \sim_{\pi} S_j$,
- (2) $B_i \sim_{\tilde{\pi}} B_j$ for all $i \neq j$, where B_i and $B_j \in \pi$.

Definition 4: Let $\tilde{\pi}$ and $\tilde{\tau}$ be two relations over S . The relation $\tilde{\pi\tau}$ and $\tilde{\pi+\tau}$ are defined as follows:

$$S_i \sim_{\tilde{\pi\tau}} S_j \iff S_i \sim_{\tilde{\pi}} S_j \text{ and } S_i \sim_{\tilde{\tau}} S_j, \quad S_i \sim_{\tilde{\pi+\tau}} S_j \iff S_i \sim_{\tilde{\pi}} S_j \text{ or } S_i \sim_{\tilde{\tau}} S_j.$$

The reduced decompositions $\pi\tau$ and $\pi+\tau$, which correspond to the relations $\tilde{\pi\tau}$ and $\tilde{\pi+\tau}$, are called the product and the union of π and τ respectively.

Definition 5: $\pi \leq \tau$ (π is finer than τ) if and only if $S_i \sim_{\pi} S_j \iff S_i \sim_{\tau} S_j$. Let I be the partition in which all elements of S form one block, and let O be the partition in which every block is a singleton.

Definition 6: A sequential machine M is called to be (k_1, k_2, \dots, k_p) -semi-FSR realizable with respect to π if the next-state function of M can be realized with the feedback-shift-register circuit shown in Fig. 2 such that binary codes of its state assignment are distinct among the states belonging to the same block of π .

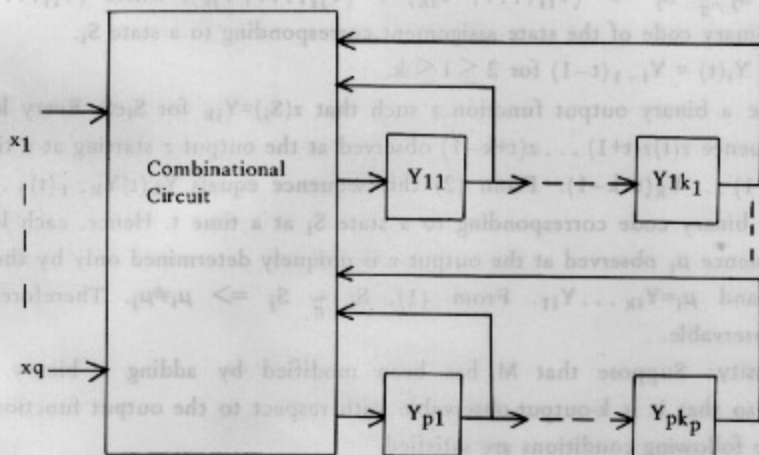


Fig. 2 Feedback-shift-register circuit

Definition 7: A sequential machine M is called to be (k_1, \dots, k_p) -output-observable with respect to the output function $z_1 \times \dots \times z_p$ and a decomposition π if the following conditions are satisfied.

(1) Each output sequence μ_{ij} of length k_j observed at the output function z_j ($j=1, \dots, p$) is uniquely determined only by the initial state S_i independently of input sequences.

(2) $S_i \sim_{\pi} S_j \implies (\mu_{i1}, \dots, \mu_{ip}) \neq (\mu_{j1}, \dots, \mu_{jp})$ for all S_i and $S_j \in S$.

When a decomposition π is I , M is briefly called to be *output-observable*.

The following lemmas can be readily proved by Definitions 6 and 7.

Lemma 1: A sequential machine M is (k_1, \dots, k_p) -semi-FSR realizable with respect to π if and only if there exist p decompositions π_1, \dots, π_p , such that $\pi = \pi_1 + \dots + \pi_p$, and for each i ($i=1, \dots, p$) M is k_i -semi-FSR realizable with respect to π_i .

Lemma 2: A sequential machine M is (k_1, \dots, k_p) -output-observable with respect to the output function $z_1 \times \dots \times z_p$, and a decomposition π if and only if there

exist p decompositions π_1, \dots, π_p , such that $\pi = \pi_1 + \dots + \pi_p$ and for each i ($i=1, \dots, p$) M is k_i -output-observable with respect to the output function z_i and the decomposition π_i .

Theorem 1: The necessary and sufficient condition for a sequential machine M to be modified by adding a binary output function z so that it will be k -output-observable with respect to the output function z and a decomposition π is that M is k -semi-FSR realizable with respect to π .

Sufficiency: Suppose that M is k -semi-FSR realizable with respect to π . Let Y_1, \dots, Y_k be its state assignment variables, and let $Y_i(t)$ be a value of Y_i at a time t . Then the following conditions are satisfied.

(1) $S_i \sim_{\pi} S_j \Rightarrow (Y_{i1}, \dots, Y_{ik}) \neq (Y_{j1}, \dots, Y_{jk})$, where (Y_{i1}, \dots, Y_{ik}) denotes a binary code of the state assignment corresponding to a state S_i .

(2) $Y_i(t) = Y_{i-1}(t-1)$ for $2 \leq i \leq k$.

Define a binary output function z such that $z(S_i) = Y_{ik}$ for $S_i \in S$. Every length- k output sequence $z(t)z(t+1) \dots z(t+k-1)$ observed at the output z starting at a time t is $Y_k(t)Y_k(t+1) \dots Y_k(t+k-1)$. From (2) this sequence equals $Y_k(t)Y_{k-1}(t) \dots Y_1(t)$ which is a binary code corresponding to a state S_i at a time t . Hence, each length- k output sequence μ_i observed at the output z is uniquely determined only by the initial state S_i , and $\mu_i = Y_{ik} \dots Y_{i1}$. From (1), $S_i \sim_{\pi} S_j \Rightarrow \mu_i \neq \mu_j$. Therefore M is k -output-observable.

Necessity: Suppose that M has been modified by adding a binary output function z so that it is k -output-observable with respect to the output function z and π . Then the following conditions are satisfied.

(1) Each output sequence μ_i of length k observed at the output z is uniquely determined only by the initial state S_i .

(2) $\mu_i \neq \mu_j$ for all $S_i \sim_{\pi} S_j$.

When $\mu_i = Z_1 Z_2 \dots Z_k$, let a state assignment be $(Y_{i1}, \dots, Y_{ik}) = (Z_k, \dots, Z_1)$. If $\delta(S_i, I_q) = S_j$ for some input I_q , then $\mu_j = Z_2 Z_3 \dots Z_k Z_{k+1}$ where Z_{k+1} is uniquely determined by S_i and I_q from (1). Hence, we can define a feedback function f such that $f(S_i, I_q) = Z_{k+1}$. Since $\mu_i = Z_1 Z_2 \dots Z_k$ and $\mu_j = Z_2 Z_3 \dots Z_k Z_{k+1}$ for $\delta(S_i, I_q) = S_j$, we have

$$Y_i(t) = Y_{i-1}(t-1) \text{ for } 2 \leq i \leq k.$$

From (2) $S_i \sim_{\pi} S_j \Rightarrow \mu_i \neq \mu_j \Rightarrow (Y_{i1}, \dots, Y_{ik}) \neq (Y_{j1}, \dots, Y_{jk})$.

Therefore M is k -semi-FSR realizable with respect to π . Q.E.D.

Theorem 2: Let M be a sequential machine. Then the following four conditions are equivalent.

(i) There exist p binary output functions z_1, \dots, z_p , such that M is (k_1, \dots, k_p) -output-observable with respect to the output function $z_1 \times \dots \times z_p$ and a decomposition π .

(ii) There exist p binary output functions z_1, \dots, z_p , and p decompositions π_1, \dots, π_p , such that M is k_i -output-observable with respect to z_i and π_i for $1 \leq i \leq p$, and $\pi_1 + \dots + \pi_p = \pi$.

(iii) There exist p decompositions π_1, \dots, π_p , such that M is k_i -semi-FSR realizable with respect to π_i for $1 \leq i \leq p$, and $\pi_1 + \dots + \pi_p = \pi$.

(iv) M is (k_1, \dots, k_p) -semi-FSR realizable with respect to π .

Proof: From Lemma 2, (i) and (ii) are equivalent. From Theorem 1 (ii) and (iii) are equivalent. And it follows immediately from Lemma 1 that (iii) is equivalent to (iv). Q.E.D.

3. Output-Observable Sequential Machines

In this section we show an algorithm for modifying a given machine to an output-observable one by adding a minimum number of extra outputs.

Observing output sequence at the output terminal z , we can find a maximum decomposition π and a minimum k , such that the sequential machine is k -output-observable with respect to z and π . This method is shown in the following.

Procedure A:

(1) Set $\pi(0) = O$, $k=1$, and $\ell=1$.

(2) Test whether every output response of length ℓ at the output z is determined only by the initial state independently of input sequences. If "no", set $\pi = \pi(\ell-1)$, and stop. If "yes", go to step (3).

(3) Let $\mu_i(\ell)$ be the output sequence of length ℓ corresponding to a state S_i . Define a relation $\sim_{\pi(\ell)}$, such that

$$S_i \sim_{\pi(\ell)} S_j \iff \mu_i(\ell) \neq \mu_j(\ell).$$

(4) If $\pi(\ell) > \pi(\ell-1)$, set $k = \ell$.

(5) If $\pi(\ell) < I$, set $\ell = \ell + 1$, and go to step (2). Otherwise set $\pi = \pi(\ell)$, and stop.

Suppose that, for a given sequential machine M , π_i and k_i ($i=1, \dots, r$) have been obtained by means of Procedure A, then M is k_i -output-observable with respect to the output function z_i and a decomposition π_i for each i ($1 \leq i \leq r$). If $\pi_1 + \dots + \pi_r = I$, then M is output-observable. If $\pi_1 + \dots + \pi_r < I$, then we have the following theorem.

Theorem 3: The necessary and sufficient condition for a sequential machine M to be modified by adding s binary output functions w_1, \dots, w_s so that it will be $(k_1, \dots, k_r, \ell_1, \dots, \ell_s)$ -output-observable with respect to the output function $z_1 \times \dots \times z_r \times w_1 \times \dots \times w_s$ is that M is (ℓ_1, \dots, ℓ_s) -semi-FSR realizable with respect to π , such that $\pi + \pi_1 + \dots + \pi_r = I$.

Proof: This can be proved readily from Theorem 2 and the fact that M is k_i -output-observable with respect to z_i and π_i for each i ($i=1, \dots, r$).

With these preparations, we are now to describe a modification algorithm of sequential machines to output-observable ones.

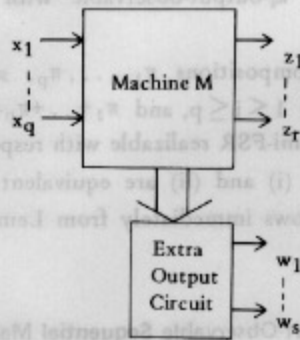


Fig. 3 Illustration of Theorem 3

Procedure B – Modification Algorithm:

- (1) Given a sequential machine M having binary output functions z_1, \dots, z_r , find a maximum decomposition π_i and a minimum k_i for each z_i ($i=1, \dots, r$) by means of Procedure A.
- (2) Construct a minimum decomposition π such that $\pi + \pi_1 + \dots + \pi_r = I$.
- (3) Set $s=1$.
- (4) Test whether M is (l_1, \dots, l_s) -semi-FSR realizable with respect to π for some integers l_1, \dots, l_s . If M is not semi-FSR realizable, set $s=s+1$, and go to step (4).
- (5) Let Y_{ij} ($i=1, \dots, s; j=1, \dots, l_i$) be the state assignment variables of the feedback-shift-registers shown in Fig. 2, and let $(Y_{11}^i, Y_{12}^i, \dots, Y_{l_1}^i; \dots; Y_{s1}^i, \dots, Y_{l_s}^i)$ be a binary code corresponding to a state S_i . Define binary output function w_j ($1 \leq j \leq s$), such that $w_j(S_i) = Y_{j l_j}^i$ for $S_i \in S$.

Table 1 Machine M_1

P. S.	N. S., z_1	
	$x = 0$	$x = 1$
1	4,0	2,0
2	3,0	2,0
3	4,1	3,1
4	5,1	5,1
5	5,1	1,1

Table 2 State assignment

	Y_1	Y_2
1	0	1
2	0	0
3	0	0
4	1	0
5	1	1

Table 3 Modified machine M_2

P.S.	N. S., $z_1 z_2$	
	$x = 0$	$x = 1$
1	4,01	2,01
2	3,00	2,00
3	4,10	3,10
4	5,10	5,10
5	5,11	1,11

Example 1: To illustrate Procedure B, consider a sequential machine M_1 given by Table 1 which is not output-observable. Let us modify M_1 to an output-observable machine by Procedure B. The determination of a minimum number of additional output functions is shown below, where each step is indicated by the corresponding number.

(1) Applying Procedure A, we can obtain $k_1=1$, and $\pi_1 = [13, 14, 15, 23, 24, 25]$.

(2) The minimum decomposition π , such that $\pi + \pi_1 = I$, is $\pi = [12, 345]$.

(3) $s=1$.

(4)* M is 2-semi-FSR realizable with respect to π . The state assignment is shown in Table 2.

(5) By adding output function z_2 such that $z_2=Y_2$, we can obtain the modified sequential machine M_2 shown in Table 3 which is (1, 2)-output-observable with respect to $z_1 \times z_2$.

4. Fault Detections for Output-Observable Sequential Machines

* State assignment problem of semi-FSR realization is the simple extension of that of FSR realization.

In this section we consider fault detection experiments for (k_1, \dots, k_p) -output-observable sequential machines. Assume that the class of allowable failures satisfies the following conditions.

- (1) Any failure which occurs is assumed to occur throughout the test.
- (2) Faulty machines are still (k'_1, \dots, k'_p) -output-observable such that $k'_i \leq k_i$ for each i ($1 \leq i \leq p$).

In Section 2 we have shown that (k_1, \dots, k_p) -output-observable sequential machines can be realized as binary FSR's of the form shown in Fig. 2. For sequential machines with shift registers, the above failure assumption (2) means that the structure of shift registers is preserved and the number of stages of each shift register does not increase even though the sequential machine might be faulty.

Under these assumptions, let us design a checking sequence. Given a (k_1, \dots, k_p) -output-observable sequential machine M , let ω_1 be the shortest input-output sequence that passes through all transitions of the state table of M , and let ω_2 be an arbitrary input-output sequence of length k which succeeds ω_1 , where $k = \max [k_1, \dots, k_p]$. It will be proved in the following theorem that the input-output sequence $\omega_1\omega_2$, called C-sequence, is a checking sequence.

Theorem 4: Let M be an output-observable sequential machine. Then the sequential machine satisfying* the C-sequence of M is either isomorphic to M or covers M .

Proof: Let $M' = (S', I, Z, \delta', \lambda')$ be a sequential machine satisfying the C-sequence of M . From the failure assumption, M' is (k'_1, \dots, k'_p) -output-observable such that $k'_i \leq k_i$ for each $1 \leq i \leq p$. Let S_t and S'_t be the states of M and M' respectively at time t in the C-sequence. Define a mapping $f: S \rightarrow S'$ such that $f(S_t) = S'_t$ for each time t . We first show that this yields a well-defined mapping.

Now suppose that $S'_{t_1} \neq S'_{t_2}$ at time t_1 and t_2 . This implies that $z_i(t_1)z_i(t_1+1) \dots z_i(t_1+k'_i-1) \neq z_i(t_2)z_i(t_2+1) \dots z_i(t_2+k'_i-1)$ for some i , since M' is (k'_1, \dots, k'_p) -output-observable. Therefore $z_i(t_1) \dots z_i(t_1+k_i-1) \neq z_i(t_2)z_i(t_2) \dots z_i(t_2+k_i-1)$. This implies $S_{t_1} \neq S_{t_2}$ for $S_{t_1}, S_{t_2} \in S$, since M is (k_1, \dots, k_p) -output-observable. Hence $S'_{t_1} \neq S'_{t_2}$ implies $S_{t_1} \neq S_{t_2}$. This shows that f is well-defined.

Let I_t and Z_t be the input and output symbol respectively at time t in the C-sequence. From the definitions of f , we have

$$f(\delta(S_t, I_t)) = f(S_{t+1}) = S'_{t+1} = \delta'(S'_t, I'_t), \text{ and}$$

$$\lambda(S_t, I_t) = Z_t = \lambda'(S'_t, I'_t) = \lambda'(f(S_t), I_t) \text{ for any time } t.$$

This holds for all states and all input symbols of M , since the C-sequence passes through all transitions of the state table of M . Hence f is a homomorphism of M into M' , and M' covers M . If the number of states of M' is equal to that of M , then f is an

* We say that a sequential machine satisfies an input-output sequence if, applying the input sequence, the output sequence is obtained.

isomorphism of M onto M' is isomorphic to M . Q.E.D.

Theorem 4 implies that only the correctly-operating machine satisfies the C-sequence of M . However the converse is not always true, i.e., the correctly-operating machine does not always satisfy the C-sequence when the machine under test is not initially in the starting state of the C-sequence of M . So the machine should be initially in the starting state of the C-sequence when the C-sequence is to be applied.

This can be done by using the initializing sequence of length at most $k+n$, where $k = \max [k_1, \dots, k_p]$ and n is the number of states, since the machine is (k_1, \dots, k_p) -output-observable. Then we have the following corollary of Theorem 4.

Corollary 1: The C-sequence of an output-observable sequential machine M is a checking sequence.

Since a checking sequence must check all transitions of the given state table, it must pass through all transitions. Hence the input-output sequence ω_1 , which is the prefix of the C-sequence $\omega_1\omega_2$, is shorter than every possible checking sequence, and consequently shorter than the minimum length checking sequence. The length of input-output sequence ω_2 , which is the suffix of the C-sequence $\omega_1\omega_2$, is $k = \max [k_1, \dots, k_p]$. Hence the C-sequence is not k longer than the minimum checking sequence. In general, k is smaller than the number of states of M . Therefore, the C-sequence* is nearly minimum.

Example 2: Consider machine M_2 , given in Table 3, which is (1, 2)-output-observable with respect to output function z_1xz_2 . Let $k = \max [1, 2] = 2$. By applying an arbitrary input sequence of length k and observing the output sequences of length 1 and 2 at the output terminals z_1 and z_2 respectively, we can establish the initial state and the final state. Suppose that the machine is in the state 1, then the shorter input-output sequence ω_1 , that passes through all transitions of M_2 , is obtained as follows:

Input	0	0	1	1	0	1	0	1	1
State	1	4	5	5	1	2	2	3	3
Output z_1	0	1	1	0	0	0	1	1	1
Output z_2	1	0	1	1	0	0	0	0	0

As the final state is 5, the following sequence is an input-output sequence ω_2 of length 2 starting at the state 5:

Input	0	0
State	5	5
Output z_1	1	1
Output z_2	1	1

* The problem of constructing the C-sequence can be reduced to the travelling salesman problem.

Then a checking sequence for M_2 is the following:

Input	0	0	0	1	1	1	0	1	0	1	0	0
State	1	4	5	5	1	2	2	3	3	4	5	5
Output	z_1	0	1	1	1	0	0	0	1	1	1	1
	z_2	1	0	1	1	1	0	0	0	0	1	1

5. Conclusion

In this paper we have described a procedure for the modification of a given sequential machine to an output-observable one by adding minimum number of extra outputs, and showed that for an output-observable sequential machine we can organize a nearly minimum checking sequence systematically. This procedure is mainly based upon the fact that the output-observability of a sequential machine is equivalent to the semi-FSR realizability of it. Hence it may be desired to find a more efficient state assignment for a minimum stage semi-FSR realization.

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References

- 1) F. C. Hennie, Prof. 5th Ann. Symp. Switching Theory and Logical Design, 1964.
- 2) C. R. Kime, Tech. Rep., Univ. of Iowa City, 66-13, 1966.
- 3) S. Murakami, K. Kinoshita, and H. Ozaki, IEEE Trans. Comput., vol. C-19, 1970, pp. 1079-1085.
- 4) C. E. Holborow, IEEE Trans. Comput., vol. C-21, 1972, p. 596-598.
- 5) Z. Kohavi and P. Lavalley, IEEE Trans. Electron. Comput., vol. EC-16, 1967, pp. 473-484.
- 6) R. L. Martin, Proc. Hawaii Internat. Conf. Syst. Sci., 1968.
- 7) K. Nakamura and T. Kasami, Inst. Electron. Comm. Eng. Japan Rec. Prof. Group on Automata and Information Theory, AIT69-43-39, 1971 (in Japanese).
- 8) Y. Kambayashi and S. Yajima, J. Inf. Process. Soc. Japan, vol. 12, 1971, (in Japanese).
- 9) T. Kawata, K. Kinoshita, and H. Ozaki, J. Inst. Electron. Comm. Eng. Japan, 1969, (in Japanese).
- 10) H. Fujiwara and K. Kinoshita, J. Inst. Electron. Comm. Eng. Japan, 1972, (in Japanese).
- 11) H. Fujiwara and K. Kinoshita, Inst. Electron. Comm. Eng. Japan, Rec. Prof. Group on Electronic Computer, EC-72-36, 1972, (in Japanese).
- 12) D. R. Haring, "Sequential-Circuit Synthesis: State Assignment Aspects," M.I.T. Press, Cambridge, Mass., 1966.
- 13) R. L. Martin, "Studies in Feedback-Shift-Register Synthesis of Sequential Machines," M.I.T. Press, Cambridge, Mass., 1969.