話の内容

- 私の履歴書
- テスト生成アルゴリズムの歴史
- 余談(FAN, 非スキャン)
- ベンチマークの歴史

The basis is necessary for development
発展には基礎が必要

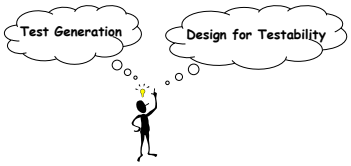
- For a tree to grow larger, its root must grow bigger and deeper into the ground.
- Similarly, for test technologies (leaves) to develop, substantial results of the fundamental research (root) are necessary.
- The more enriched the fundamental research results become, the more enriched the practical research results become.

Fundamental problems of testing
テストの基本

What are the fundamentals of testing?

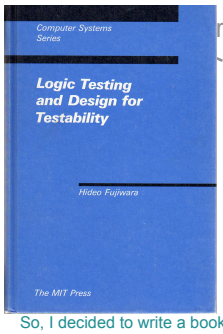
I had the opportunity to ask myself the same question 28 years ago when I was requested to write a book from MIT Press.

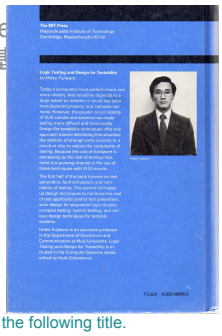
Fundamental problems of testing
テストの基本



So, I decided to write a book with the following title.

Hideo Fujiwara, *Logic Testing and Design for Testability*, The MIT Press, 1985





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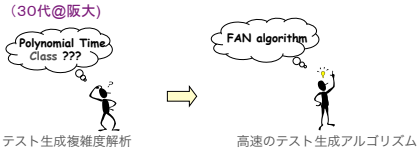
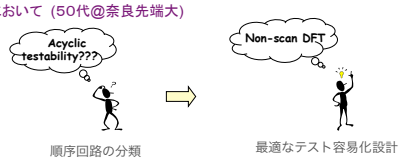
私の経験から
理論的・基礎的研究が実用的研究に貢献する

テスト生成において（30代@阪大）



テスト生成複雑度解析　　高速のテスト生成アルゴリズム

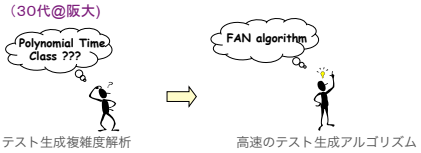
テスト容易化設計において（50代@奈良先端大）



順序回路の分類　　最適なテスト容易化設計

私の経験から
理論的・基礎的研究が実用的研究に貢献する

テスト生成において（30代@阪大）



テスト容易化設計において（50代@奈良先端大）

Complexity of test generation
テスト生成複雑度 [Fujiwara, et al, IEEE Trans. Comp, 1982]

- *Fault detection* (FD): Is a given single stuck-at fault detectable?
  kM-FD: Fault detection problem for k-level monotone circuits
  kU-FD: Fault detection problem for k-level unate circuits

- *Theorem 1 :*
  3M-FD is NP-complete.
  Hence,
  3U-FD and FD are NP-complete.

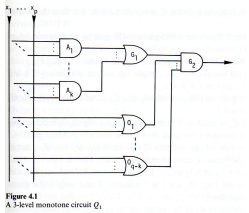
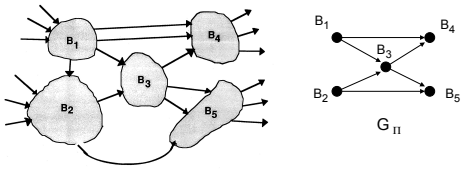


Figure 4.1
A 3-level monotone circuit Q_1

Complexity of test generation
テスト生成複雑度 [Fujiwara, et al, IEEE Trans. Comp, 1982]

- A combinational circuit C is said to be *k-bounded* if there exists a partition $\Pi=\{B_1, B_2, \ldots, B_l\}$ such that
  (1) the number of inputs of each block Bi is at most *k*, and
  (2) graph G_Π has no cycle.



Complexity of test generation
テスト生成複雑度 [Fujiwara, et al, IEEE Trans. Comp, 1982]

- *Theorem 2:* Let C be a *k-bounded* circuit. Then there is an algorithm of time complexity $O(16^k m)$ to find a test for a single stuck-at fault in C, where m is the number of lines in C.

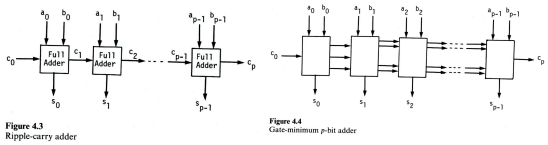
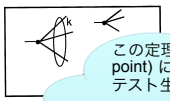


Figure 4.3
Ripple-carry adder

Figure 4.4
Gate-minimum *p*-bit adder

3-bounded circuit *6-bounded circuit*

Complexity of test generation
テスト生成複雑度 [Fujiwara, et al, IEEE Trans. Comp, 1982]



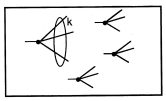
この定理の証明で、分岐点(fanout-point) に0,1,D, D'の４値を割り当てるテスト生成アルゴリズムを示した。

このアルゴリズムが、後のFANアルゴリズムの元になった。

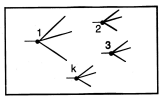
- k-FL-FD: Fau
- k-FPB-FD: Fault detecti nded circuits

- *Theorem 3 :*
  k-FL-FD is NP-complete if k>2.
  k-FPB-FD is solvable in $O(4^k m)$ where m is the number of lines in C.

Complexity of test generation
テスト生成複雑度 [Fujiwara, et al, IEEE Trans. Comp, 1982]



k-fanout-limited



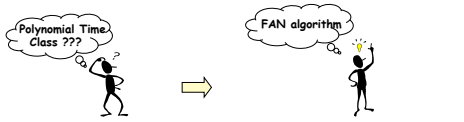
k-fanout-point-bounded

- Observation:
  k-FL-FD is NP-complete even if k is a constant.
  k-FPB-FD is solvable in O(m) if k is a constant.

- The complexity of test generation is affected
  not by the number of fanout branches from a fanout point
  but by the number of fanout points.

Complexity of test generation
テスト生成複雑度 [Fujiwara, et al, IEEE Trans. Comp, 1982]

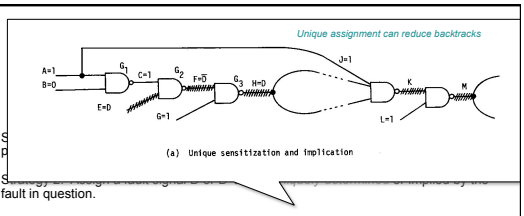
定理の証明で示したアルゴリズムが，FANアルゴリズムの元になった。

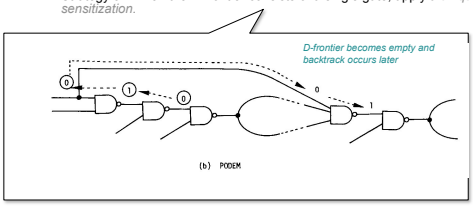


テスト生成複雑度解析　　高速のテスト生成アルゴリズム

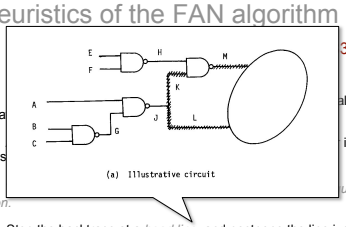
Heuristics of the FAN algorithm
[Fujiwara, et al, IEEE Trans. Comp., 1983]

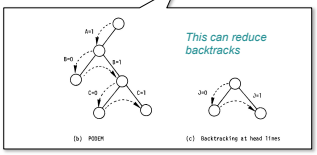
- Strategy 1: In each step of the algorithm, determine as many signal values as possible that can be *uniquely implied*.
- Strategy 2: Assign a fault signal D or D' that is *uniquely determined* or implied by the fault in question.
- Strategy 3: When the D-frontier consists of a single gate, apply a *unique sensitization.*
- Strategy 4: Stop the backtrace at a *head line*, and postpone the line justification for the head line to later.
- Strategy 5: *Multiple backtracing* (concurrent backtracing of more than one path) is more efficient than backtracing along a single path.
- Strategy 6: In the multiple backtrace, if an objective at a fanout point p has a contradictory requirement, stop the backtrace so as to *assign a binary value to the fanout point.*



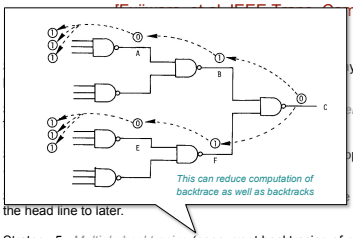


Heuristics of the FAN algorithm





Heuristics of the FAN algorithm



Heuristics of the FAN algorithm
[Fujiwara, et al, IEEE Trans. Comp., 1983]

- Strategy 1: In each step of the algorithm, determine as many signal values as possible that can be *uniquely implied*.

PODEM assigns a binary value only to primary inputs.
So, backtracks occur at primary inputs.

FAN assigns a binary value only to head lines and fanout points.
So, backtracks occur at headlines and fanout points.

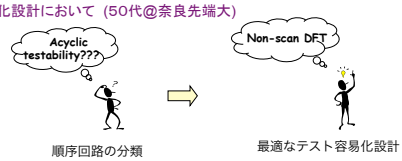
This is effective to reduce the number of backtracks.

- Strategy 6: In the multiple backtrace, if an objective at a fanout point p has a contradictory requirement, stop the backtrace so as to *assign a binary value to the fanout point.*

私の経験から
理論的・基礎的研究が実用的研究に貢献する

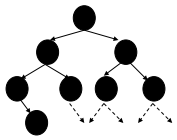
テスト生成において（30代@阪大）

つぎに、テスト容易化設計において（50代@奈良先端大）



Classification of sequential circuits
Combinational test generation complexity

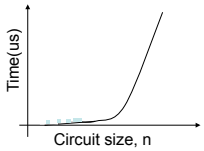
Theoretically,



CTG is NP-hard.

CTG = Combinational Test Generation Problem

Empirically,



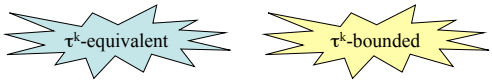
CTG seems to be solved in time $O(n^r)$ for some constant r.

[Goel 1980], [Prasad 1999]

Classification of sequential circuits
τ^k notation

[Fujiwara, IEEE Trans. Comp., 2000]
[Fujiwara, et al, IEEE Trans. CAD, 2008]

- Introduced **τ^k notation** to clarify the time complexity for the test generation problem.



- Classified sequential circuits based on **τ^k notation** .

Classification of sequential circuits
Test generation complexity

[Fujiwara, IEEE TCAD, 2008]

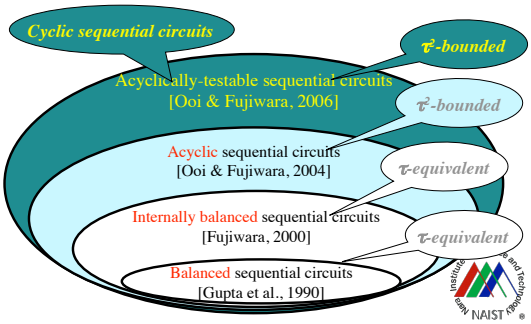
- Let
  - P_C : combinational test generation problem.
  - P_S : sequential test generation problem.
  - P_α : class α test generation problem.
- Let $T_C(n)$, $T_S(n)$ and $T_\alpha(n)$ be the *time complexity* of P_C , P_S and P_α respectively.
- We assume that $T_C(n) = \Theta(n^r)$ for some constant r larger than 2.
- *Combinational test generation complexity:* $\tau(n) = T_C(n)$

Classification of sequential circuits
τ^k-equivalent and τ^k-bounded

[Fujiwara, IEEE TCAD, 2008]

- A class α is *τ^k-equivalent* if $T_\alpha(n)=\Theta(\tau^k(n))$
  and *τ^k–bounded* if $T_\alpha(n)=O(\tau^k(n))$
  where k is a positive integer.
- A class of circuits with *combinational test generation complexity* is *τ-equivalent*

Classification of sequential circuits
Class of acyclic test generation complexity



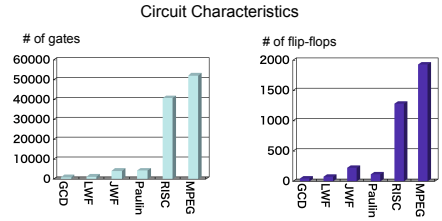
Classification of sequential circuits
Design for acyclic testability

- Introduced two classes of acyclically-testable circuits
  - Thru-testable circuits (at gate level) [C.Y.Ooi, H.Fujiwara, ICCD 2006]
  - Linear-depth time-bounded circuits (at RTL) [H.Iwata, T.Yoneda, H.Fujiwara, DAC 2007]
- Proposed Non-Scan type DFT for acyclic testability
  - Non-scan
  - At-speed test
  - 100% fault efficiency
  - Hardware overhead is lower than Full Scan
  - Test application time is much shorter than Full Scan

Design for acyclic testability

[Fujiwara, et al, IEEE Trans. CAD, 2008]

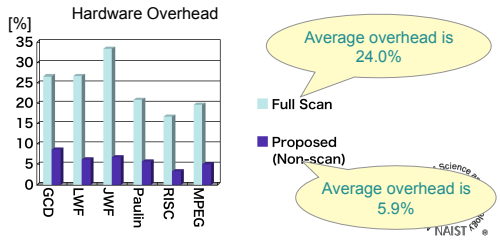
- Linear-depth time-bounded RTL circuits



Design for acyclic testability

[Fujiwara, et al, IEEE Trans. CAD, 2008]

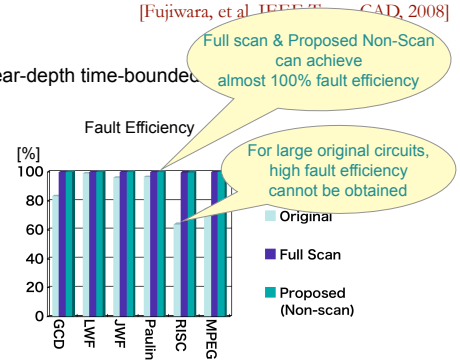
- Linear-depth time-bounded RTL circuits



Design for acyclic testability

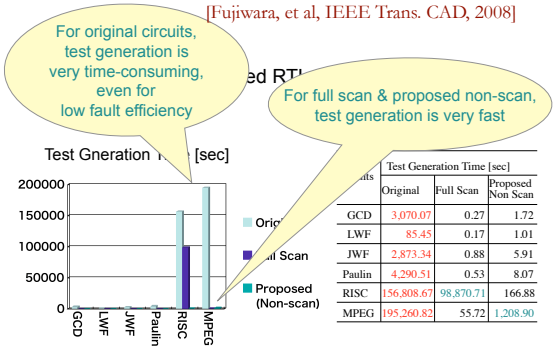
[Fujiwara, et al, IEEE Trans. CAD, 2008]

- Linear-depth time-bounded



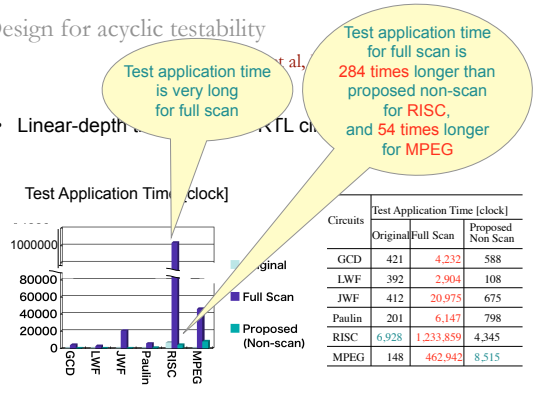
Design for acyclic testability

[Fujiwara, et al, IEEE Trans. CAD, 2008]



	Test Generation Time [sec]		
	Original	Full Scan	Proposed Non Scan
GCD	3,070.07	0.27	1.72
LWF	85.45	0.17	1.01
JWF	2,873.34	0.88	5.91
Paulin	4,290.51	0.53	8.07
RISC	156,808.67	98,870.71	166.88
MPEG	195,260.82	55.72	1,208.90

Design for acyclic testability



Circuits	Test Application Time [clock]		
	Original	Full Scan	Proposed Non Scan
GCD	421	4,232	588
LWF	392	2,904	108
JWF	412	20,975	675
Paulin	201	6,147	798
RISC	6,928	1,233,859	4,345
MPEG	148	462,942	8,515