ISCAS'89 1989 International Symposium on Circuits and Systems
1989 Portland, Oregon

Special Session: Benchmarks for Sequential Test Generation
Chairs: B. Krishnamurthy
Tektronix Labs
Beaverton, OR

H. Fujiwara
Meiji University
Kawasaki, Japan

1. **Combinational Profiles of Sequential Benchmark Circuits,**
F. Brglez, D. Bryan and K. Kozminski, *MCNC, Research Triangle Park, NC.*
2. **A Concurrent Test Generator for Sequential Circuit Testing,**
V. Agrawal and K-T. Cheng, *AT&T Bell Labs, Murray Hill, NJ.*
3. **Sequential Circuit Test Generator (STG) Benchmark Results,**
S. Davidson and W-T. Cheng, *AT&T Engineering Research Center, Princeton, NJ.*
4. **Two Test Generation Methods for Sequential Circuits,**
T. Hayashi, *Hitachi Research Laboratory, Ibaraki-ken, Japan.*
5. **The Complexity of Sequential ATPG,**
A. Lioy, *Politecnico di Torino, Torino, Italy.*
6. **The Coupling of Sequential ATG with Partial Scan,**
R. Marlett, *HHB Systems, Mahwah, NJ.*
7. **Benchmarking Results for a Sequential ATPG Program,**
T. Sridhar, *Gateway Automation, Lowell, MA.*

ベンチマークの歴史

1983年 (37歳) FANアルゴリズム FTCS-13@Milano
1984年 (38歳) 在外研究 McGill Univ.@Montreal
1985年 (39歳)
1988年 (42歳)
1989年 (43歳)

テスト生成アルゴリズム用のベンチマークとして、ISCAS85ベンチマークを第1世代と考えれば、ISCAS89ベンチマークは第2世代と考えることができる。その後，テスト生成の対象となる回路規模は増大の一歩をたどり、より大規模で現実的な新しいベンチマークの必要性を問うた（H. Fujiwara、"Needed, Third-generation ATPG benchmarks", The Last Byte, IEEE Design & Test of Computers, p.96, 1998.）

1998年 (52歳) The Last Byte H.Fujiwara@IEEE_Design&Test
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THE LAST BYTE

Needed: Third-generation ATPG benchmarks

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In 1983 I published the FAN algorithm, and by using actual combinational circuits, showed its superiority over both the D-algorithm (by J.P. Roth) and the PODEM algorithm (by P. Goel). In 1984 I discussed ATPG (automatic test pattern generation) benchmarking with Franc Brglez (then with Bell Northern Research and now with North Carolina State University) while I was on sabbatical visiting Vinod Agarwal at McGill University.

Before this, we had no benchmarks for ATPG algorithms. Brglez and I agreed that benchmark circuits helped advance ATPG algorithm research and development. We organized a special session on combinational ATPG benchmarking at ISCAS 85 (the 1985 International Symposium on Circuits and Systems) in Kyoto, Japan. With the cooperation of many people from industry and universities in the USA, Canada, Europe, and Japan, we collected excellent benchmarks with various and useful characteristics.

Later, others reported many better, more-efficient ATPG algorithms for combinational circuits. The widespread availability of these benchmarks drove the development of new algorithms, as researchers strove to generate the best-known results in terms of runtime, vector length, and fault coverage.

Today, new benchmarks are required again. The existing ISCAS 85/89 benchmarks are no longer close to the size of industrial designs. We need much larger circuits (perhaps several million gates) to realistically study ATPG efficiency. We need circuits with features found in modern designs and not found in the current benchmarks. We encourage the development of advanced ATPG algorithms that can achieve almost 100% fault efficiency for very large, realistic circuits within practical computation time.

The current benchmarks are described in a simple netlist format. Future benchmarks should be available at the behavioral, register-transfer, and gate levels. They should be described in a high-level language such as VHDL to facilitate research on high-level ATPG.

The ISCAS 85 benchmarks were first-generation benchmarks for ATPG algorithms, and the ISCAS 89 benchmarks were the second generation. We now need a third generation to tackle urgent current issues and continue to stimulate research on solutions for future issues. Perhaps the solutions to the impossible challenges of today, when represented in third-generation benchmarks, will become the new products of tomorrow.